# Intel - EP20K200EQC240-2X Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 832 |
| Number of Logic Elements/Cells | 8320 |
| Total RAM Bits | 106496 |
| Number of I/O | 168 |
| Number of Gates | 526000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k200eqc240-2x |

*Table 2. Additional APEX 20K Device Features* *Note (1)*

| Feature | EP20K300E | EP20K400 | EP20K400E | EP20K600E | EP20K1000E | EP20K1500E |
|---|---|---|---|---|---|---|
| Maximum system gates | 728,000 | 1,052,000 | 1,052,000 | 1,537,000 | 1,772,000 | 2,392,000 |
| Typical gates | 300,000 | 400,000 | 400,000 | 600,000 | 1,000,000 | 1,500,000 |
| LEs | 11,520 | 16,640 | 16,640 | 24,320 | 38,400 | 51,840 |
| ESBs | 72 | 104 | 104 | 152 | 160 | 216 |
| Maximum RAM bits | 147,456 | 212,992 | 212,992 | 311,296 | 327,680 | 442,368 |
| Maximum macrocells | 1,152 | 1,664 | 1,664 | 2,432 | 2,560 | 3,456 |
| Maximum user I/O pins | 408 | 502 | 488 | 588 | 708 | 808 |

*Note to Tables 1 and 2:*
(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

*Table 3. APEX 20K Supply Voltages*

| Feature | Device | |
|---|---|---|
| | EP20K100<br>EP20K200<br>EP20K400 | EP20K30E<br>EP20K60E<br>EP20K100E<br>EP20K160E<br>EP20K200E<br>EP20K300E<br>EP20K400E<br>EP20K600E<br>EP20K1000E<br>EP20K1500E |
| Internal supply voltage ($V_{CCINT}$) | 2.5 V | 1.8 V |
| MultiVolt I/O interface voltage levels ($V_{CCIO}$) | 2.5 V, 3.3 V, 5.0 V | 1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)* |

*Note to Table 3:*
(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

## General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices.

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

***Figure 3. LAB Structure***

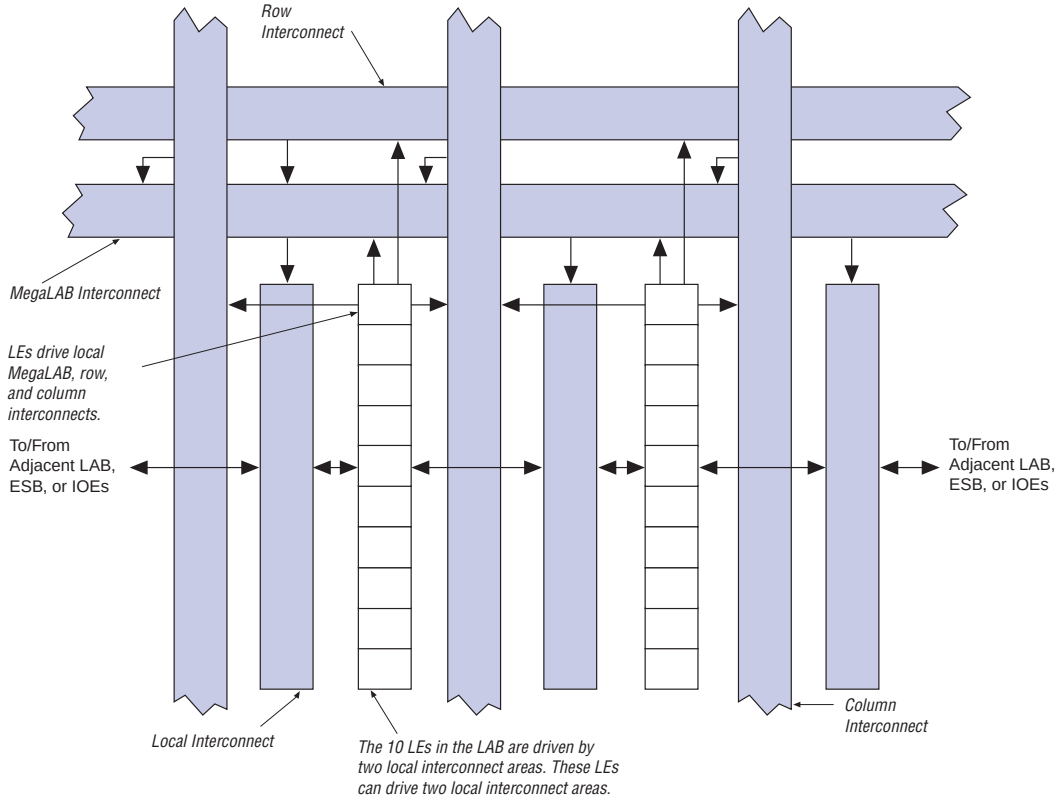
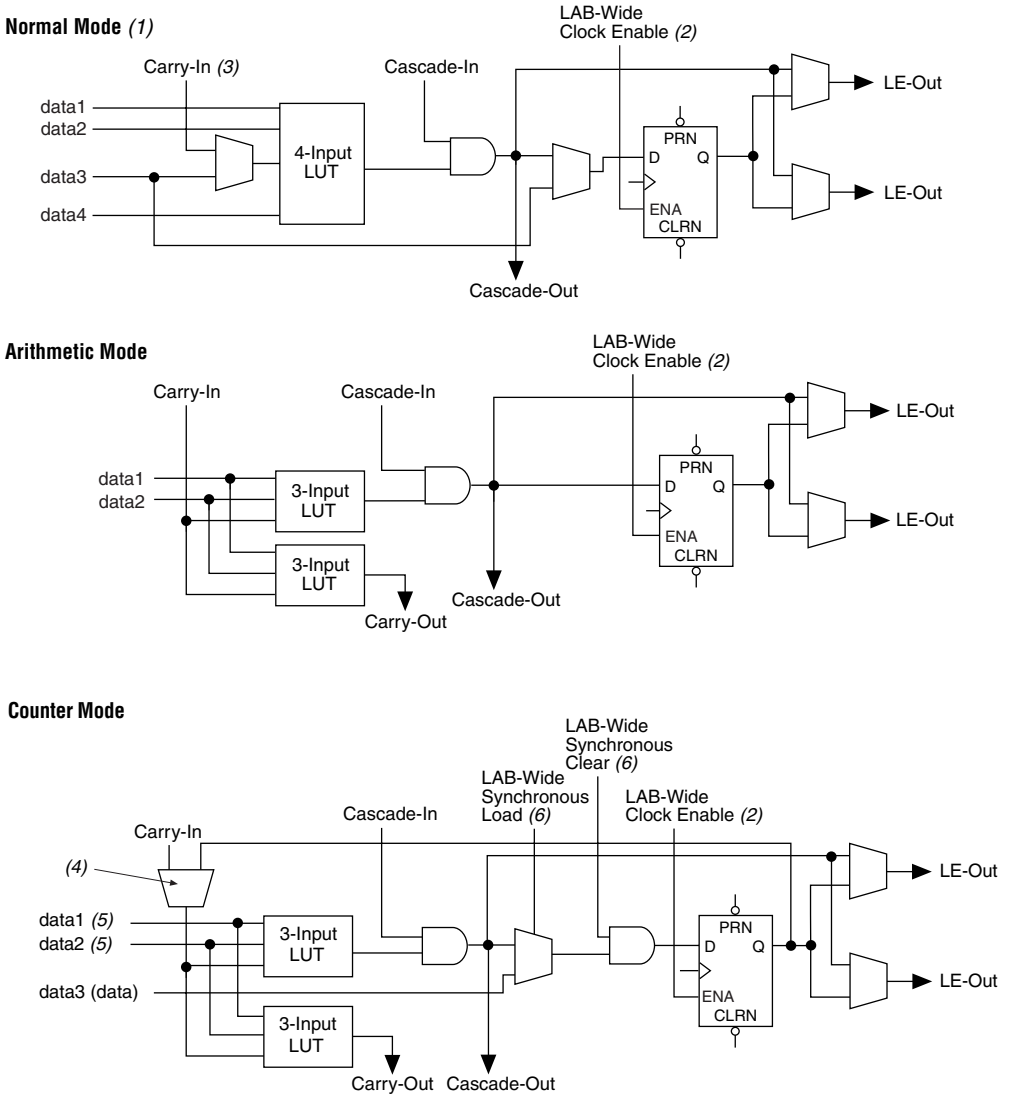


*Figure 8. APEX 20K LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

*Figure 10. FastTrack Connection to Local Interconnect*

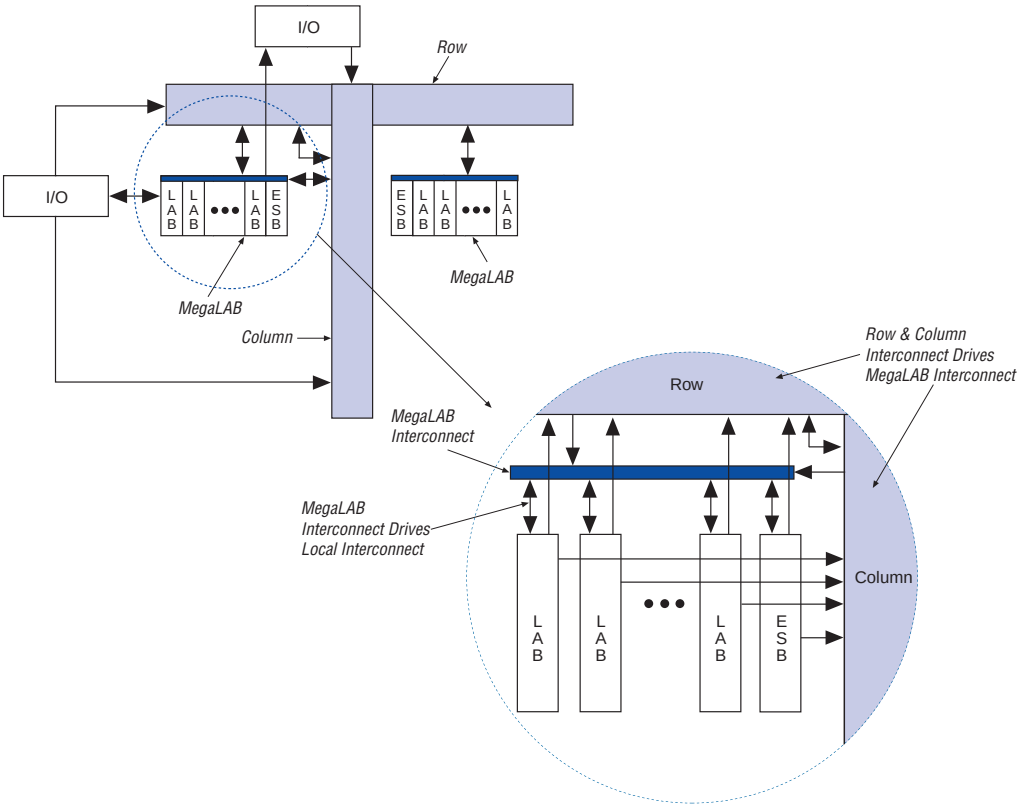


*Figure 12. APEX 20KE FastRow Interconnect*

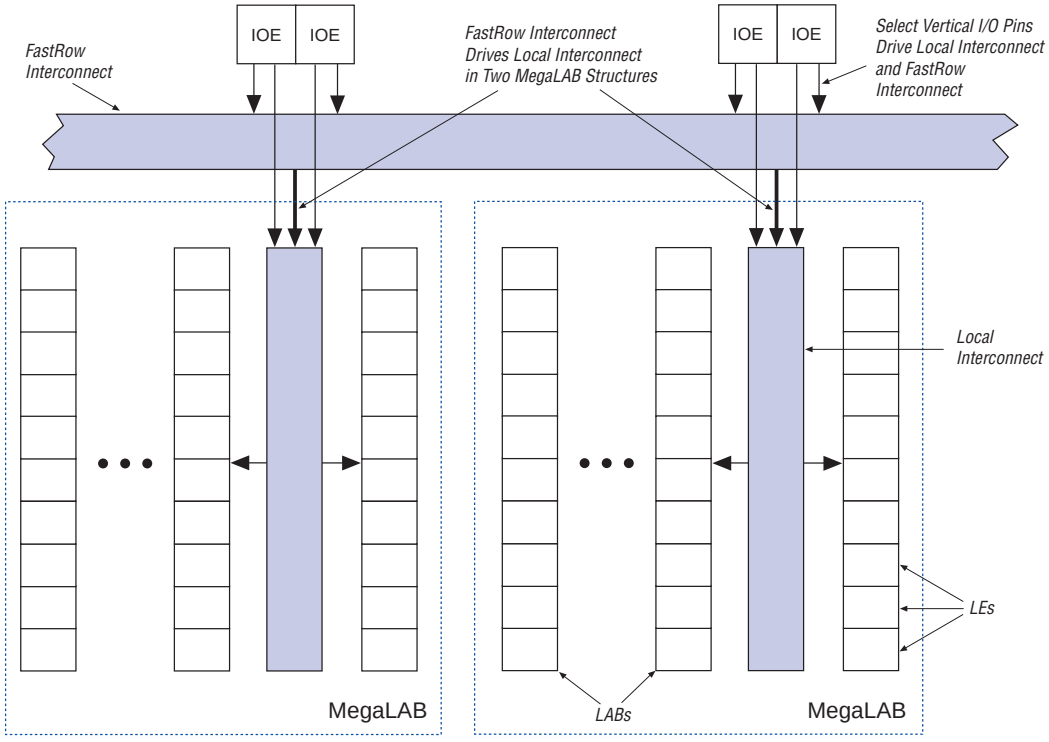
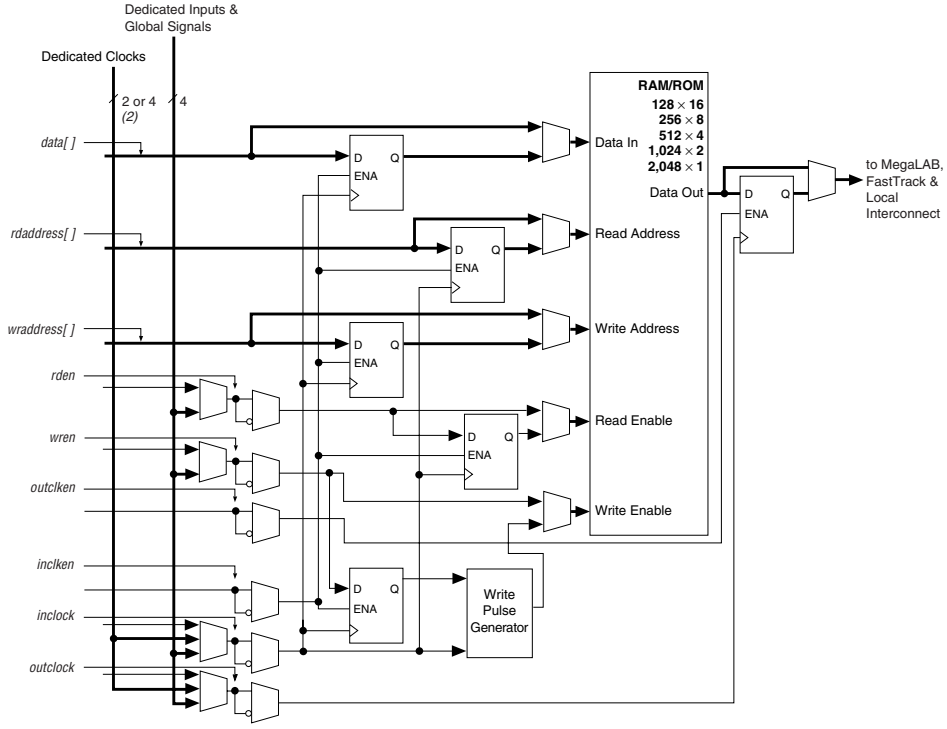



Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

***Figure 21. ESB in Input/Output Clock Mode*** *Note (1)*

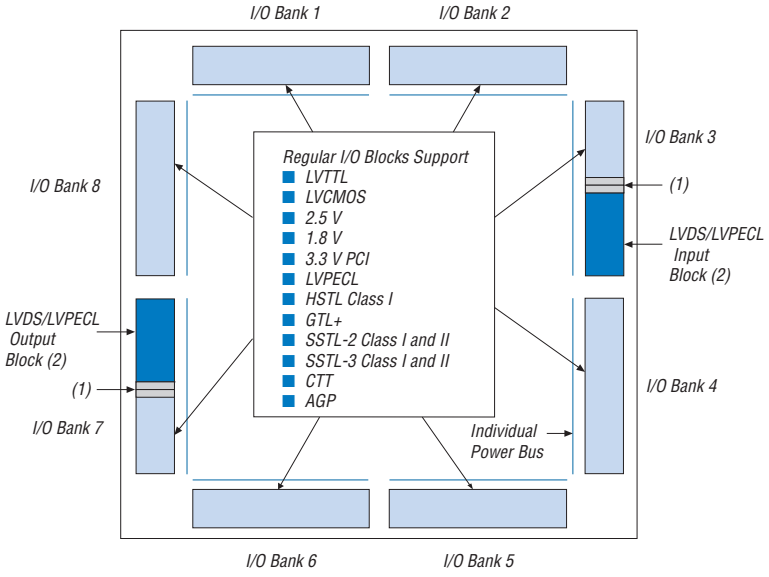



*Notes to Figure 21:*
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

*Figure 29. APEX 20KE I/O Banks*




*Notes to Figure 29:*

(1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices*).

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with $V_{CCIO}$ set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the $V_{CCIO}$ and $V_{CCINT}$ power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

## MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V $V_{CCINT}$ level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

*Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support*

| $V_{CCIO}$ (V) | Input Signals (V) | | | Output Signals (V) | | |
|---|---|---|---|---|---|---|
| | 2.5 | 3.3 | 5.0 | 2.5 | 3.3 | 5.0 |
| 2.5 | ✓ | ✓(1) | ✓(1) | ✓ | | |
| 3.3 | ✓ | ✓ | ✓(1) | ✓(2) | ✓ | ✓ |

*Notes to Table 12:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$.

(2) When $V_{CCIO}$ = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

*Table 14. Multiplication Factor Combinations*

| Clock 1 | Clock 2 |
|---|---|
| ×1 | ×1 |
| ×1, ×2 | ×2 |
| ×1, ×2, ×4 | ×4 |

## APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

### *External PLL Feedback*

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

### *Clock Multiplication*

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where $m$ and $k$ range from 2 to 160, and $n$ and $v$ range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

*Notes to Table 16:*

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus II software, designers must specify the input frequency. The Quartus II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the $t_{LOCK}$ value is less than the time required for configuration.

(4) The $t_{JITTER}$ specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

*Table 17. APEX 20KE ClockLock & ClockBoost Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $t_{INJITTER}$ | Input jitter peak-to-peak | | | | 2% of input period | peak-to-peak |
| $t_{OUTJITTER}$ | Jitter on ClockLock or ClockBoost-generated clock | | | | 0.35% of output period | RMS |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 45 | | 55 | % |
| $t_{LOCK}$ *(2), (3)* | Time required for ClockLock or ClockBoost to acquire lock | | | | 40 | µs |

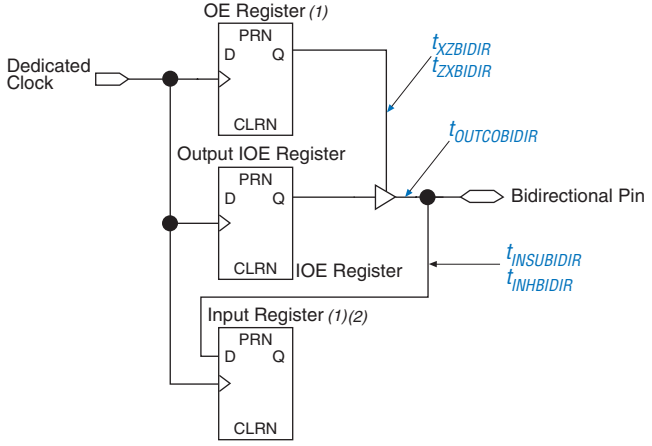
*Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions* *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4), (5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3), (6)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(9)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 1.7 | | | V |

*Figure 40. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 40:*

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the $f_{MAX}$ timing parameters shown in Figure 36 on page 68.

*Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 1 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{ESBRC}$ | ESB Asynchronous read cycle time |
| $t_{ESBWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |

| Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 2 of 2) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB macrocell register clock-to-output delay |
| $t_{F1-4}$ | Fanout delay using local interconnect |
| $t_{F5-20}$ | Fanout delay using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay using FastTrack Interconnect |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 32 and 33 describe APEX 20K external timing parameters.

| Table 32. APEX 20K External Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Clock Parameter** |
| $t_{INSU}$ | Setup time with global clock at IOE register |
| $t_{INH}$ | Hold time with global clock at IOE register |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register |

| Table 33. APEX 20K External Bidirectional Timing Parameters *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | C1 = 10 pF |

*Table 57. EP20K60E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.26 | | 0.30 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.58 | | 1.79 | ns |
| $t_{F20+}$ | | 1.96 | | 2.14 | | 2.45 | ns |

*Table 58. EP20K60E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.28 | | 0.41 | | ns |
| $t_{PREP}$ | 0.20 | | 0.28 | | 0.41 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBWP}$ | 1.29 | | 1.80 | | 2.66 | | ns |
| $t_{ESBRP}$ | 1.04 | | 1.45 | | 2.14 | | ns |

*Table 59. EP20K60E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.03 | | 2.12 | | 2.23 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{INSUPLL}$ | 1.12 | | 1.15 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |

*Table 62. EP20K100E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.61 | | 1.84 | | 1.97 | ns |
| $t_{ESBSRC}$ | | 2.57 | | 2.97 | | 3.20 | ns |
| $t_{ESBAWC}$ | | 0.52 | | 4.09 | | 4.39 | ns |
| $t_{ESBSWC}$ | | 3.17 | | 3.78 | | 4.09 | ns |
| $t_{ESBWASU}$ | 0.56 | | 6.41 | | 0.63 | | ns |
| $t_{ESBWAH}$ | 0.48 | | 0.54 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.71 | | 0.80 | | 0.81 | | ns |
| $t_{ESBWDH}$ | .048 | | 0.54 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.57 | | 1.75 | | 1.87 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.20 | | ns |
| $t_{ESBWESU}$ | 1.54 | | 1.72 | | 1.80 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.16 | | -0.20 | | -0.20 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.12 | | 0.08 | | 0.13 | | ns |
| $t_{ESBRADDRSU}$ | 0.17 | | 0.15 | | 0.19 | | ns |
| $t_{ESBDATACO1}$ | | 1.20 | | 1.39 | | 1.52 | ns |
| $t_{ESBDATACO2}$ | | 2.54 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.06 | | 3.56 | | 3.85 | ns |
| $t_{PD}$ | | 1.73 | | 2.02 | | 2.20 | ns |
| $t_{PTERMSU}$ | 1.11 | | 1.26 | | 1.38 | | ns |
| $t_{PTERMCO}$ | | 1.19 | | 1.40 | | 1.08 | ns |

*Table 63. EP20K100E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.04 | | 1.26 | | 1.52 | ns |
| $t_{F20+}$ | | 1.12 | | 1.36 | | 1.86 | ns |

*Table 78. EP20K200E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.81 | | 3.19 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.12 | 2.00 | 5.62 | 2.00 | 6.11 | ns |
| $t_{XZBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{ZXBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{INSUBIDIRPLL}$ | 3.30 | | 3.64 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.01 | 0.50 | 3.36 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |

Tables 79 through 84 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

*Table 79. EP20K300E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.17 | | 0.18 | | ns |
| $t_{H}$ | 0.31 | | 0.33 | | 0.38 | | ns |
| $t_{CO}$ | | 0.28 | | 0.38 | | 0.51 | ns |
| $t_{LUT}$ | | 0.79 | | 1.07 | | 1.43 | ns |

*Table 87. EP20K400E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.01 | | 1.12 | | 1.25 | ns |
| $t_{F20+}$ | | 3.71 | | 3.92 | | 4.17 | ns |

*Table 88. EP20K400E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.36 | | 2.22 | | 2.35 | | ns |
| $t_{CL}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.18 | | 0.19 | | ns |
| $t_{PREP}$ | 0.18 | | 0.18 | | 0.19 | | ns |
| $t_{ESBCH}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{ESBCL}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{ESBWP}$ | 1.17 | | 1.38 | | 1.56 | | ns |
| $t_{ESBRP}$ | 0.94 | | 1.09 | | 1.25 | | ns |

*Table 89. EP20K400E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.51 | | 2.64 | | 2.77 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.25 | 2.00 | 5.79 | 2.00 | 6.32 | ns |
| $t_{INSUPLL}$ | 3.221 | | 3.38 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.45 | - | - | ns |

*Table 92. EP20K600E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 2.39 | | 3.11 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 3.07 | | 3.86 | ns |
| $t_{ESBAWC}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{ESBSWC}$ | | 3.51 | | 4.62 | | 5.72 | ns |
| $t_{ESBWASU}$ | 1.46 | | 2.08 | | 2.70 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.60 | | 2.29 | | 2.97 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 2.30 | | 2.99 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.49 | | 2.30 | | 3.11 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.01 | | 0.35 | | 0.71 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.19 | | 0.62 | | 1.06 | | ns |
| $t_{ESBRADDRSU}$ | 0.25 | | 0.71 | | 1.17 | | ns |
| $t_{ESBDATACO1}$ | | 1.01 | | 1.19 | | 1.37 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 3.12 | | 4.05 | ns |
| $t_{ESBDD}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{PD}$ | | 1.57 | | 2.25 | | 2.92 | ns |
| $t_{PTERMSU}$ | 0.85 | | 1.43 | | 2.01 | | ns |
| $t_{PTERMCO}$ | | 1.03 | | 1.21 | | 1.39 | ns |

*Table 93. EP20K600E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.26 | | 1.39 | | 1.52 | ns |
| $t_{F20+}$ | | 3.51 | | 3.88 | | 4.26 | ns |