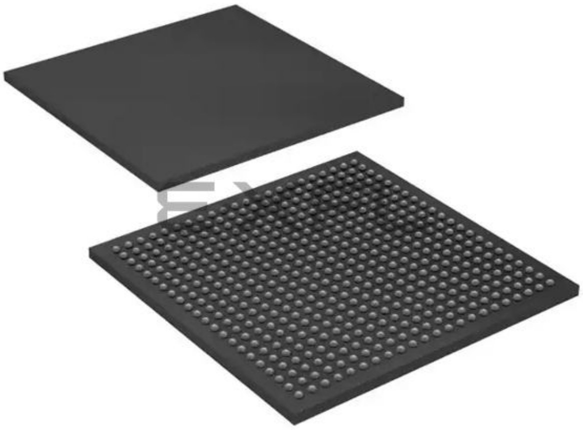

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

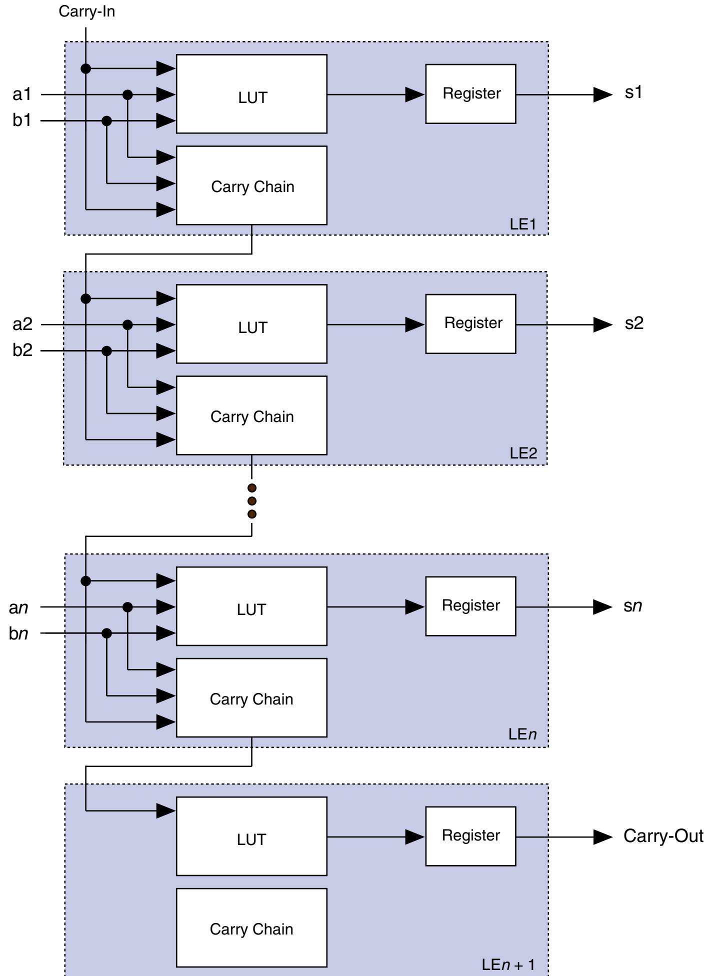
Details	
Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	382
Number of Gates	526000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200fc484-2

General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices.

Figure 6. APEX 20K Carry Chain



The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

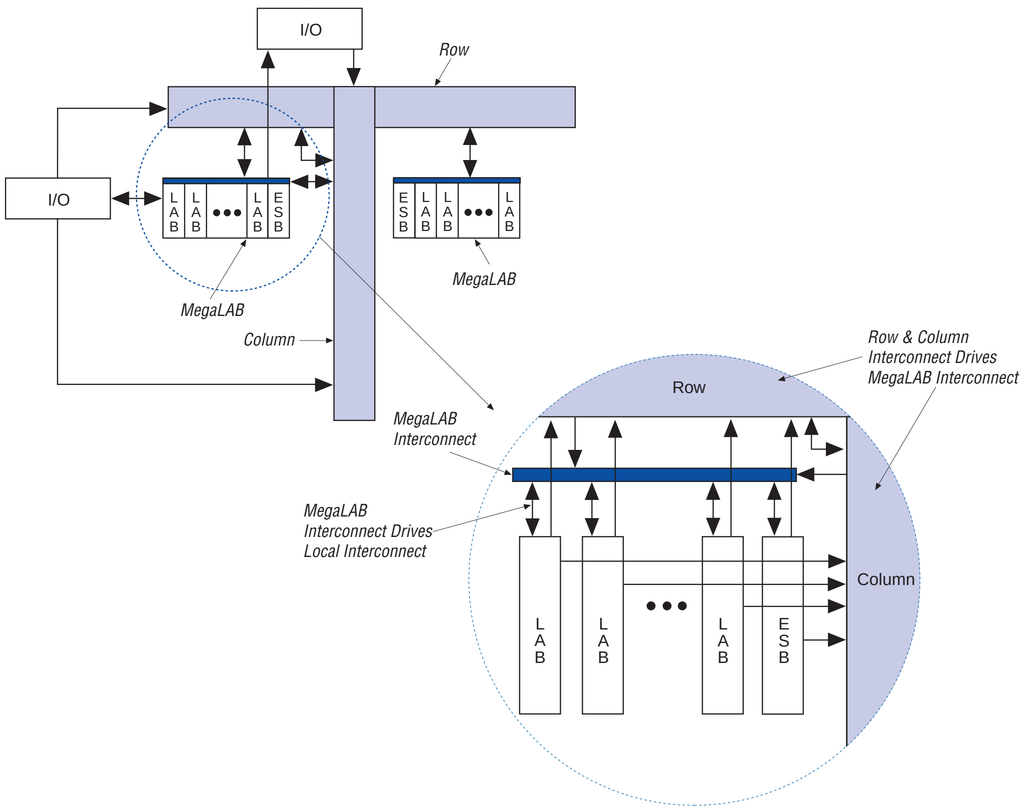
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 10. FastTrack Connection to Local Interconnect



For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to `CLK2p`. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The `CLK2p` pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (`CLK1p`) cannot be used.

Table 14. Multiplication Factor Combinations

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where m and k range from 2 to 160, and n and v range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

Table 19. APEX 20K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions *(1)*	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 19:

(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 *(1)*

Note to Table 20:
(1) This device does not support JTAG boundary scan testing.

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 21:

(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

Figure 31. APEX 20K JTAG Waveforms

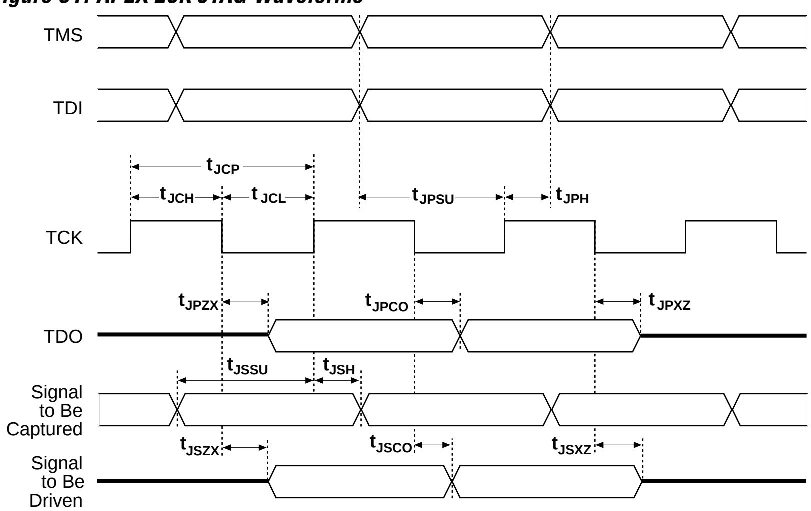


Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*, *(5)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*, *(5)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ *(9)*		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8, $0.3 \times V_{CCIO}$ *(9)*	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(10)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(10)*	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(10)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(10)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(10)*	1.7			V

Figure 33. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

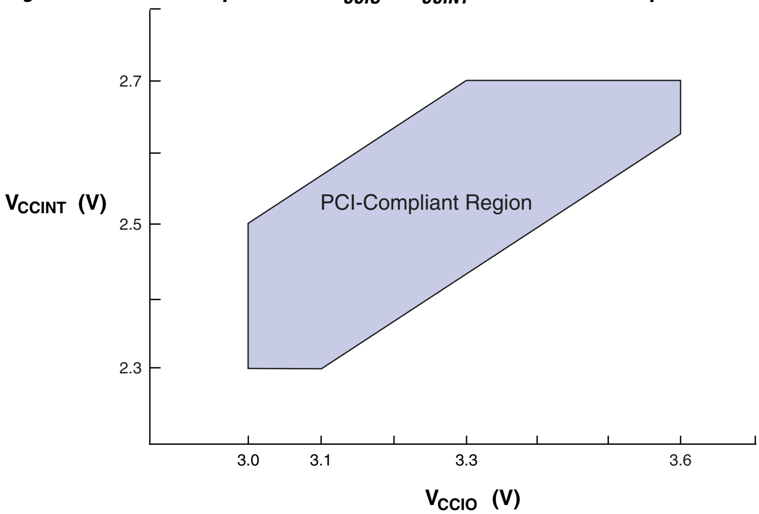
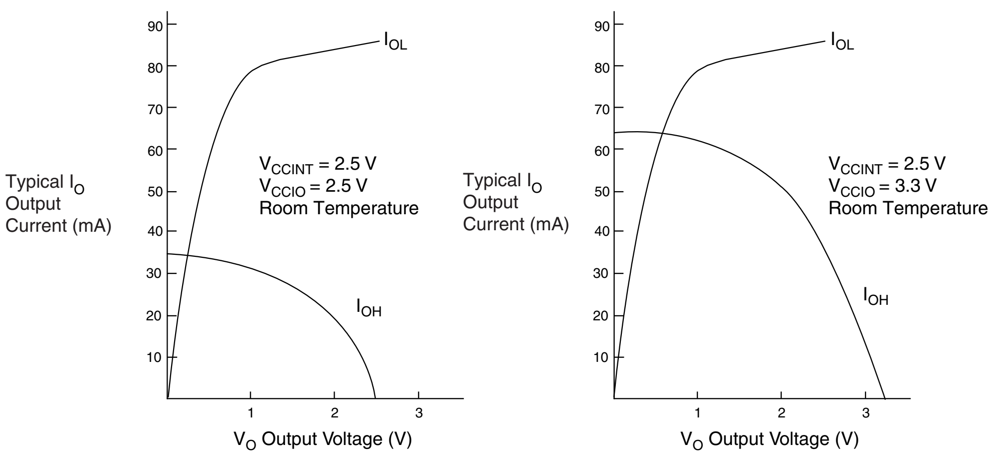


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when VCCIO pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

Figure 34. Output Drive Characteristics of APEX 20K Device *Note (1)*



Note to Figure 34:
(1) These are transient (AC) currents.

Figure 37. APEX 20KE f_{MAX} Timing Model

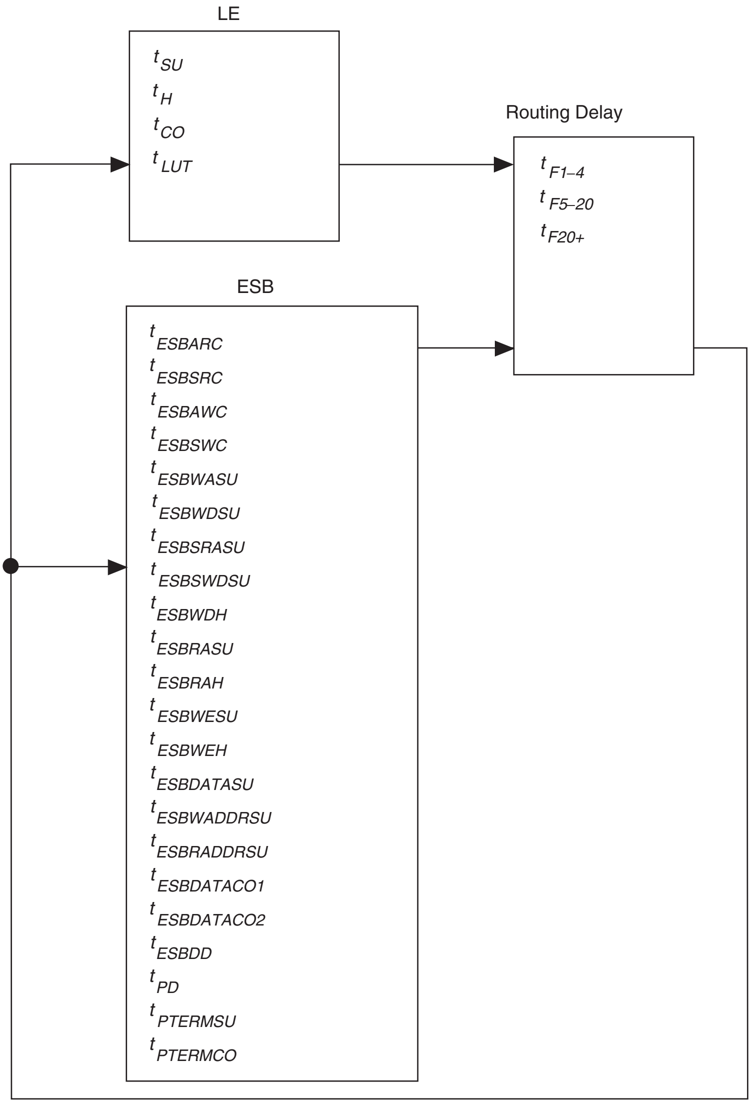


Table 31. APEX 20K f_{MAX} Timing Parameters (Part 2 of 2)

Symbol	Parameter
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
t_{F1-4}	Fanout delay using local interconnect
t_{F5-20}	Fanout delay using MegaLab Interconnect
t_{F20+}	Fanout delay using FastTrack Interconnect
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

Table 32. APEX 20K External Timing Parameters Note (1)

Symbol	Clock Parameter
t_{INSU}	Setup time with global clock at IOE register
t_{INH}	Hold time with global clock at IOE register
t_{OUTCO}	Clock-to-output delay with global clock at IOE register

Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF

Table 46. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(1)*	1.9		2.3		2.6		ns
$t_{INHBIDIR}$ *(1)*	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ *(1)*	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{XZBIDIR}$ *(1)*		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ *(1)*		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ *(2)*	1.1		1.2		–		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(2)*	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ *(2)*		4.3		5.0		–	ns
$t_{ZXBIDIR}$ *(2)*		4.3		5.0		–	ns

Table 47. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} *(1)*	1.4		1.8		2.0		ns
t_{INH} *(1)*	0.0		0.0		0.0		ns
t_{OUTCO} *(1)*	2.0	4.9	2.0	6.1	2.0	7.0	ns
t_{INSU} *(2)*	0.4		1.0		–		ns
t_{INH} *(2)*	0.0		0.0		–		ns
t_{OUTCO} *(2)*	0.5	3.1	0.5	4.1	–	–	ns

Table 48. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(1)*	1.4		1.8		2.0		ns
$t_{INHBIDIR}$ *(1)*	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ *(1)*	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{XZBIDIR}$ *(1)*		7.3		8.9		10.3	ns
$t_{ZXBIDIR}$ *(1)*		7.3		8.9		10.3	ns
$t_{INSUBIDIR}$ *(2)*	0.5		1.0		–		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(2)*	0.5	3.1	0.5	4.1	–	–	ns
$t_{XZBIDIR}$ *(2)*		6.2		7.6		–	ns
$t_{ZXBIDIR}$ *(2)*		6.2		7.6		–	ns

Table 52. EP20K30E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	0.55		0.78		1.15		ns
t_{CL}	0.55		0.78		1.15		ns
t_{CLRP}	0.22		0.31		0.46		ns
t_{PREP}	0.22		0.31		0.46		ns
t_{ESBCH}	0.55		0.78		1.15		ns
t_{ESBCL}	0.55		0.78		1.15		ns
t_{ESBWP}	1.43		2.01		2.97		ns
t_{ESBRP}	1.15		1.62		2.39		ns

Table 53. EP20K30E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.02		2.13		2.24		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{INSUPLL}$	2.11		2.23		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.88	-	-	ns

Table 54. EP20K30E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.85		1.77		1.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{XZBIDIR}$		7.48		8.46		9.83	ns
$t_{ZXBIDIR}$		7.48		8.46		9.83	ns
$t_{INSUBIDIRPLL}$	4.12		4.24		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.60	0.50	2.88	-	-	ns
$t_{XZBIDIRPLL}$		5.21		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.21		5.99		-	ns

Table 57. EP20K60E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.26		0.30	ns
t_{F5-20}		1.45		1.58		1.79	ns
t_{F20+}		1.96		2.14		2.45	ns

Table 58. EP20K60E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.00		2.50		2.75		ns
t_{CL}	2.00		2.50		2.75		ns
t_{CLRP}	0.20		0.28		0.41		ns
t_{PREP}	0.20		0.28		0.41		ns
t_{ESBCH}	2.00		2.50		2.75		ns
t_{ESBCL}	2.00		2.50		2.75		ns
t_{ESBWP}	1.29		1.80		2.66		ns
t_{ESBRP}	1.04		1.45		2.14		ns

Table 59. EP20K60E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.03		2.12		2.23		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

Table 87. EP20K400E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.25		0.26	ns
t_{F5-20}		1.01		1.12		1.25	ns
t_{F20+}		3.71		3.92		4.17	ns

Table 88. EP20K400E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.22		2.35		ns
t_{CL}	1.36		2.26		2.35		ns
t_{CLRP}	0.18		0.18		0.19		ns
t_{PREP}	0.18		0.18		0.19		ns
t_{ESBCH}	1.36		2.26		2.35		ns
t_{ESBCL}	1.36		2.26		2.35		ns
t_{ESBWP}	1.17		1.38		1.56		ns
t_{ESBRP}	0.94		1.09		1.25		ns

Table 89. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.51		2.64		2.77		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

Tables 97 through 102 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

Table 97. EP20K1000E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.32		0.33	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 104. EP20K1500E f_{MAX} ESB Timing Microparameters							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 105. EP20K1500E f_{MAX} Routing Delays							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.28		0.28		0.28	ns
t_{F5-20}		1.36		1.50		1.62	ns
t_{F20+}		4.43		4.48		5.07	ns

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 107. EP20K1500E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.09		3.30		3.58		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{INSUPLL}$	1.94		2.08		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.67	0.50	2.99	-	-	ns

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