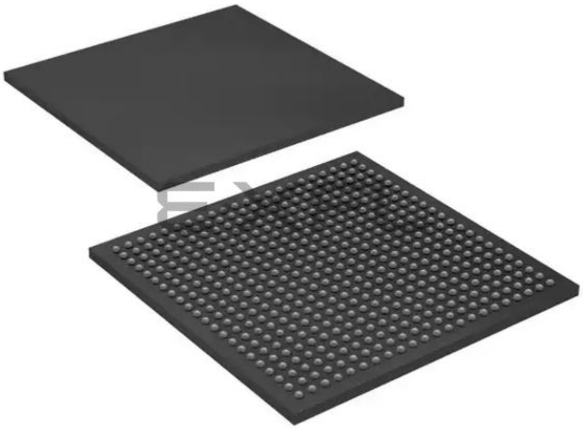
# Intel - EP20K200FC484-2XN Datasheet



**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 832 |
| Number of Logic Elements/Cells | 8320 |
| Total RAM Bits | 106496 |
| Number of I/O | 382 |
| Number of Gates | 526000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k200fc484-2xn |

*Table 2. Additional APEX 20K Device Features* *Note (1)*

| Feature | EP20K300E | EP20K400 | EP20K400E | EP20K600E | EP20K1000E | EP20K1500E |
|---|---|---|---|---|---|---|
| Maximum system gates | 728,000 | 1,052,000 | 1,052,000 | 1,537,000 | 1,772,000 | 2,392,000 |
| Typical gates | 300,000 | 400,000 | 400,000 | 600,000 | 1,000,000 | 1,500,000 |
| LEs | 11,520 | 16,640 | 16,640 | 24,320 | 38,400 | 51,840 |
| ESBs | 72 | 104 | 104 | 152 | 160 | 216 |
| Maximum RAM bits | 147,456 | 212,992 | 212,992 | 311,296 | 327,680 | 442,368 |
| Maximum macrocells | 1,152 | 1,664 | 1,664 | 2,432 | 2,560 | 3,456 |
| Maximum user I/O pins | 408 | 502 | 488 | 588 | 708 | 808 |

*Note to Tables 1 and 2:*

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

*Table 3. APEX 20K Supply Voltages*

| Feature | Device | |
|---|---|---|
| | EP20K100<br>EP20K200<br>EP20K400 | EP20K30E<br>EP20K60E<br>EP20K100E<br>EP20K160E<br>EP20K200E<br>EP20K300E<br>EP20K400E<br>EP20K600E<br>EP20K1000E<br>EP20K1500E |
| Internal supply voltage ($V_{CCINT}$) | 2.5 V | 1.8 V |
| MultiVolt I/O interface voltage levels ($V_{CCIO}$) | 2.5 V, 3.3 V, 5.0 V | 1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)* |

*Note to Table 3:*

(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

*Table 8. Comparison of APEX 20K & APEX 20KE Features*

| Feature | APEX 20K Devices | APEX 20KE Devices |
|---|---|---|
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

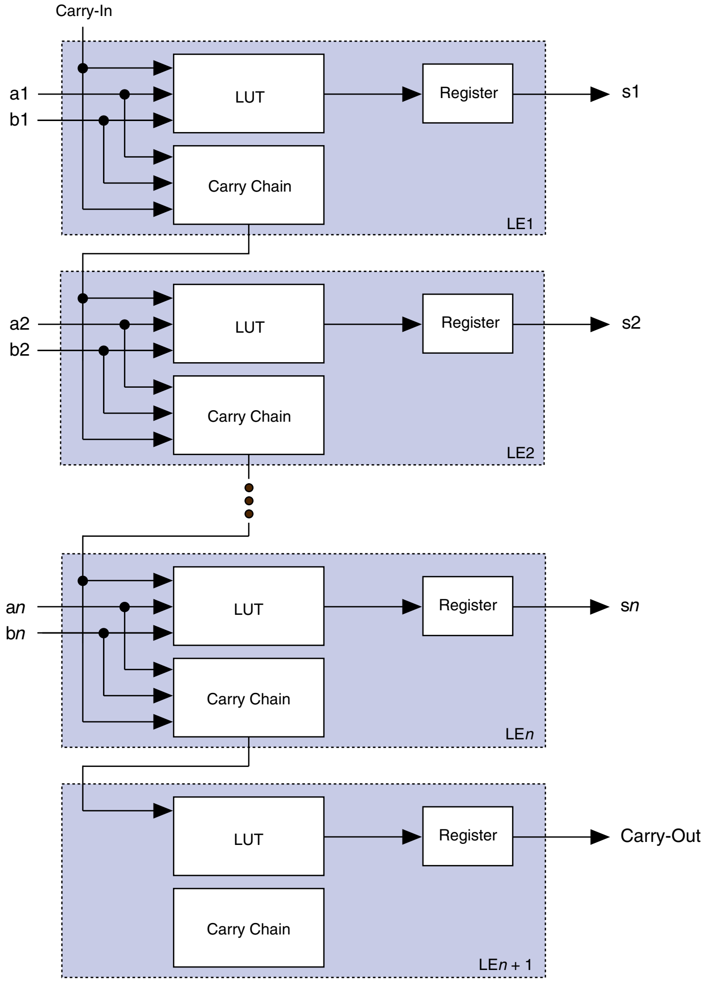
APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

*Figure 6. APEX 20K Carry Chain*



### *LE Operating Modes*

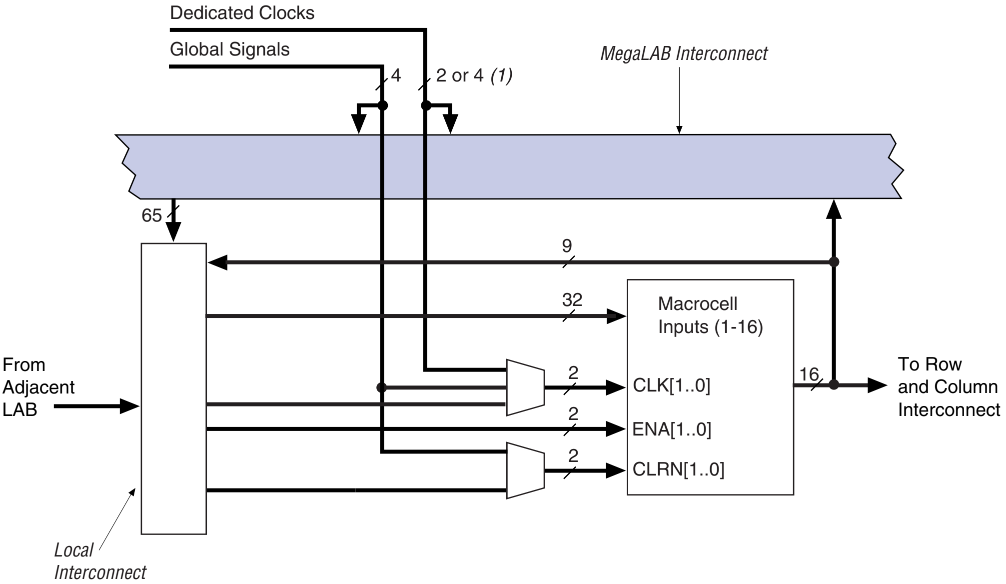
The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

**Figure 13. Product-Term Logic in ESB**



*Note to Figure 13:*
(1) APEX 20KE devices have four dedicated clocks.

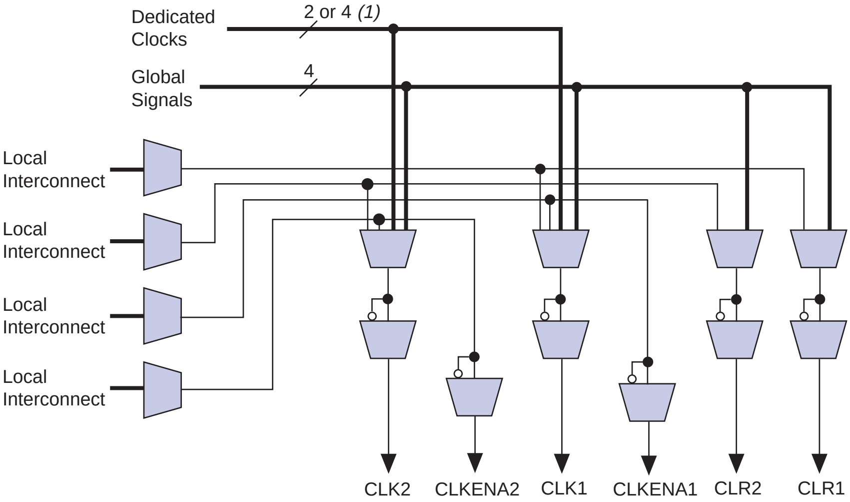
### Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide `OR` functions. The Quartus II software Compiler can use a `NOT`-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*



*Note to Figure 15:*

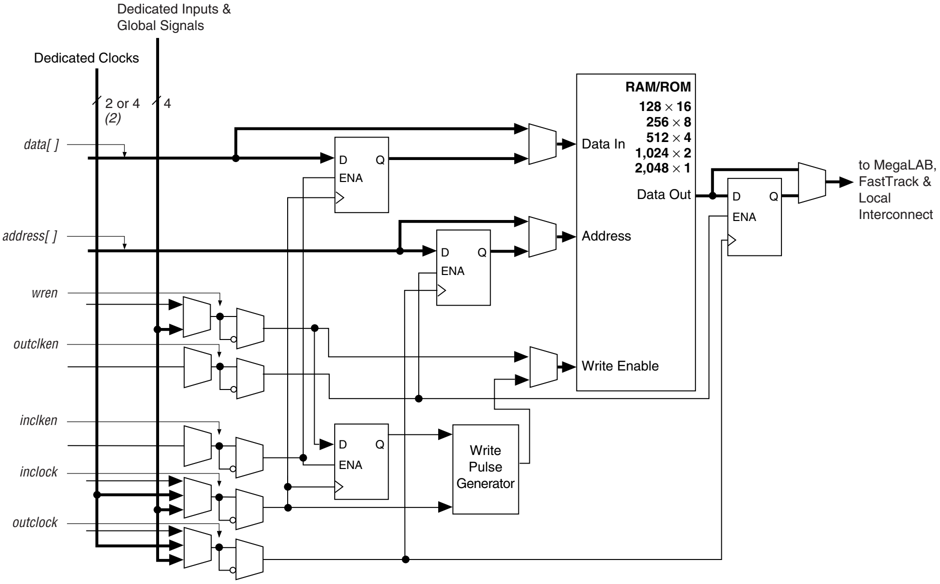
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell `OR` logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

*Figure 22. ESB in Single-Port Mode* *Note (1)*



*Notes to Figure 22:*

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

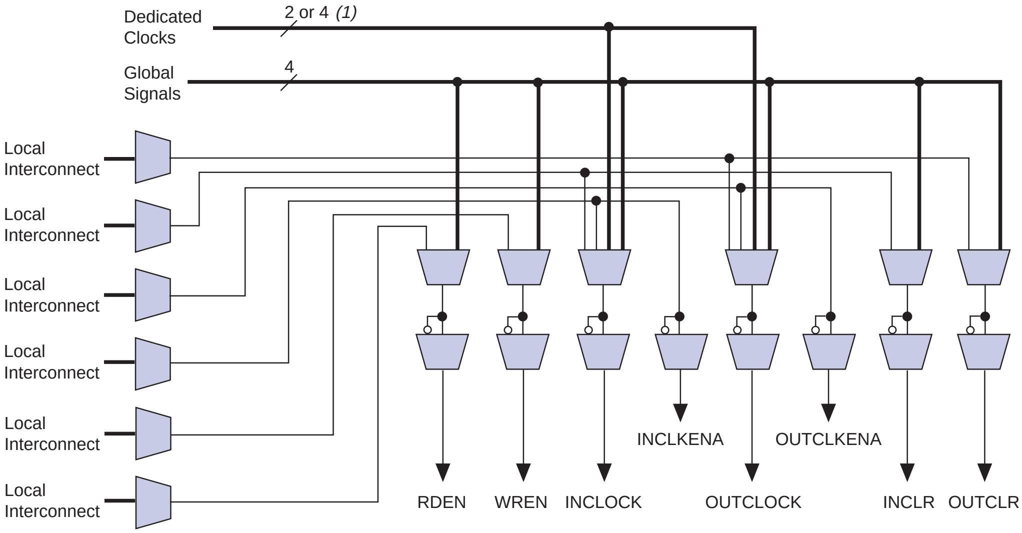
CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, `WE`, and `RE` signals. The global signals and the local interconnect can drive the `WE` and `RE` signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the `WE` and `RE` signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

*Figure 24. ESB Control Signal Generation*



*Note to Figure 24:*
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own `VCCIO` pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same `VCCIO` for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same `VCCIO` voltage level. For example, when `VCCIO` is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

*Table 22. APEX 20K JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | `TCK` clock period | 100 | | ns |
| $t_{JCH}$ | `TCK` clock high time | 50 | | ns |
| $t_{JCL}$ | `TCK` clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

**Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions** *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4)*, *(5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4)*, *(5)* | 3.00 (3.00) | 3.60 (3.60) | V |
|  | Supply voltage for output buffers, 2.5-V operation | *(4)*, *(5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3)*, *(6)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage |  | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
|  |  | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time |  |  | 40 | ns |
| $t_F$ | Input fall time |  |  | 40 | ns |

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)** *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage |  | 1.7, 0.5 × $V_{CCIO}$ *(9)* |  | 5.75 | V |
| $V_{IL}$ | Low-level input voltage |  | –0.5 |  | 0.8, 0.3 × $V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 |  |  | V |
|  | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | $V_{CCIO}$ – 0.2 |  |  | V |
|  | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | 0.9 × $V_{CCIO}$ |  |  | V |
|  | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.1 |  |  | V |
|  |  | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.0 |  |  | V |
|  |  | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 1.7 |  |  | V |

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)** *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC,<br>$V_{CCIO}$ = 3.00 V *(11)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC,<br>$V_{CCIO}$ = 3.00 V *(11)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC,<br>$V_{CCIO}$ = 3.00 to 3.60 V *(11)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC,<br>$V_{CCIO}$ = 2.30 V *(11)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC,<br>$V_{CCIO}$ = 2.30 V *(11)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC,<br>$V_{CCIO}$ = 2.30 V *(11)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade *(12)* | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades *(12)* | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | W |
| | | $V_{CCIO}$ = 2.375 V *(13)* | 30 | | 80 | W |

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

**Table 30. APEX 20KE Device Capacitance** *Note (15)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 27 through 30:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Numbers in parentheses are for industrial-temperature-range devices.

(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.

(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

| Vin | Max. Duty Cycle |
|---|---|
| 4.0V | 100% (DC) |
| 4.1 | 90% |
| 4.2 | 50% |
| 4.3 | 30% |
| 4.4 | 17% |
| 4.5 | 10% |

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.

(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.

(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.

(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, and $I_I$ parameters when VCCIO = 1.8 V.

(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.

(11) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.

(12) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.

(13) This value is specified for normal device operation. The value may vary during power-up.

(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.

(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.

**Table 36. APEX 20KE Routing Timing Microparameters** *Note (1)*

| Symbol | Parameter |
|---|---|
| $t_{F1-4}$ | Fanout delay using Local Interconnect |
| $t_{F5-20}$ | Fanout delay estimate using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay estimate using FastTrack Interconnect |

*Note to Table 36:*

(1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

**Table 37. APEX 20KE Functional Timing Microparameters**

| Symbol | Parameter |
|---|---|
| TCH | Minimum clock high time from clock pin |
| TCL | Minimum clock low time from clock pin |
| TCLRP | LE clear Pulse Width |
| TPREP | LE preset pulse width |
| TESBCH | Clock high time for ESB |
| TESBCL | Clock low time for ESB |
| TESBWP | Write pulse width |
| TESBRP | Read pulse width |

Tables 38 and 39 describe the APEX 20KE external timing parameters.

**Table 38. APEX 20KE External Timing Parameters** *Note (1)*

| Symbol | Clock Parameter | Conditions |
|---|---|---|
| $t_{INSU}$ | Setup time with global clock at IOE input register | |
| $t_{INH}$ | Hold time with global clock at IOE input register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE output register | C1 = 10 pF |
| $t_{INSUPLL}$ | Setup time with PLL clock at IOE input register | |
| $t_{INHPLL}$ | Hold time with PLL clock at IOE input register | |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register | C1 = 10 pF |

*Table 39. APEX 20KE External Bidirectional Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous Output Enable Register to output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous Output Enable Register output buffer enable delay | C1 = 10 pF |
| $t_{INSUBIDIRPLL}$ | Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{INHBIDIRPLL}$ | Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIRPLL}$ | Clock-to-output delay for bidirectional pins with PLL clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIRPLL}$ | Synchronous Output Enable Register to output buffer disable delay with PLL | C1 = 10 pF |
| $t_{ZXBIDIRPLL}$ | Synchronous Output Enable Register output buffer enable delay with PLL | C1 = 10 pF |

*Note to Tables 38 and 39:*

(1) These timing parameters are sample-tested only.

Tables 67 through 72 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

*Table 67. EP20K160E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_H$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.25 | | 0.31 | | 0.35 | ns |
| $t_{LUT}$ | | 0.69 | | 0.88 | | 1.12 | ns |

***Table 86. EP20K400E $f_{MAX}$ ESB Timing Microparameters***

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 1.91 | | 1.99 | ns |
| $t_{ESBSRC}$ | | 2.30 | | 2.66 | | 2.93 | ns |
| $t_{ESBAWC}$ | | 3.09 | | 3.58 | | 3.99 | ns |
| $t_{ESBSWC}$ | | 3.01 | | 3.65 | | 4.05 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.63 | | 0.65 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.77 | | 0.84 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.77 | | 1.86 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.35 | | 1.47 | | 1.61 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.18 | | -0.30 | | -0.27 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | -0.02 | | -0.11 | | -0.03 | | ns |
| $t_{ESBRADDRSU}$ | 0.06 | | -0.01 | | -0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.16 | | 1.40 | | 1.54 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 2.55 | | 2.85 | ns |
| $t_{ESBDD}$ | | 2.73 | | 3.17 | | 3.58 | ns |
| $t_{PD}$ | | 1.57 | | 1.83 | | 2.07 | ns |
| $t_{PTERMSU}$ | 0.92 | | 0.99 | | 1.18 | | ns |
| $t_{PTERMCO}$ | | 1.18 | | 1.43 | | 1.17 | ns |

*Table 110. Selectable I/O Standard Output Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.09 | | 0.10 | ns |
| 1.8 V | | 2.49 | | 2.98 | | 3.03 | ns |
| PCI | | –0.03 | | 0.17 | | 0.16 | ns |
| GTL+ | | 0.75 | | 0.75 | | 0.76 | ns |
| SSTL-3 Class I | | 1.39 | | 1.51 | | 1.50 | ns |
| SSTL-3 Class II | | 1.11 | | 1.23 | | 1.23 | ns |
| SSTL-2 Class I | | 1.35 | | 1.48 | | 1.47 | ns |
| SSTL-2 Class II | | 1.00 | | 1.12 | | 1.12 | ns |
| LVDS | | –0.48 | | –0.48 | | –0.48 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

## Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

## Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to $V_{CCIO}$ by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (`nCE`) and configuration enable output (`nCEO`) pins on each device.

*Table 111. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, EPC16 configuration devices |
| Passive serial (PS) | MasterBlaster or ByteBlasterMV download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File |

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

## Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information