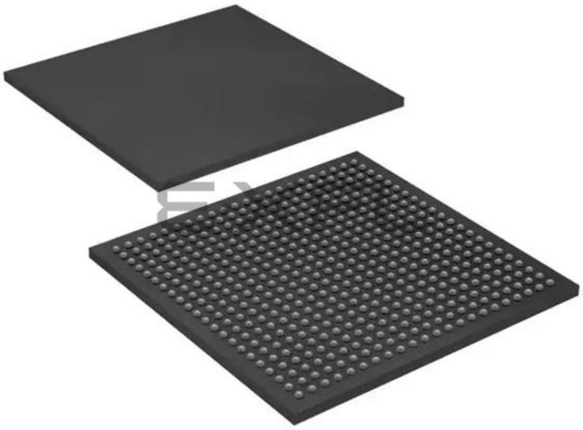

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 832 |
| Number of Logic Elements/Cells | 8320 |
| Total RAM Bits | 106496 |
| Number of I/O | 382 |
| Number of Gates | 526000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k200fc484-2xv |

| Table 8. Comparison of APEX 20K & APEX 20KE Features | | |
|---|---|---|
| **Feature** | **APEX 20K Devices** | **APEX 20KE Devices** |
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

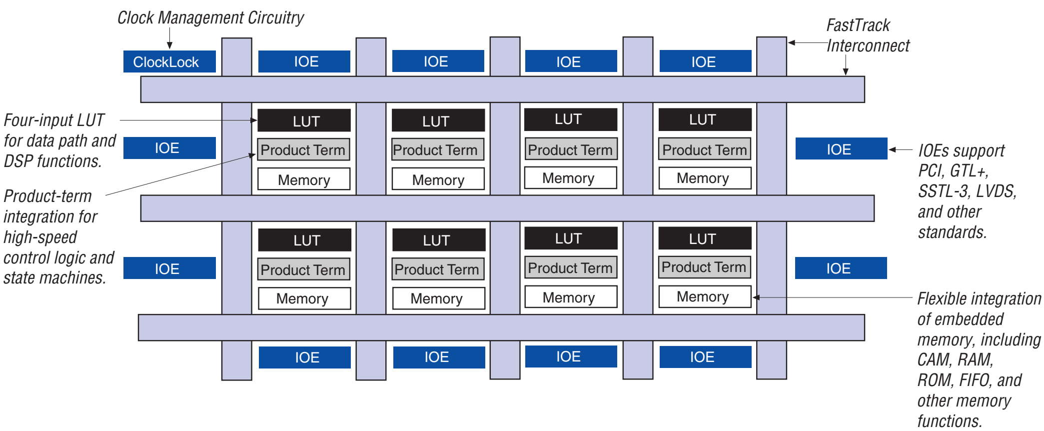
# Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

**Figure 1. APEX 20K Device Block Diagram**



Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

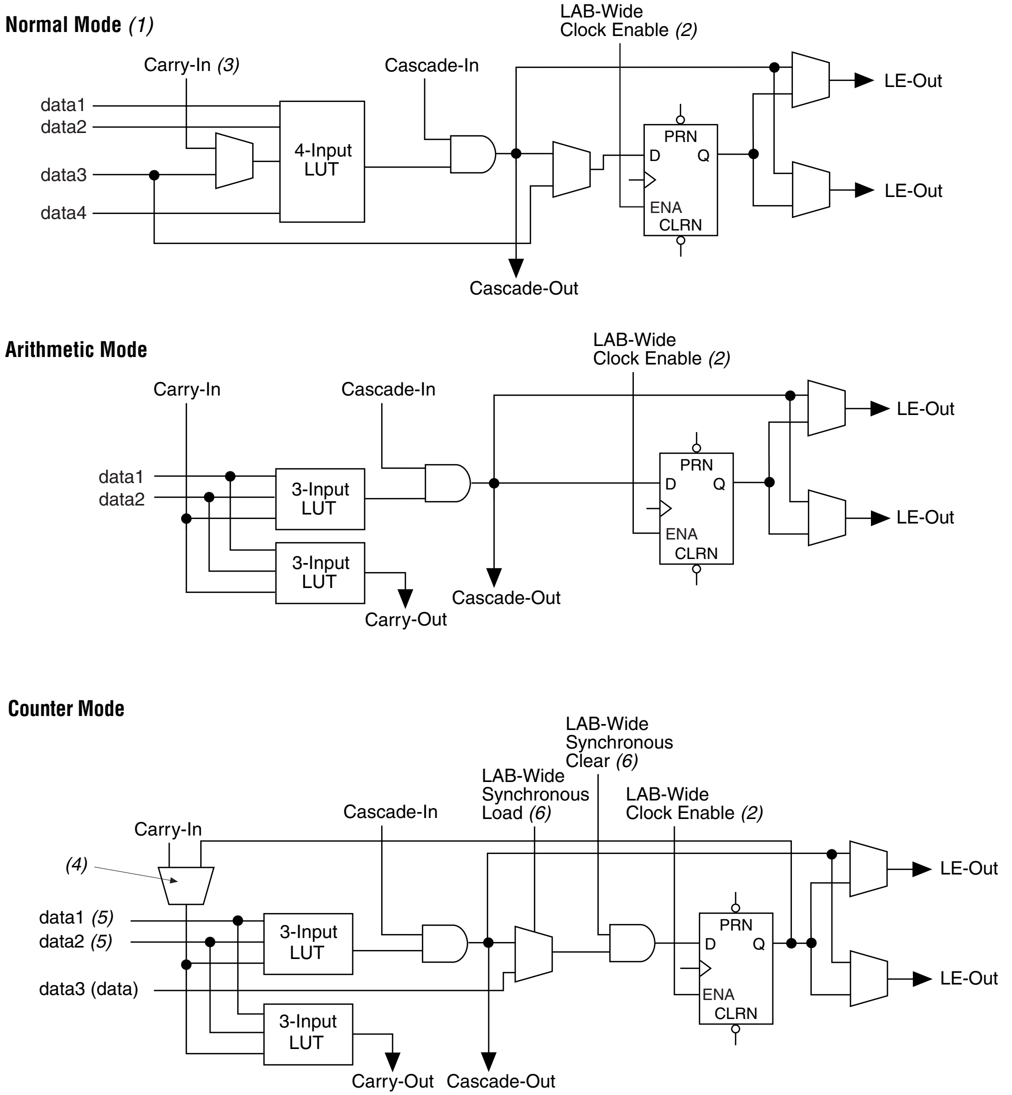
### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an $n$-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

*Figure 8. APEX 20K LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another `AND` gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a `NOT`-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable `NOT`-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

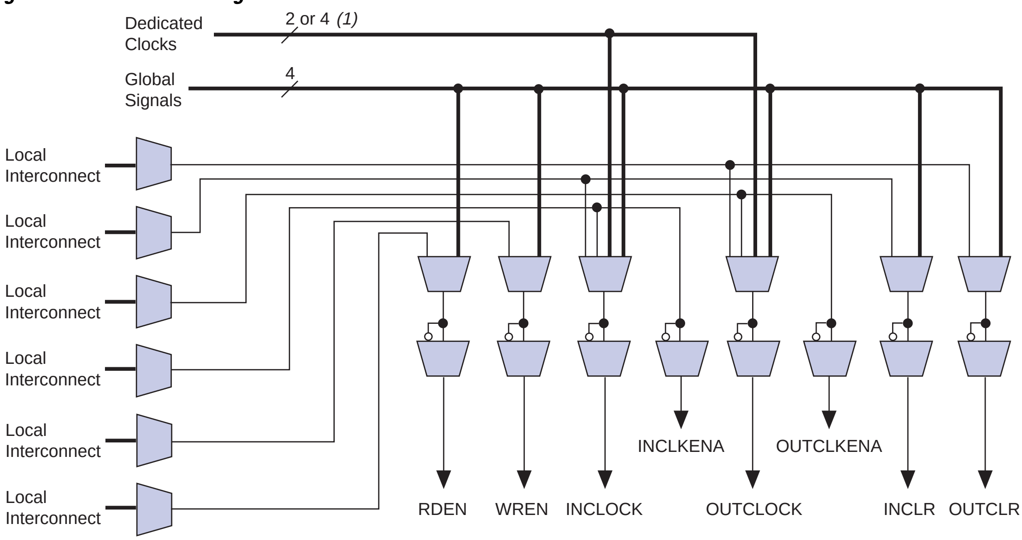
The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, `WE`, and `RE` signals. The global signals and the local interconnect can drive the `WE` and `RE` signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the `WE` and `RE` signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

***Figure 24. ESB Control Signal Generation***

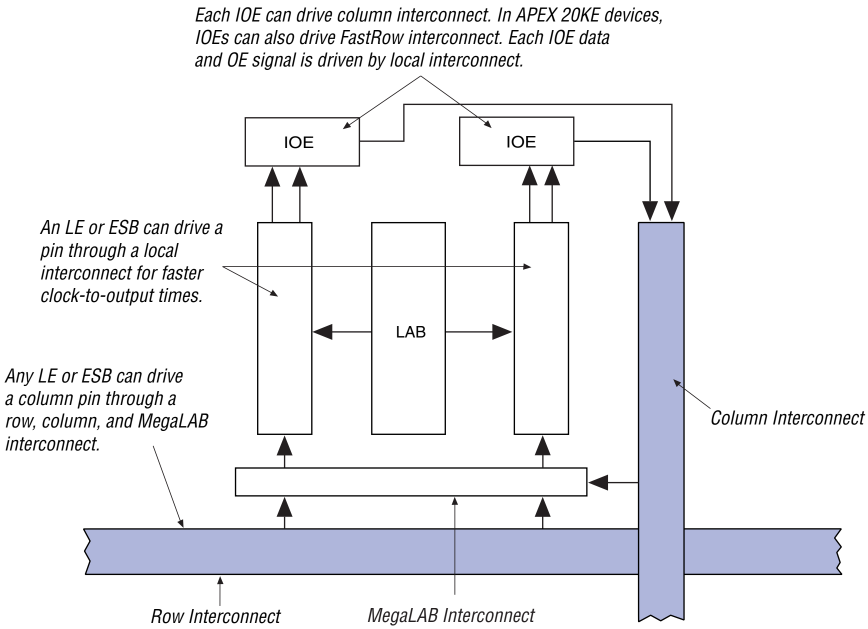



*Note to Figure 24:*
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Figure 28 shows how a column IOE connects to the interconnect.

*Figure 28. Column IOE Connection to the Interconnect*




## Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own `VCCIO` pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same `VCCIO` for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same `VCCIO` voltage level. For example, when `VCCIO` is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

## MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of `VCC` pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The APEX 20K `VCCINT` pins must always be connected to a 2.5 V power supply. With a 2.5-V $V_{CCINT}$ level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The `VCCIO` pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

**Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support**

| $V_{CCIO}$ (V) | Input Signals (V) | | | Output Signals (V) | | |
|---|---|---|---|---|---|---|
| | 2.5 | 3.3 | 5.0 | 2.5 | 3.3 | 5.0 |
| 2.5 | ✓ | ✓ *(1)* | ✓ *(1)* | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ *(1)* | ✓ *(2)* | ✓ | ✓ |

***Notes to Table 12:***

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$.

(2) When $V_{CCIO}$ = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

**Table 13. APEX 20KE MultiVolt I/O Support** *Note (1)*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | *(2)* | | | ✓*(3)* | |

*Notes to Table 13:*
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.
(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.
(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

| Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2) | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $t_{SKEW}$ | Skew delay between related ClockLock/ClockBoost-generated clocks | | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ClockBoost-generated clock *(5)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

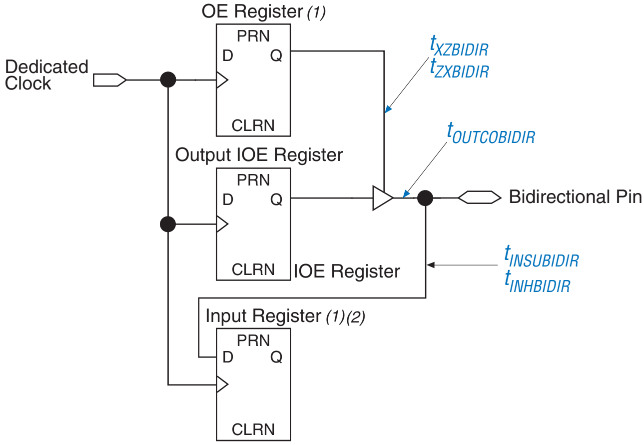
*Notes to Table 15:*

(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, $t_{JITTER}$ is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

| Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $f_{OUT}$ | Output frequency | 25 | 170 | MHz |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 170 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 80 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 34 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)* | | 25,000 *(2)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ ClockBoost to acquire lock *(3)* | | 10 | µs |
| $t_{SKEW}$ | Skew delay between related ClockLock/ ClockBoost-generated clock | 500 | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ ClockBoost-generated clock *(4)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

*Figure 40. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 40:*

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the $f_{MAX}$ timing parameters shown in Figure 36 on page 68.

*Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 1 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{ESBRC}$ | ESB Asynchronous read cycle time |
| $t_{ESBWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |

*Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 2 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB macrocell register clock-to-output delay |
| $t_{F1-4}$ | Fanout delay using local interconnect |
| $t_{F5-20}$ | Fanout delay using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay using FastTrack Interconnect |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 32 and 33 describe APEX 20K external timing parameters.

*Table 32. APEX 20K External Timing Parameters Note (1)*

| Symbol | Clock Parameter |
|---|---|
| $t_{INSU}$ | Setup time with global clock at IOE register |
| $t_{INH}$ | Hold time with global clock at IOE register |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register |

*Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | C1 = 10 pF |

| *Table 41. EP20K200 $f_{MAX}$ Timing Parameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1 Speed Grade** | | **-2 Speed Grade** | | **-3 Speed Grade** | | **Units** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.7 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

Table 51. EP20K30E $f_{MAX}$ Routing Delays

Tables 55 through 60 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

**Table 55. EP20K60E $f_{MAX}$ LE Timing Microparameters**

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.17 | | 0.15 | | 0.16 | | ns |
| $t_H$ | 0.32 | | 0.33 | | 0.39 | | ns |
| $t_{CO}$ | | 0.29 | | 0.40 | | 0.60 | ns |
| $t_{LUT}$ | | 0.77 | | 1.07 | | 1.59 | ns |

*Table 74. EP20K200E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.68 | | 2.06 | | 2.24 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 2.77 | | 3.18 | ns |
| $t_{ESBAWC}$ | | 3.10 | | 3.86 | | 4.50 | ns |
| $t_{ESBSWC}$ | | 2.90 | | 3.67 | | 4.21 | ns |
| $t_{ESBWASU}$ | 0.55 | | 0.67 | | 0.74 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.83 | | 0.95 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.90 | | 2.09 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.42 | | 1.71 | | 2.01 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.06 | | -0.07 | | 0.05 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.13 | | 0.31 | | ns |
| $t_{ESBRADDRSU}$ | 0.18 | | 0.23 | | 0.39 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.35 | | 1.51 | ns |
| $t_{ESBDATACO2}$ | | 2.19 | | 2.75 | | 3.22 | ns |
| $t_{ESBDD}$ | | 2.75 | | 3.41 | | 4.03 | ns |
| $t_{PD}$ | | 1.58 | | 1.97 | | 2.33 | ns |
| $t_{PTERMSU}$ | 1.00 | | 1.22 | | 1.51 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.37 | | 1.09 | ns |

*Table 75. EP20K200E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.02 | | 1.20 | | 1.41 | ns |
| $t_{F20+}$ | | 1.99 | | 2.23 | | 2.53 | ns |

*Table 86. EP20K400E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 1.91 | | 1.99 | ns |
| $t_{ESBSRC}$ | | 2.30 | | 2.66 | | 2.93 | ns |
| $t_{ESBAWC}$ | | 3.09 | | 3.58 | | 3.99 | ns |
| $t_{ESBSWC}$ | | 3.01 | | 3.65 | | 4.05 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.63 | | 0.65 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.77 | | 0.84 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.77 | | 1.86 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.35 | | 1.47 | | 1.61 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.18 | | -0.30 | | -0.27 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | -0.02 | | -0.11 | | -0.03 | | ns |
| $t_{ESBRADDRSU}$ | 0.06 | | -0.01 | | -0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.16 | | 1.40 | | 1.54 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 2.55 | | 2.85 | ns |
| $t_{ESBDD}$ | | 2.73 | | 3.17 | | 3.58 | ns |
| $t_{PD}$ | | 1.57 | | 1.83 | | 2.07 | ns |
| $t_{PTERMSU}$ | 0.92 | | 0.99 | | 1.18 | | ns |
| $t_{PTERMCO}$ | | 1.18 | | 1.43 | | 1.17 | ns |

Tables 97 through 102 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

**Table 97. EP20K1000E $f_{MAX}$ LE Timing Microparameters**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_H$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

| Table 99. EP20K1000E $f_{MAX}$ Routing Delays | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.27 | | 0.27 | | 0.27 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.63 | | 1.75 | ns |
| $t_{F20+}$ | | 4.15 | | 4.33 | | 4.97 | ns |

| Table 100. EP20K1000E Minimum Pulse Width Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

| Table 101. EP20K1000E External Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.70 | | 2.84 | | 2.97 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{INSUPLL}$ | 1.64 | | 2.09 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | - | - | ns |