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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	-
Number of Gates	526000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k200fc672-3">https://www.e-xfl.com/product-detail/intel/ep20k200fc672-3</a>

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 12. APEX 20KE FastRow Interconnect

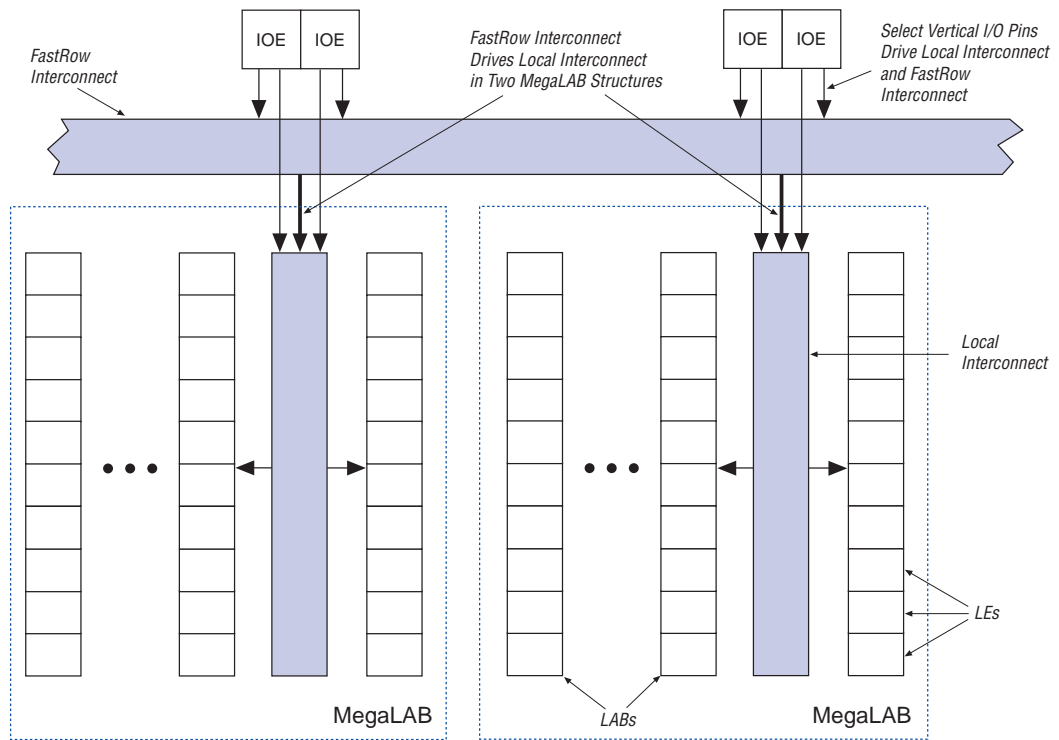


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

## Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

## Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

## MultiVolt I/O Interface

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V VCCINT level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

<b>Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support</b>						
<b>V<sub>CCIO</sub> (V)</b>	<b>Input Signals (V)</b>			<b>Output Signals (V)</b>		
	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

**Notes to Table 12:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V<sub>CCIO</sub>.
- (2) When V<sub>CCIO</sub> = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V<sub>IH</sub> of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I<sub>OL</sub> current specification should be considered when selecting a pull-up resistor.

**Notes to Table 16:**

- (1) To implement the ClockLock and ClockBoost circuitry with the Quartus II software, designers must specify the input frequency. The Quartus II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The  $f_{CLKDEV}$  parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the  $t_{LOCK}$  value is less than the time required for configuration.
- (4) The  $t_{JITTER}$  specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

<b>Table 17. APEX 20KE ClockLock &amp; ClockBoost Parameters</b> <i>Note (1)</i>						
<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
$t_R$	Input rise time				5	ns
$t_F$	Input fall time				5	ns
$t_{INDUTY}$	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	peak-to-peak
$t_{OUTJITTER}$	Jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	RMS
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
$t_{LOCK}$ (2), (3)	Time required for ClockLock or ClockBoost to acquire lock				40	μs





For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

**Table 30. APEX 20KE Device Capacitance** Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 27 through 30:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than  $100\text{ mA}$ . The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to  $100\%$  duty cycle.

$V_{IN}$	Max. Duty Cycle
$4.0\text{ V}$	$100\%$ (DC)
$4.1$	$90\%$
$4.2$	$50\%$
$4.3$	$30\%$
$4.4$	$17\%$
$4.5$	$10\%$
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 1.8\text{ V}$ , and  $V_{CCIO} = 1.8\text{ V}$ ,  $2.5\text{ V}$  or  $3.3\text{ V}$ .
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ , and  $I_I$  parameters when  $V_{CCIO} = 1.8\text{ V}$ .
- (10) The APEX 20KE input buffers are compatible with  $1.8\text{-V}$ ,  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVCMOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for  $3.3\text{-V}$  PCI compliance on APEX 20K devices.

Figure 33. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

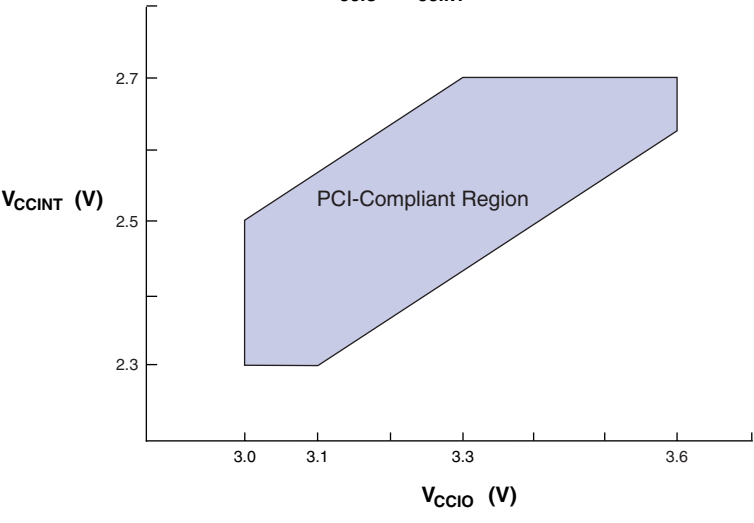
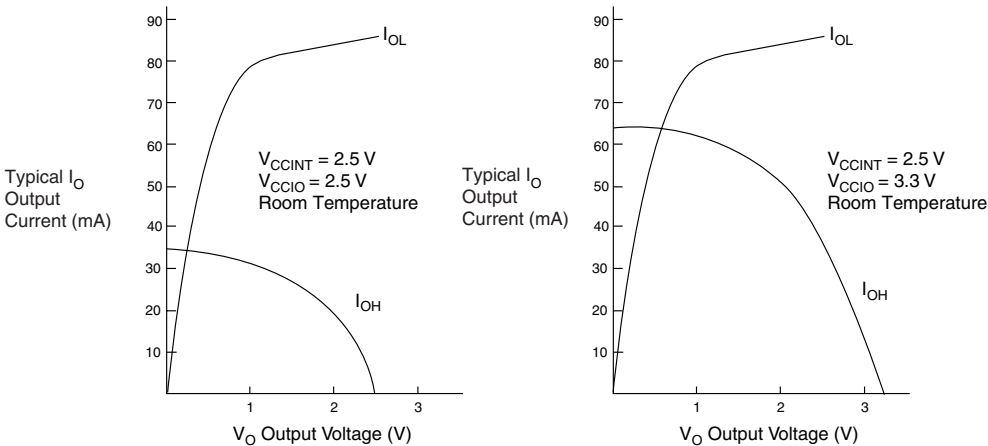


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when  $V_{CCIO}$  pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

Figure 34. Output Drive Characteristics of APEX 20K Device *Note (1)*



Note to Figure 34:

(1) These are transient (AC) currents.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the  $f_{MAX}$  timing model for APEX 20K devices.

**Figure 36. APEX 20K  $t_{MAX}$  Timing Model**

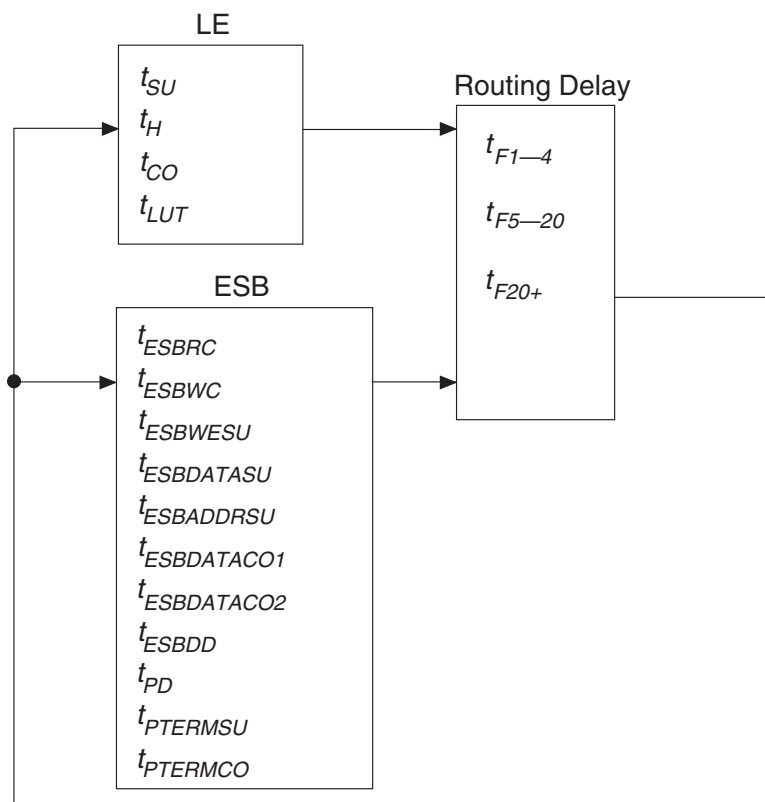
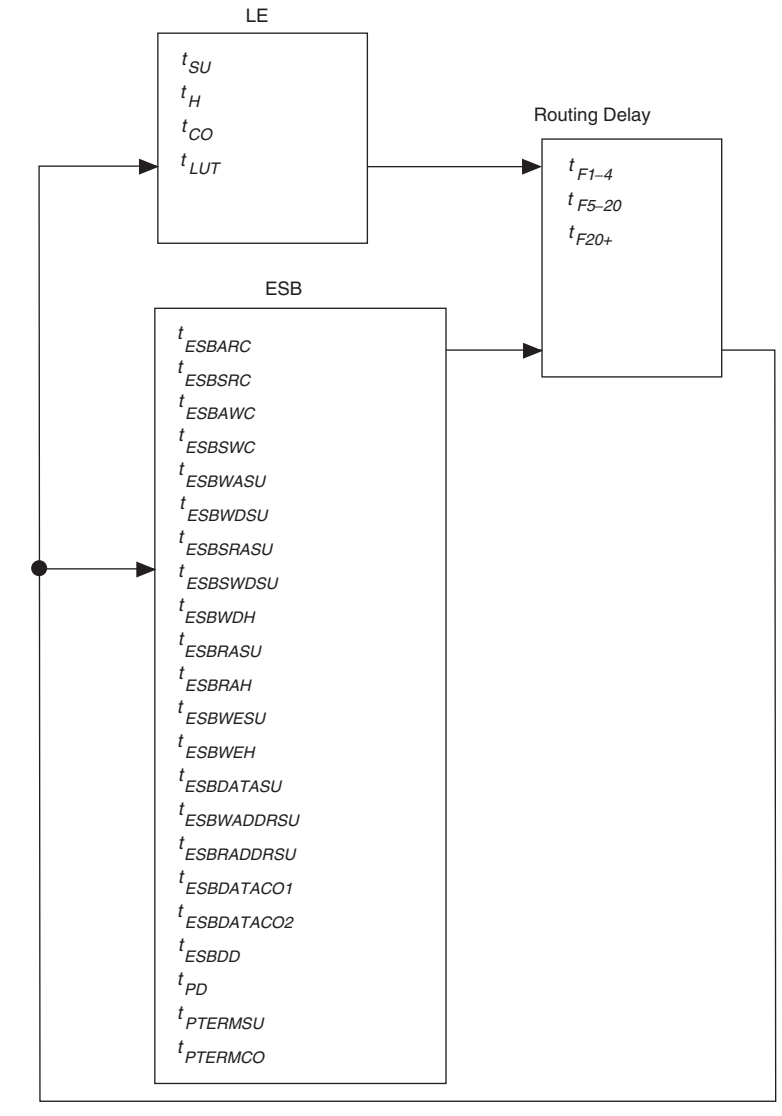


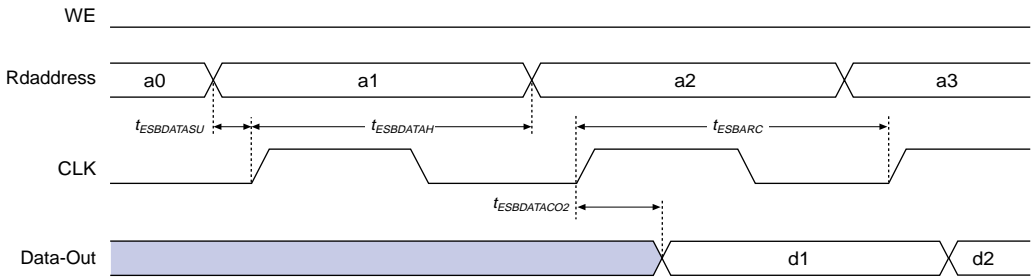
Figure 37 shows the  $f_{MAX}$  timing model for APEX 20KE devices. These parameters can be used to estimate  $f_{MAX}$  for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Figure 37. APEX 20KE  $t_{MAX}$  Timing Model



**Figure 39. ESB Synchronous Timing Waveforms**

**ESB Synchronous Read**



**ESB Synchronous Write (ESB Output Registers Used)**

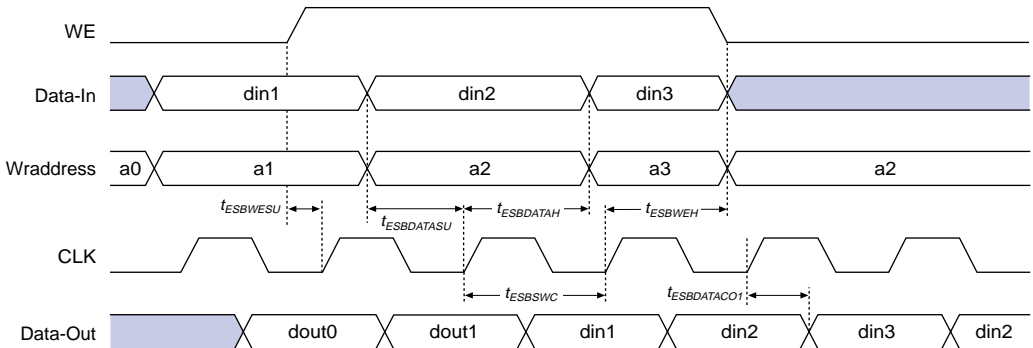


Figure 40 shows the timing model for bidirectional I/O pin timing.

**Table 36. APEX 20KE Routing Timing Microparameters** *Note (1)*

Symbol	Parameter
$t_{F1-4}$	Fanout delay using Local Interconnect
$t_{F5-20}$	Fanout delay estimate using MegaLab Interconnect
$t_{F20+}$	Fanout delay estimate using FastTrack Interconnect

*Note to Table 36:*

- (1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

**Table 37. APEX 20KE Functional Timing Microparameters**

Symbol	Parameter
TCH	Minimum clock high time from clock pin
TCL	Minimum clock low time from clock pin
TCLRP	LE clear Pulse Width
TPREP	LE preset pulse width
TESBCH	Clock high time for ESB
TESBCL	Clock low time for ESB
TESBWP	Write pulse width
TESBRP	Read pulse width

Tables 38 and 39 describe the APEX 20KE external timing parameters.

**Table 38. APEX 20KE External Timing Parameters** *Note (1)*

Symbol	Clock Parameter	Conditions
$t_{INSU}$	Setup time with global clock at IOE input register	
$t_{INH}$	Hold time with global clock at IOE input register	
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
$t_{INHPLL}$	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF

**Table 41. EP20K200  $f_{MAX}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.5		0.6		0.8		ns
$t_H$	0.7		0.8		1.0		ns
$t_{CO}$		0.3		0.4		0.5	ns
$t_{LUT}$		0.8		1.0		1.3	ns
$t_{ESBRC}$		1.7		2.1		2.4	ns
$t_{ESBWC}$		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
$t_{ESBDD}$		2.5		3.3		3.6	ns
$t_{PD}$		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
$t_{F1-4}$		0.5		0.6		0.7	ns
$t_{F5-20}$		1.6		1.7		1.8	ns
$t_{F20+}$		2.2		2.2		2.3	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns
$t_{CLRP}$	0.3		0.4		0.4		ns
$t_{PREP}$	0.4		0.5		0.5		ns
$t_{ESBCH}$	2.0		2.5		3.0		ns
$t_{ESBCL}$	2.0		2.5		3.0		ns
$t_{ESBWP}$	1.6		1.9		2.2		ns
$t_{ESBRP}$	1.0		1.3		1.4		ns

**Table 52. EP20K30E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	0.55		0.78		1.15		ns
t <sub>CL</sub>	0.55		0.78		1.15		ns
t <sub>CLRP</sub>	0.22		0.31		0.46		ns
t <sub>PREP</sub>	0.22		0.31		0.46		ns
t <sub>ESBCH</sub>	0.55		0.78		1.15		ns
t <sub>ESBCL</sub>	0.55		0.78		1.15		ns
t <sub>ESBWP</sub>	1.43		2.01		2.97		ns
t <sub>ESBRP</sub>	1.15		1.62		2.39		ns

**Table 53. EP20K30E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.02		2.13		2.24		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>INSUPLL</sub>	2.11		2.23		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns

**Table 54. EP20K30E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	1.85		1.77		1.54		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>XZBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>ZXBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>INSUBIDIRPLL</sub>	4.12		4.24		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns
t <sub>XZBIDIRPLL</sub>		5.21		5.99		-	ns
t <sub>ZXBIDIRPLL</sub>		5.21		5.99		-	ns



Tables 55 through 60 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

**Table 55. EP20K60E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.17		0.15		0.16		ns
$t_H$	0.32		0.33		0.39		ns
$t_{CO}$		0.29		0.40		0.60	ns
$t_{LUT}$		0.77		1.07		1.59	ns

**Table 57. EP20K60E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

Tables 67 through 72 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

**Table 67. EP20K160E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.22		0.24		0.26		ns
$t_H$	0.22		0.24		0.26		ns
$t_{CO}$		0.25		0.31		0.35	ns
$t_{LUT}$		0.69		0.88		1.12	ns

**Table 108. EP20K1500E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.47		3.68		3.99		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{\text{XZBIDIR}}$		6.91		7.62		8.38	ns
$t_{\text{ZXBIDIR}}$		6.91		7.62		8.38	ns
$t_{\text{INSUBIDIRPLL}}$	3.05		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.67	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		3.41		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

**Table 109. Selectable I/O Standard Input Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		-0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		-0.24		-0.23		-0.19	ns
SSTL-3 Class I		-0.32		-0.21		-0.47	ns
SSTL-3 Class II		-0.08		0.03		-0.23	ns
SSTL-2 Class I		-0.17		-0.06		-0.32	ns
SSTL-2 Class II		-0.16		-0.05		-0.31	ns
LVDS		-0.12		-0.12		-0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$  added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).