Altera - EP20K300EBC652-3 Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1152
Number of Logic Elements/Cells	11520
Total RAM Bits	147456
Number of I/O	408
Number of Gates	728000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k300ebc652-3

Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram

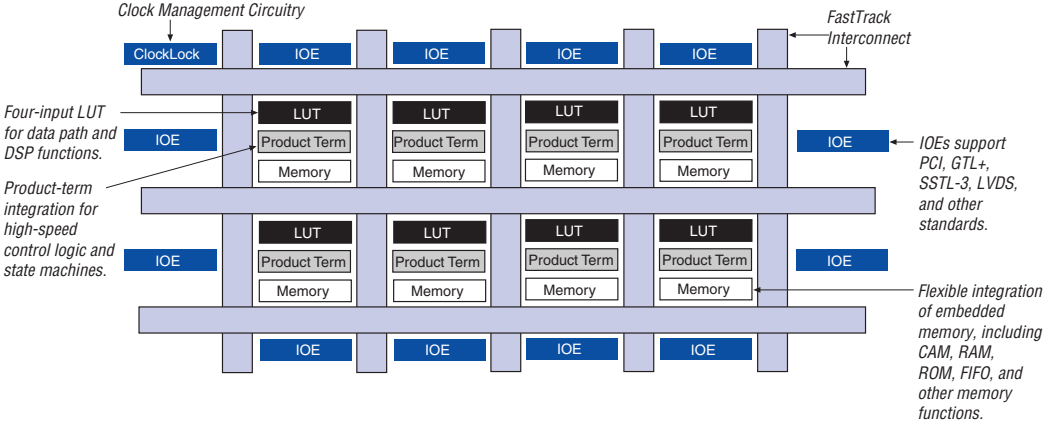


Figure 12. APEX 20KE FastRow Interconnect

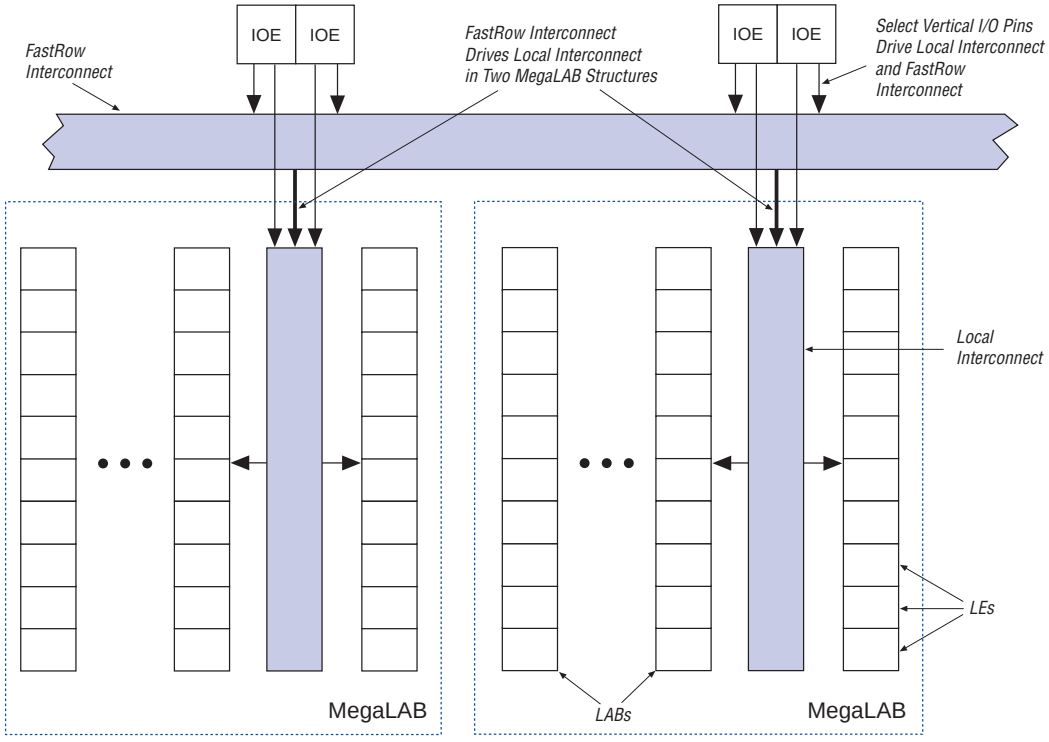
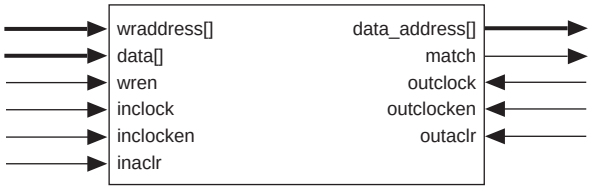


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

Figure 23. APEX 20KE CAM Block Diagram



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't-care" bit can be used as a mask for CAM comparisons; any bit set to "don't-care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address `12`, the ESB output is `12`. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address `12`, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

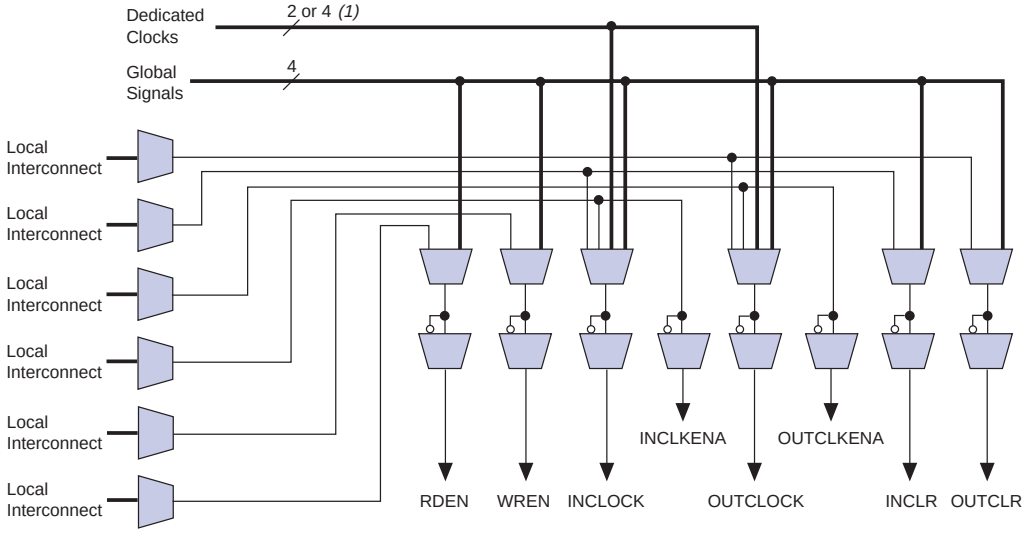
CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't-care" bits are used, a third clock cycle is required.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

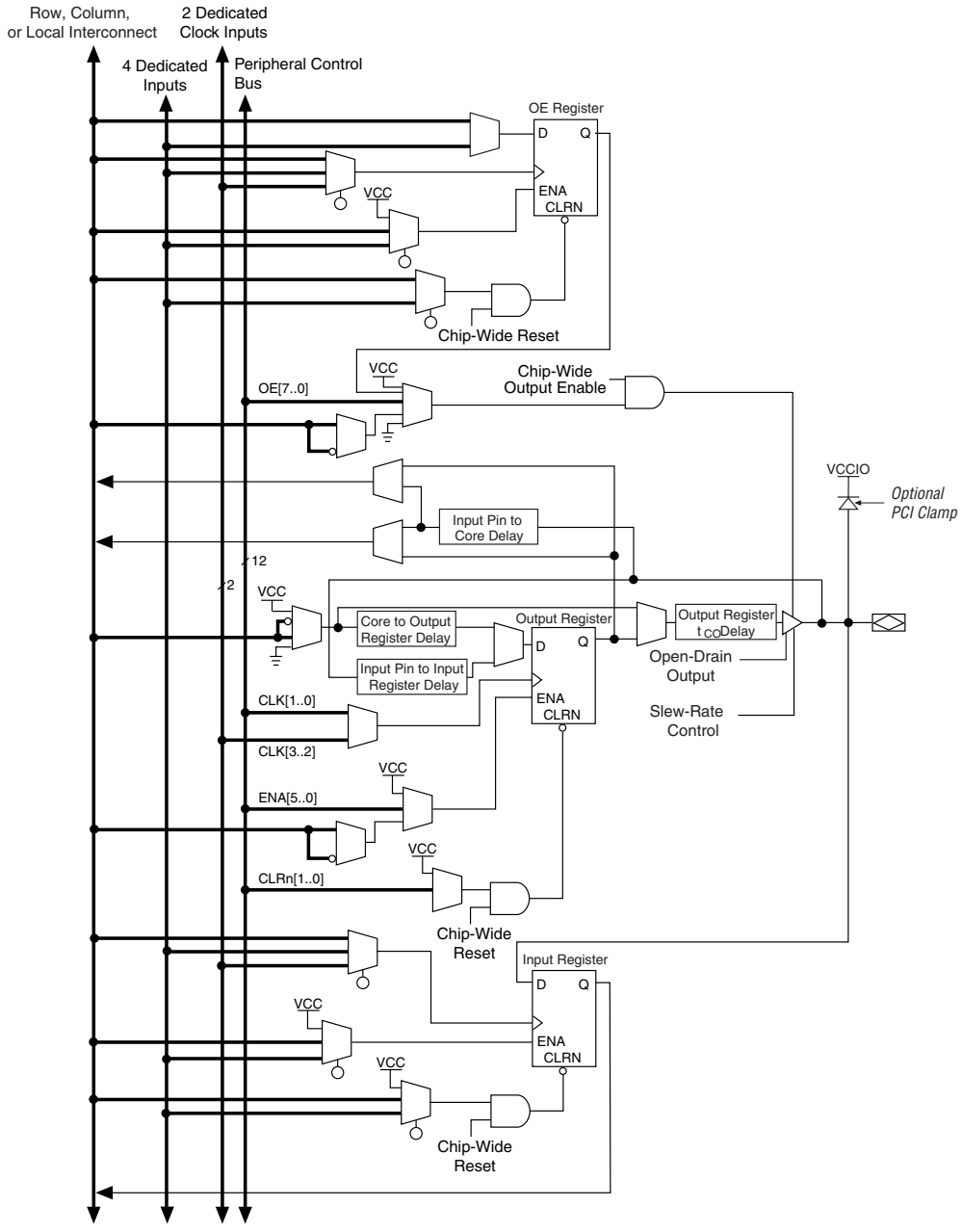
Figure 24. ESB Control Signal Generation



Note to Figure 24:
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Figure 25. APEX 20K Bidirectional I/O Registers *Note (1)*

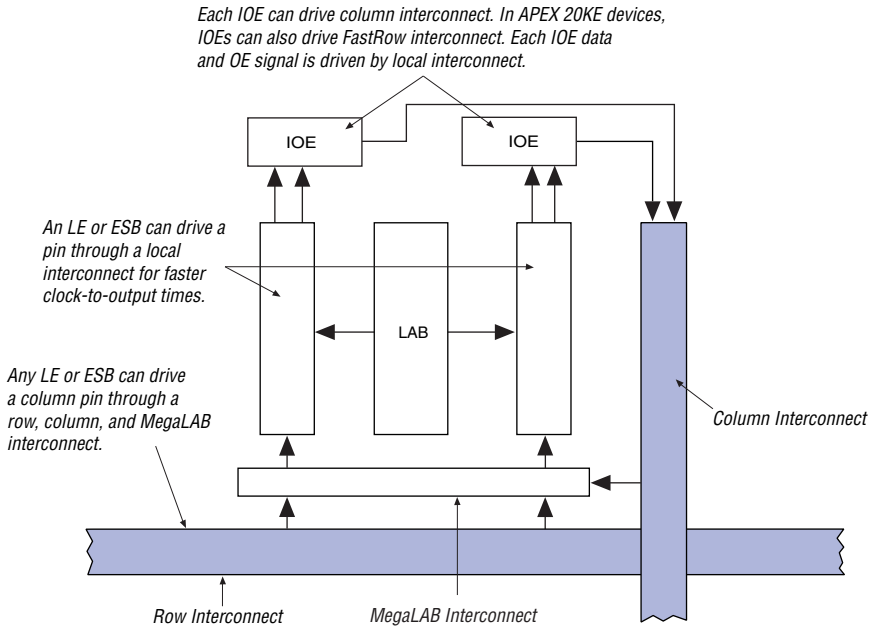


Note to Figure 25:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Figure 28 shows how a column IOE connects to the interconnect.

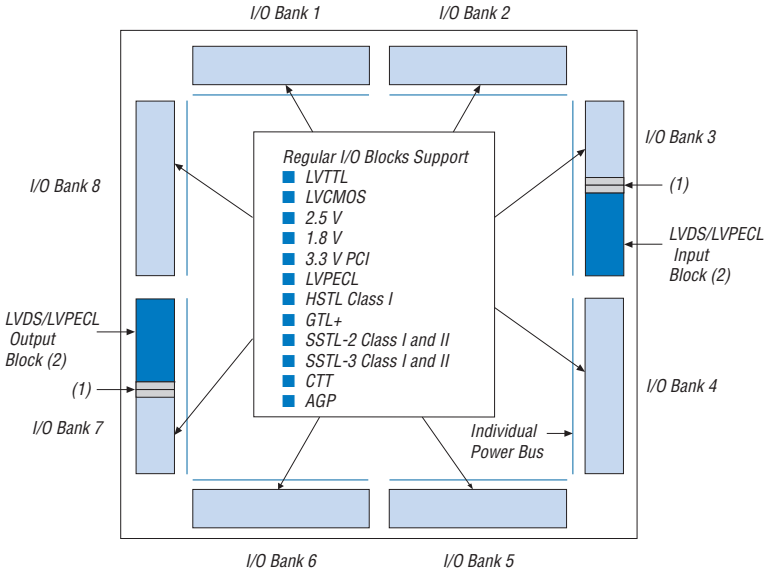
Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Figure 29. APEX 20KE I/O Banks



Notes to Figure 29:

(1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices*).

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 14. Multiplication Factor Combinations

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where m and k range from 2 to 160, and n and v range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(11)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(11)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(11)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(11)*			0.7	V
I_I	Input pin leakage current	V_I = 5.75 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.75 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade *(12)*		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades *(12)*		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(13)*	20		50	W
		V_{CCIO} = 2.375 V *(13)*	30		80	W

Figure 37. APEX 20KE f_{MAX} Timing Model

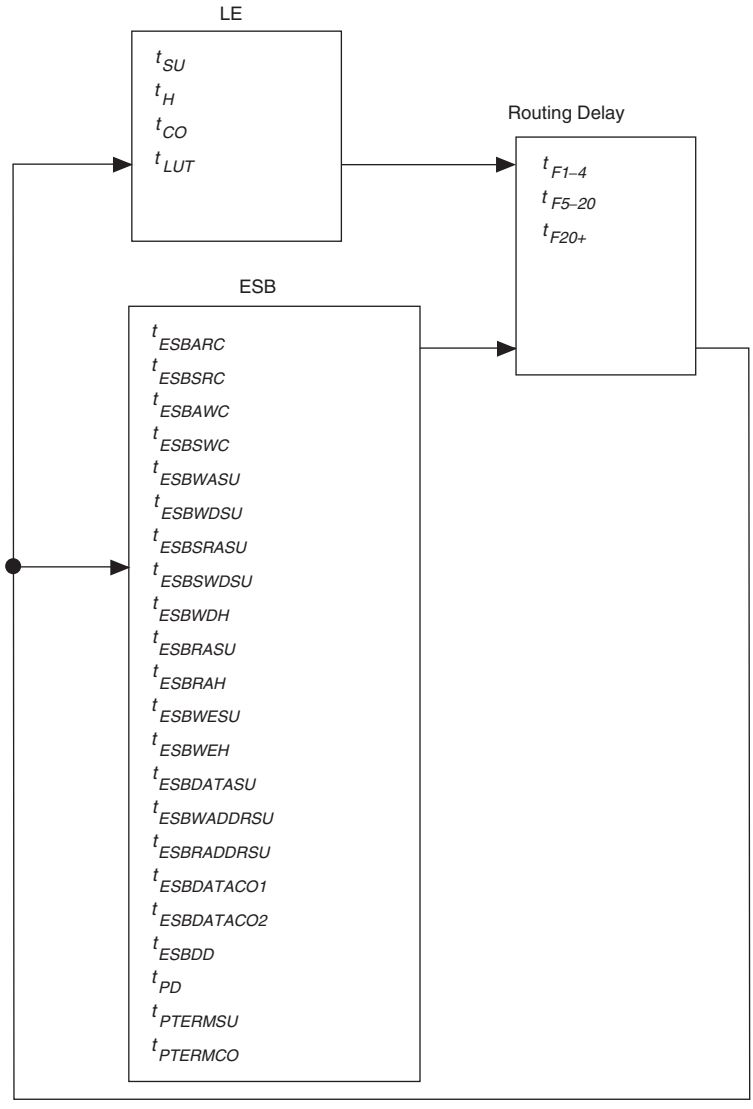


Table 69. EP20K160E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.26		0.28	ns
t_{F5-20}		1.00		1.18		1.35	ns
t_{F20+}		1.95		2.19		2.30	ns

Table 70. EP20K160E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.34		1.43		1.55		ns
t_{CL}	1.34		1.43		1.55		ns
t_{CLRP}	0.18		0.19		0.21		ns
t_{PREP}	0.18		0.19		0.21		ns
t_{ESBCH}	1.34		1.43		1.55		ns
t_{ESBCL}	1.34		1.43		1.55		ns
t_{ESBWP}	1.15		1.45		1.73		ns
t_{ESBRP}	0.93		1.15		1.38		ns

Table 71. EP20K160E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.23		2.34		2.47		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{INSUPLL}$	2.12		2.07		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns

Table 72. EP20K160E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.86		3.24		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{XZBIDIR}$		7.43		8.23		8.58	ns
$t_{ZXBIDIR}$		7.43		8.23		8.58	ns
$t_{INSUBIDIRPLL}$	4.93		5.48		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{XZBIDIRPLL}$		5.36		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.36		5.99		-	ns

Tables 73 through 78 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

Table 73. EP20K200E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.24		0.26		ns
t_{H}	0.23		0.24		0.26		ns
t_{CO}		0.26		0.31		0.36	ns
t_{LUT}		0.70		0.90		1.14	ns

Table 78. EP20K200E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.81		3.19		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{XZBIDIR}$		7.51		8.32		8.67	ns
$t_{ZXBIDIR}$		7.51		8.32		8.67	ns
$t_{INSUBIDIRPLL}$	3.30		3.64		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{XZBIDIRPLL}$		5.40		6.05		-	ns
$t_{ZXBIDIRPLL}$		5.40		6.05		-	ns

Tables 79 through 84 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

Table 79. EP20K300E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.17		0.18		ns
t_{H}	0.31		0.33		0.38		ns
t_{CO}		0.28		0.38		0.51	ns
t_{LUT}		0.79		1.07		1.43	ns

Table 80. EP20K300E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.79		2.44		3.25	ns
t_{ESBSRC}		2.40		3.12		4.01	ns
t_{ESBAWC}		3.41		4.65		6.20	ns
t_{ESBSWC}		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
t_{ESBDD}		3.41		4.65		6.20	ns
t_{PD}		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

Table 81. EP20K300E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.24		0.26	ns
t_{F5-20}		1.33		1.43		1.58	ns
t_{F20+}		3.63		3.93		4.35	ns

Table 86. EP20K400E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		1.91		1.99	ns
t_{ESBSRC}		2.30		2.66		2.93	ns
t_{ESBAWC}		3.09		3.58		3.99	ns
t_{ESBSWC}		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
t_{ESBWAH}	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
t_{ESBWDH}	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
t_{ESBDD}		2.73		3.17		3.58	ns
t_{PD}		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

Table 87. EP20K400E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.25		0.26	ns
t_{F5-20}		1.01		1.12		1.25	ns
t_{F20+}		3.71		3.92		4.17	ns

Table 88. EP20K400E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.22		2.35		ns
t_{CL}	1.36		2.26		2.35		ns
t_{CLRP}	0.18		0.18		0.19		ns
t_{PREP}	0.18		0.18		0.19		ns
t_{ESBCH}	1.36		2.26		2.35		ns
t_{ESBCL}	1.36		2.26		2.35		ns
t_{ESBWP}	1.17		1.38		1.56		ns
t_{ESBRP}	0.94		1.09		1.25		ns

Table 89. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.51		2.64		2.77		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

Table 92. EP20K600E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		2.39		3.11	ns
t_{ESBSRC}		2.27		3.07		3.86	ns
t_{ESBAWC}		3.19		4.56		5.93	ns
t_{ESBSWC}		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATACO1}$		1.01		1.19		1.37	ns
$t_{ESBDATACO2}$		2.18		3.12		4.05	ns
t_{ESBDD}		3.19		4.56		5.93	ns
t_{PD}		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

Table 93. EP20K600E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.25		0.26	ns
t_{F5-20}		1.26		1.39		1.52	ns
t_{F20+}		3.51		3.88		4.26	ns

Table 94. EP20K600E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.00		2.50		2.75		ns
t_{CL}	2.00		2.50		2.75		ns
t_{CLRP}	0.18		0.26		0.34		ns
t_{PREP}	0.18		0.26		0.34		ns
t_{ESBCH}	2.00		2.50		2.75		ns
t_{ESBCL}	2.00		2.50		2.75		ns
t_{ESBWP}	1.17		1.68		2.18		ns
t_{ESBRP}	0.95		1.35		1.76		ns

Table 95. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.74		2.74		2.87		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.51	2.00	6.06	2.00	6.61	ns
$t_{INSUPLL}$	1.86		1.96		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.62	0.50	2.91	-	-	ns

Table 96. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	0.64		0.98		1.08		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.51	2.00	6.06	2.00	6.61	ns
$t_{XZBIDIR}$		6.10		6.74		7.10	ns
$t_{ZXBIDIR}$		6.10		6.74		7.10	ns
$t_{INSUBIDIRPLL}$	2.26		2.68		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.62	0.50	2.91	-	-	ns
$t_{XZBIDIRPLL}$		3.21		3.59		-	ns
$t_{ZXBIDIRPLL}$		3.21		3.59		-	ns

Table 110. Selectable I/O Standard Output Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		–0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		–0.48		–0.48		–0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.