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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1152
Number of Logic Elements/Cells	11520
Total RAM Bits	147456
Number of I/O	408
Number of Gates	728000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k300ebc672-2x">https://www.e-xfl.com/product-detail/intel/ep20k300ebc672-2x</a>

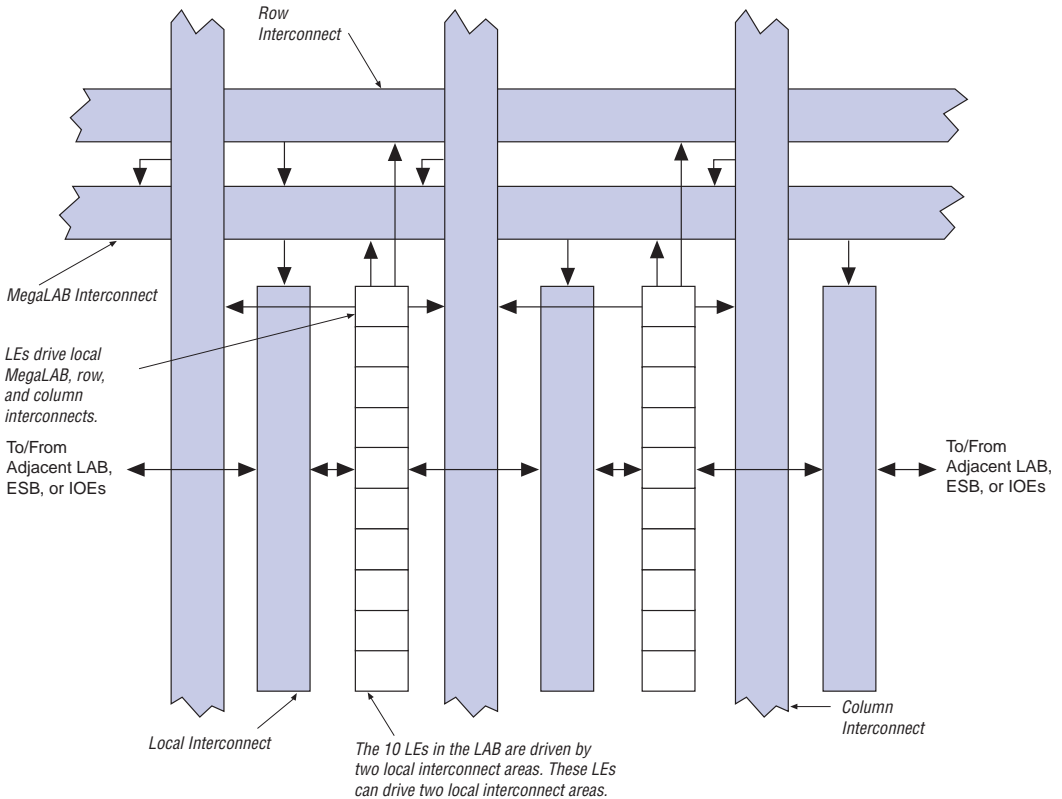
- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock<sup>®</sup> feature reducing clock delay and skew
  - ClockBoost<sup>®</sup> feature providing clock multiplication and division
  - ClockShift<sup>™</sup> programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ( $t_{CO} + t_{SU}$ ) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - Programmable clamp to  $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack<sup>®</sup> Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
  - FineLine BGA<sup>®</sup> packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera<sup>®</sup> Quartus<sup>®</sup> II development system for

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 3. LAB Structure**



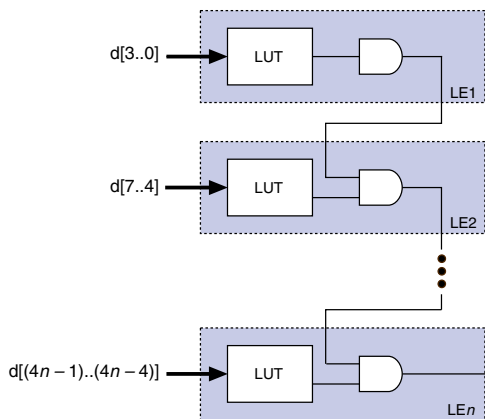
## Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

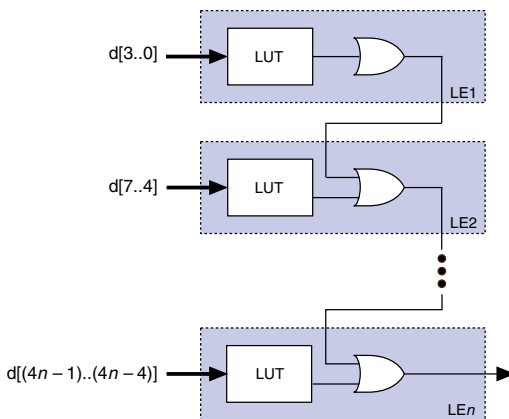
Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

**Figure 7. APEX 20K Cascade Chain**

**AND Cascade Chain**



**OR Cascade Chain**



### *LE Operating Modes*

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

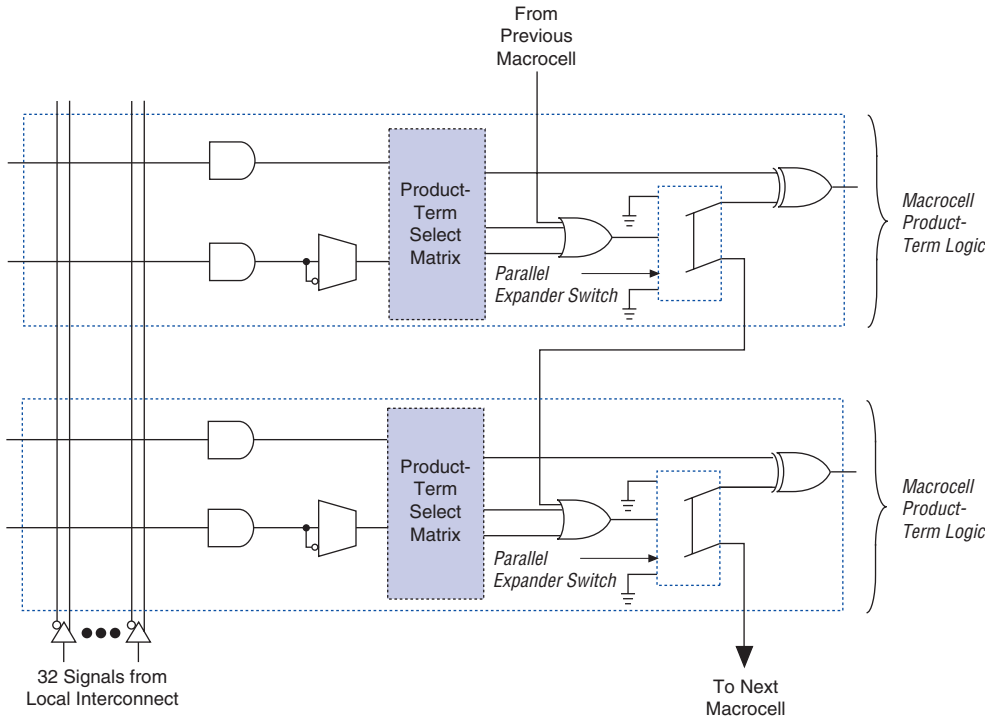
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV\_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## **FastTrack Interconnect**

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).

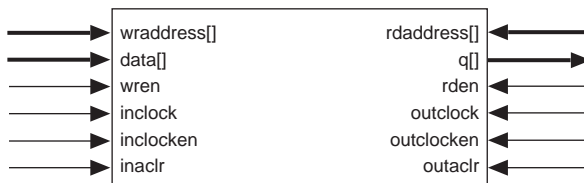
**Figure 16. APEX 20K Parallel Expanders**



## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

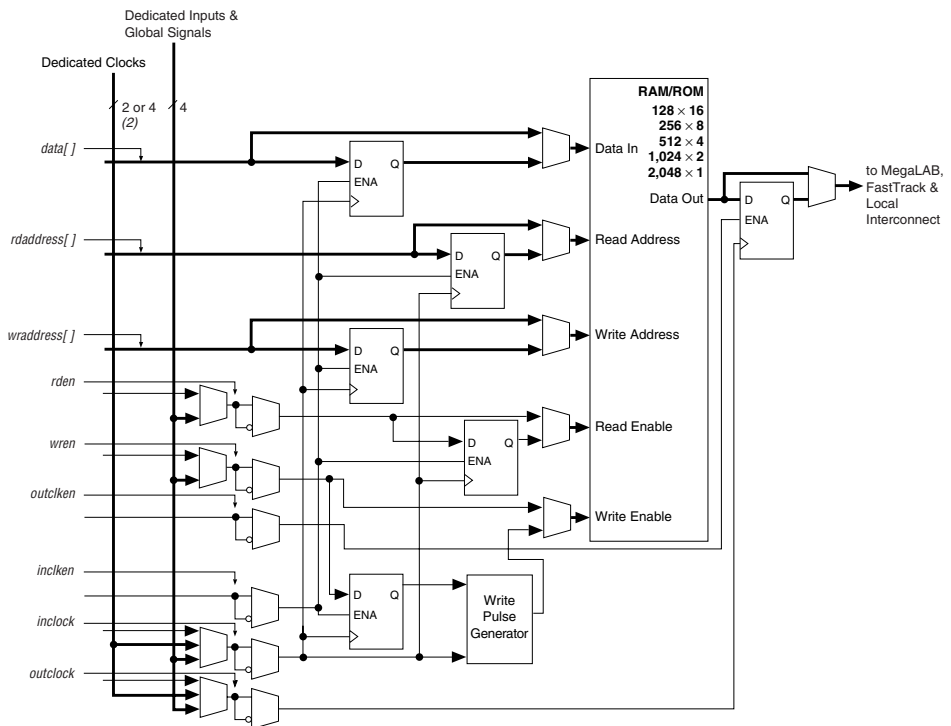
**Figure 17. ESB Block Diagram**



## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

**Figure 21. ESB in Input/Output Clock Mode** Note (1)



### Notes to Figure 21:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.



## Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

## Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

<b>Table 10. APEX 20K Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register $t_{CO}$ delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

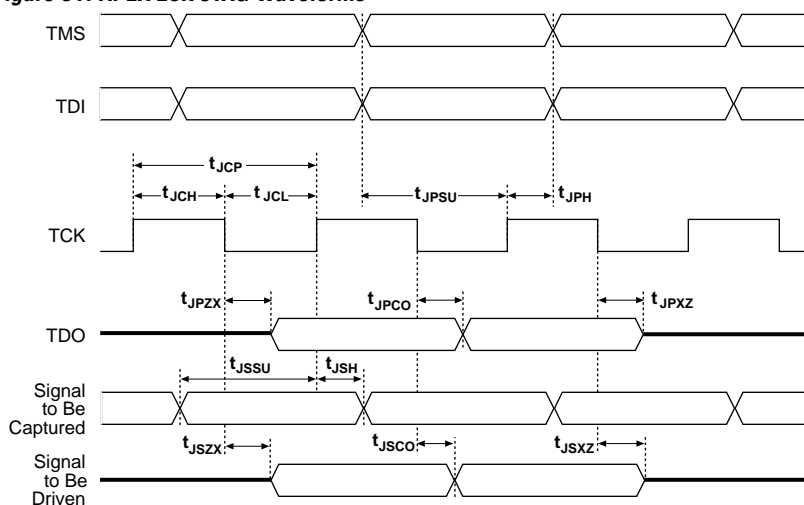
**Table 21. 32-Bit APEX 20K Device IDCODE**

Device	IDCODE (32 Bits) <sup>(1)</sup>			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) <sup>(2)</sup>
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

**Notes to Table 21:**

- (1) The most significant bit (MSB) is on the left.  
 (2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

**Figure 31. APEX 20K JTAG Waveforms**

**Table 52. EP20K30E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	0.55		0.78		1.15		ns
t <sub>CL</sub>	0.55		0.78		1.15		ns
t <sub>CLRP</sub>	0.22		0.31		0.46		ns
t <sub>PREP</sub>	0.22		0.31		0.46		ns
t <sub>ESBCH</sub>	0.55		0.78		1.15		ns
t <sub>ESBCL</sub>	0.55		0.78		1.15		ns
t <sub>ESBWP</sub>	1.43		2.01		2.97		ns
t <sub>ESBRP</sub>	1.15		1.62		2.39		ns

**Table 53. EP20K30E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.02		2.13		2.24		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>INSUPLL</sub>	2.11		2.23		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns

**Table 54. EP20K30E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	1.85		1.77		1.54		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>XZBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>ZXBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>INSUBIDIRPLL</sub>	4.12		4.24		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns
t <sub>XZBIDIRPLL</sub>		5.21		5.99		-	ns
t <sub>ZXBIDIRPLL</sub>		5.21		5.99		-	ns

**Table 64. EP20K100E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	2.00		2.00		2.00		ns
t <sub>CL</sub>	2.00		2.00		2.00		ns
t <sub>CLRP</sub>	0.20		0.20		0.20		ns
t <sub>PREP</sub>	0.20		0.20		0.20		ns
t <sub>ESBCH</sub>	2.00		2.00		2.00		ns
t <sub>ESBCL</sub>	2.00		2.00		2.00		ns
t <sub>ESBWP</sub>	1.29		1.53		1.66		ns
t <sub>ESBRP</sub>	1.11		1.29		1.41		ns

**Table 65. EP20K100E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.23		2.32		2.43		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.86	2.00	5.35	2.00	5.84	ns
t <sub>INSUPLL</sub>	1.58		1.66		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.96	0.50	3.29	-	-	ns

**Table 66. EP20K100E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	2.74		2.96		3.19		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.86	2.00	5.35	2.00	5.84	ns
t <sub>XZBIDIR</sub>		5.00		5.48		5.89	ns
t <sub>ZXBIDIR</sub>		5.00		5.48		5.89	ns
t <sub>INSUBIDIRPLL</sub>	4.64		5.03		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.96	0.50	3.29	-	-	ns
t <sub>XZBIDIRPLL</sub>		3.10		3.42		-	ns
t <sub>ZXBIDIRPLL</sub>		3.10		3.42		-	ns

Tables 67 through 72 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

**Table 67. EP20K160E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.22		0.24		0.26		ns
$t_H$	0.22		0.24		0.26		ns
$t_{CO}$		0.25		0.31		0.35	ns
$t_{LUT}$		0.69		0.88		1.12	ns

**Table 68. EP20K160E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.65		2.02		2.11	ns
$t_{ESBSRC}$		2.21		2.70		3.11	ns
$t_{ESBAWC}$		3.04		3.79		4.42	ns
$t_{ESBSWC}$		2.81		3.56		4.10	ns
$t_{ESBWASU}$	0.54		0.66		0.73		ns
$t_{ESBWAH}$	0.36		0.45		0.47		ns
$t_{ESBWDSU}$	0.68		0.81		0.94		ns
$t_{ESBWDH}$	0.36		0.45		0.47		ns
$t_{ESBRASU}$	1.58		1.87		2.06		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.41		1.71		2.00		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.02		-0.03		0.09		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.14		0.17		0.35		ns
$t_{ESBRADDRSU}$	0.21		0.27		0.43		ns
$t_{ESBDATACO1}$		1.04		1.30		1.46	ns
$t_{ESBDATACO2}$		2.15		2.70		3.16	ns
$t_{ESBDD}$		2.69		3.35		3.97	ns
$t_{PD}$		1.55		1.93		2.29	ns
$t_{PTERMSU}$	1.01		1.23		1.52		ns
$t_{PTERMCO}$		1.06		1.32		1.04	ns

**Table 69. EP20K160E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.26		0.28	ns
$t_{F5-20}$		1.00		1.18		1.35	ns
$t_{F20+}$		1.95		2.19		2.30	ns

**Table 70. EP20K160E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.34		1.43		1.55		ns
$t_{CL}$	1.34		1.43		1.55		ns
$t_{CLRP}$	0.18		0.19		0.21		ns
$t_{PREP}$	0.18		0.19		0.21		ns
$t_{ESBCH}$	1.34		1.43		1.55		ns
$t_{ESBCL}$	1.34		1.43		1.55		ns
$t_{ESBWP}$	1.15		1.45		1.73		ns
$t_{ESBRP}$	0.93		1.15		1.38		ns

**Table 71. EP20K160E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.23		2.34		2.47		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{INSUPLL}$	2.12		2.07		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns



**Table 78. EP20K200E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.81		3.19		3.54		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{\text{XZBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{ZXBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{INSUBIDIRPLL}}$	3.30		3.64		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.40		6.05		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.40		6.05		-	ns

Tables 79 through 84 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

**Table 79. EP20K300E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.16		0.17		0.18		ns
$t_{\text{H}}$	0.31		0.33		0.38		ns
$t_{\text{CO}}$		0.28		0.38		0.51	ns
$t_{\text{LUT}}$		0.79		1.07		1.43	ns

**Table 80. EP20K300E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.79		2.44		3.25	ns
$t_{ESBSRC}$		2.40		3.12		4.01	ns
$t_{ESBAWC}$		3.41		4.65		6.20	ns
$t_{ESBSWC}$		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
$t_{ESBDD}$		3.41		4.65		6.20	ns
$t_{PD}$		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

**Table 81. EP20K300E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.24		0.26	ns
$t_{F5-20}$		1.33		1.43		1.58	ns
$t_{F20+}$		3.63		3.93		4.35	ns

**Table 87. EP20K400E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.25		0.26	ns
$t_{F5-20}$		1.01		1.12		1.25	ns
$t_{F20+}$		3.71		3.92		4.17	ns

**Table 88. EP20K400E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.36		2.22		2.35		ns
$t_{CL}$	1.36		2.26		2.35		ns
$t_{CLRP}$	0.18		0.18		0.19		ns
$t_{PREP}$	0.18		0.18		0.19		ns
$t_{ESBCH}$	1.36		2.26		2.35		ns
$t_{ESBCL}$	1.36		2.26		2.35		ns
$t_{ESBWP}$	1.17		1.38		1.56		ns
$t_{ESBRP}$	0.94		1.09		1.25		ns

**Table 89. EP20K400E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.51		2.64		2.77		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

**Table 92. EP20K600E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		2.39		3.11	ns
$t_{ESBSRC}$		2.27		3.07		3.86	ns
$t_{ESBAWC}$		3.19		4.56		5.93	ns
$t_{ESBSWC}$		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATAO1}$		1.01		1.19		1.37	ns
$t_{ESBDATAO2}$		2.18		3.12		4.05	ns
$t_{ESBDD}$		3.19		4.56		5.93	ns
$t_{PD}$		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

**Table 93. EP20K600E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.25		0.26	ns
$t_{F5-20}$		1.26		1.39		1.52	ns
$t_{F20+}$		3.51		3.88		4.26	ns

## Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

### Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

### Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for  $t_{ESB\text{DATAH}}$  parameter.

### Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

### Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.