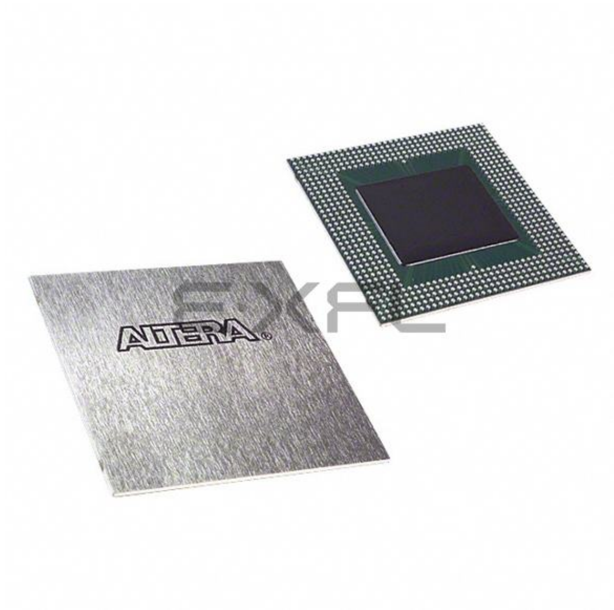

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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1152 |
| Number of Logic Elements/Cells | 11520 |
| Total RAM Bits | 147456 |
| Number of I/O | 408 |
| Number of Gates | 728000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 652-BBGA |
| Supplier Device Package | 652-BGA (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k300ebi652-2x |

*Table 8. Comparison of APEX 20K & APEX 20KE Features*

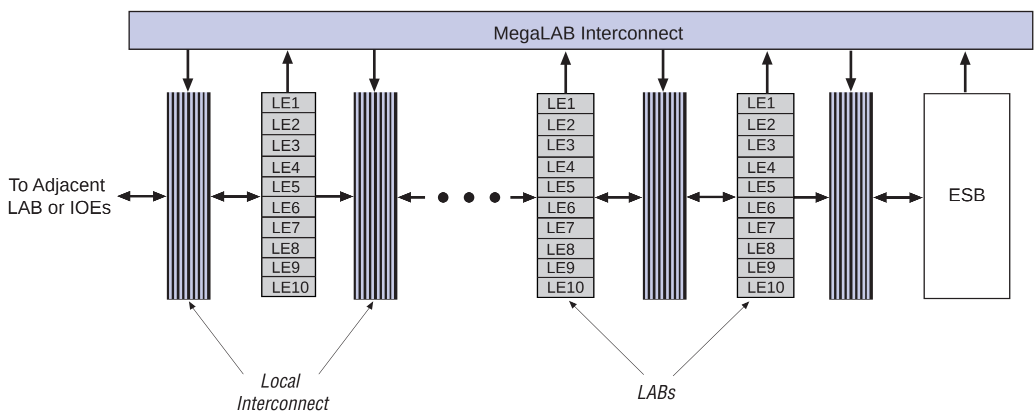
| Feature | APEX 20K Devices | APEX 20KE Devices |
|---|---|---|
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

## MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

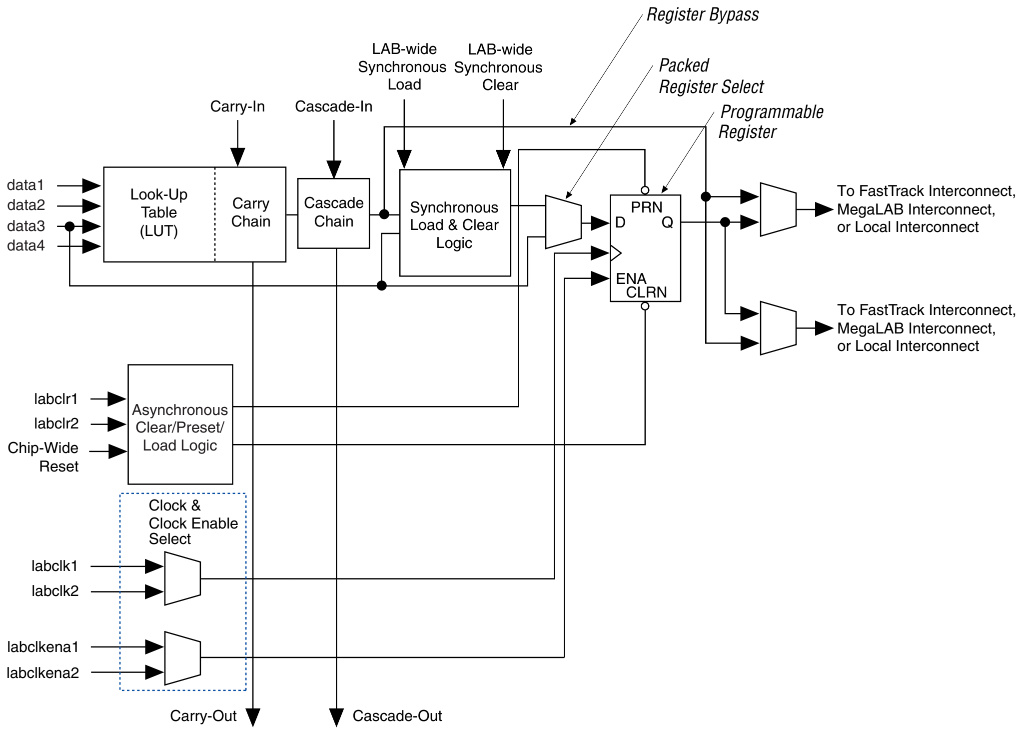
*Figure 2. MegaLAB Structure*



## Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

*Figure 5. APEX 20K Logic Element*




Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

### Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

**Figure 7. APEX 20K Cascade Chain**

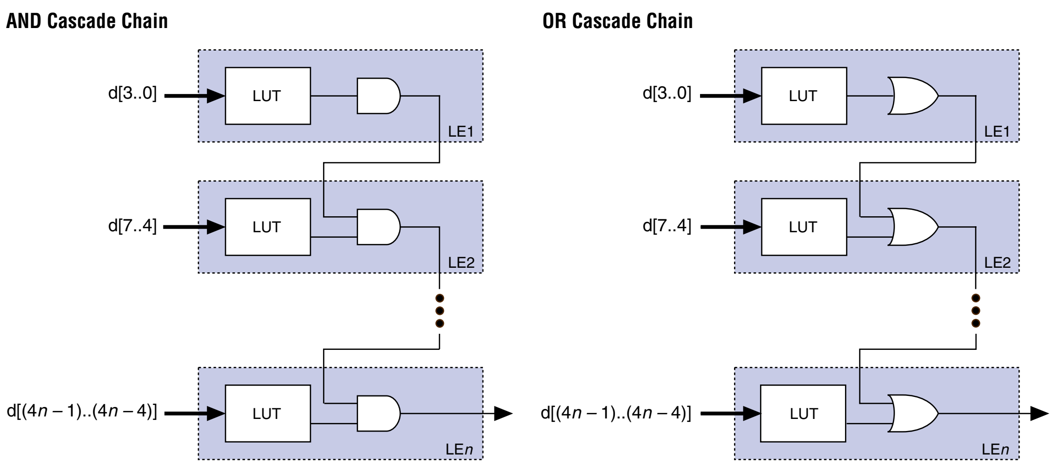
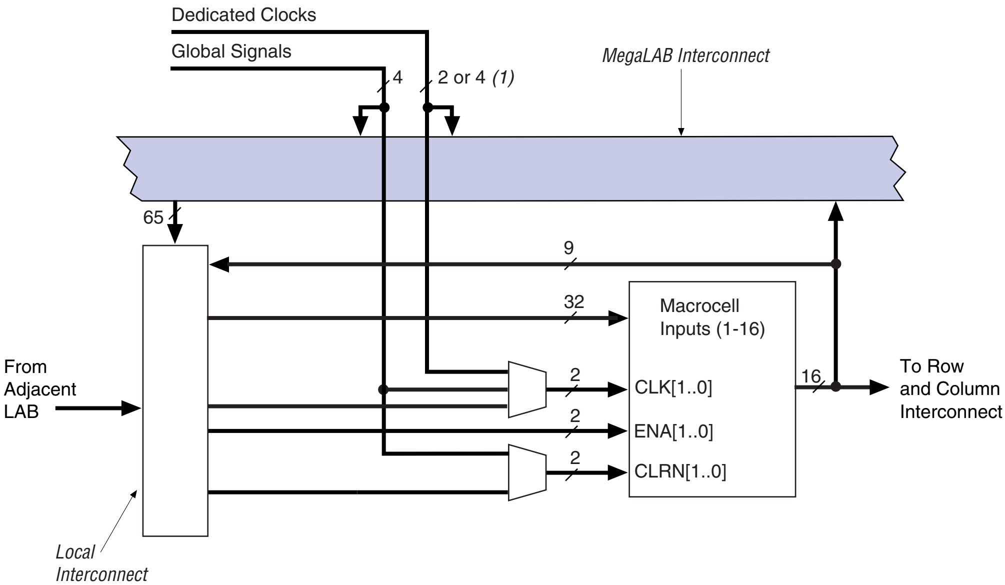


*Figure 13. Product-Term Logic in ESB*




*Note to Figure 13:*

(1) APEX 20KE devices have four dedicated clocks.

## Macrocells

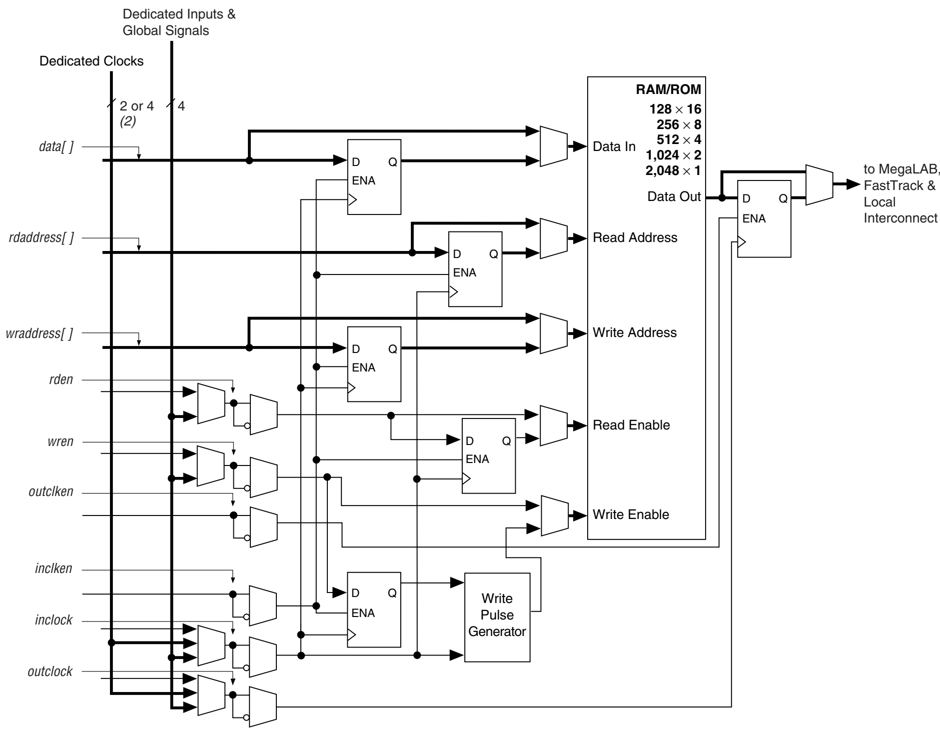
APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide `OR` functions. The Quartus II software Compiler can use a `NOT`-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

**Figure 21. ESB in Input/Output Clock Mode** Note (1)




*Notes to Figure 21:*

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

### Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

### Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

### *Clock Phase & Delay Adjustment*

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

### *LVDS Support*

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

### *Lock Signals*

The APEX 20KE ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

*Notes to Table 16:*

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus II software, designers must specify the input frequency. The Quartus II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the $t_{LOCK}$ value is less than the time required for configuration.

(4) The $t_{JITTER}$ specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

**Table 17. APEX 20KE ClockLock & ClockBoost Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $t_{INJITTER}$ | Input jitter peak-to-peak | | | | 2% of input period | peak-to-peak |
| $t_{OUTJITTER}$ | Jitter on ClockLock or ClockBoost-generated clock | | | | 0.35% of output period | RMS |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 45 | | 55 | % |
| $t_{LOCK}$ (2), (3) | Time required for ClockLock or ClockBoost to acquire lock | | | | 40 | µs |

| *Table 18. APEX 20KE Clock Input & Output Parameters (Part 2 of 2) Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **I/O Standard** | **-1X Speed Grade** | | **-2X Speed Grade** | | **Units** |
| | | | **Min** | **Max** | **Min** | **Max** | |
| $f_{IN}$ | Input clock frequency | 3.3-V LVTTL | 1.5 | 290 | 1.5 | 257 | MHz |
| | | 2.5-V LVTTL | 1.5 | 281 | 1.5 | 250 | MHz |
| | | 1.8-V LVTTL | 1.5 | 272 | 1.5 | 243 | MHz |
| | | GTL+ | 1.5 | 303 | 1.5 | 261 | MHz |
| | | SSTL-2 Class I | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-2 Class II | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-3 Class I | 1.5 | 300 | 1.5 | 260 | MHz |
| | | SSTL-3 Class II | 1.5 | 300 | 1.5 | 260 | MHz |
| | | LVDS | 1.5 | 420 | 1.5 | 350 | MHz |

*Notes to Tables 17 and 18:*

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.

(2) The maximum lock time is 40 µs or 2000 input clock cycles, whichever occurs first.

(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.

(4) The PLL VCO operating range is 200 MHz ð $f_{VCO}$ ð 840 MHz for LVDS mode.

## SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

**Table 19. APEX 20K JTAG Instructions**

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS *(1)* | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`. |
| IDCODE | Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`. |
| ICR Instructions | Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor. |
| SignalTap Instructions *(1)* | Monitors internal device operation with the SignalTap embedded logic analyzer. |

*Note to Table 19:*
(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

*Table 20. APEX 20K Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K30E | 420 |
| EP20K60E | 624 |
| EP20K100 | 786 |
| EP20K100E | 774 |
| EP20K160E | 984 |
| EP20K200 | 1,176 |
| EP20K200E | 1,164 |
| EP20K300E | 1,266 |
| EP20K400 | 1,536 |
| EP20K400E | 1,506 |
| EP20K600E | 1,806 |
| EP20K1000E | 2,190 |
| EP20K1500E | 1 *(1)* |

***Note to Table 20:***
(1) This device does not support JTAG boundary scan testing.

| *Table 29. APEX 20KE Device DC Operating Conditions* *Notes (7), (8), (9)* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{IH}$ | High-level LVTTL, CMOS, or 3.3-V PCI input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(10)* | | 4.1 | V |
| $V_{IL}$ | Low-level LVTTL, CMOS, or 3.3-V PCI input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(10)* | V |
| $V_{OH}$ | 3.3-V high-level LVTTL output voltage | $I_{OH}$ = –12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | 2.4 | | | V |
| | 3.3-V high-level LVCMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(11)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level LVTTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(12)* | | | 0.4 | V |
| | 3.3-V low-level LVCMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(12)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(12)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 4.1 to –0.5 V *(13)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 4.1 to –0.5 V *(13)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(14)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(14)* | 30 | | 80 | kΩ |
| | | $V_{CCIO}$ = 1.71 V *(14)* | 60 | | 150 | kΩ |

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

**Table 30. APEX 20KE Device Capacitance** *Note (15)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 27 through 30:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

| Vin | Max. Duty Cycle |
|---|---|
| 4.0V | 100% (DC) |
| 4.1 | 90% |
| 4.2 | 50% |
| 4.3 | 30% |
| 4.4 | 17% |
| 4.5 | 10% |

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, and $I_I$ parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.

| Table 60. EP20K60E External Bidirectional Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 | | -2 | | -3 | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.91 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{XZBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{ZXBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{INSUBIDIRPLL}$ | 3.44 | | 3.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |

Tables 61 through 66 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

| Table 61. EP20K100E $f_{MAX}$ LE Timing Microparameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 | | -2 | | -3 | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_H$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.28 | | 0.34 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

Tables 67 through 72 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

**Table 67. EP20K160E $f_{MAX}$ LE Timing Microparameters**

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_H$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.25 | | 0.31 | | 0.35 | ns |
| $t_{LUT}$ | | 0.69 | | 0.88 | | 1.12 | ns |

| Table 90. EP20K400E External Bidirectional Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.93 | | 3.23 | | 3.44 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.25 | 2.00 | 5.79 | 2.00 | 6.32 | ns |
| $t_{XZBIDIR}$ | | 5.95 | | 6.77 | | 7.12 | ns |
| $t_{ZXBIDIR}$ | | 5.95 | | 6.77 | | 7.12 | ns |
| $t_{INSUBIDIRPLL}$ | 4.31 | | 4.76 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.45 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 2.94 | | 3.43 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 2.94 | | 3.43 | | - | ns |

Tables 91 through 96 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K600E APEX 20KE devices.

| Table 91. EP20K600E $f_{MAX}$ LE Timing Microparameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.16 | | 0.17 | | ns |
| $t_H$ | 0.29 | | 0.33 | | 0.37 | | ns |
| $t_{CO}$ | | 0.65 | | 0.38 | | 0.49 | ns |
| $t_{LUT}$ | | 0.70 | | 1.00 | | 1.30 | ns |

*Table 108. EP20K1500E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 3.47 | | 3.68 | | 3.99 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 6.18 | 2.00 | 6.81 | 2.00 | 7.36 | ns |
| $t_{XZBIDIR}$ | | 6.91 | | 7.62 | | 8.38 | ns |
| $t_{ZXBIDIR}$ | | 6.91 | | 7.62 | | 8.38 | ns |
| $t_{INSUBIDIRPLL}$ | 3.05 | | 3.26 | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.67 | 0.50 | 2.99 | | | ns |
| $t_{XZBIDIRPLL}$ | | 3.41 | | 3.80 | | | ns |
| $t_{ZXBIDIRPLL}$ | | 3.41 | | 3.80 | | | ns |

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

*Table 109. Selectable I/O Standard Input Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.04 | | 0.05 | ns |
| 1.8 V | | –0.11 | | 0.03 | | 0.04 | ns |
| PCI | | 0.01 | | 0.09 | | 0.10 | ns |
| GTL+ | | –0.24 | | –0.23 | | –0.19 | ns |
| SSTL-3 Class I | | –0.32 | | –0.21 | | –0.47 | ns |
| SSTL-3 Class II | | –0.08 | | 0.03 | | –0.23 | ns |
| SSTL-2 Class I | | –0.17 | | –0.06 | | –0.32 | ns |
| SSTL-2 Class II | | –0.16 | | –0.05 | | –0.31 | ns |
| LVDS | | –0.12 | | –0.12 | | –0.12 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$ added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.