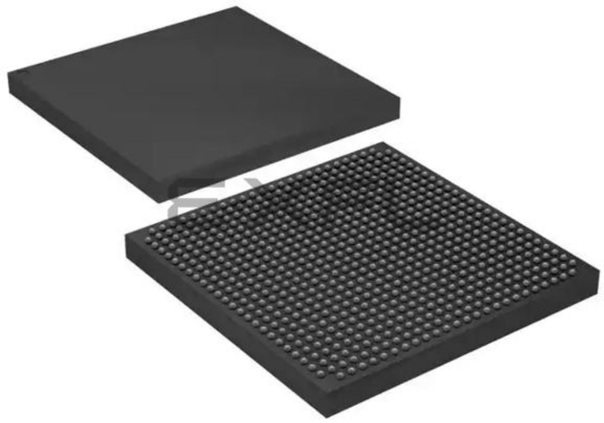
Intel - EP20K300EFI672-3 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1152
Number of Logic Elements/Cells	11520
Total RAM Bits	147456
Number of I/O	408
Number of Gates	728000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k300efi672-3

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 2. Additional APEX 20K Device Features *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

Note to Tables 1 and 2:

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

Table 3. APEX 20K Supply Voltages

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)*

Note to Table 3:

(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS)

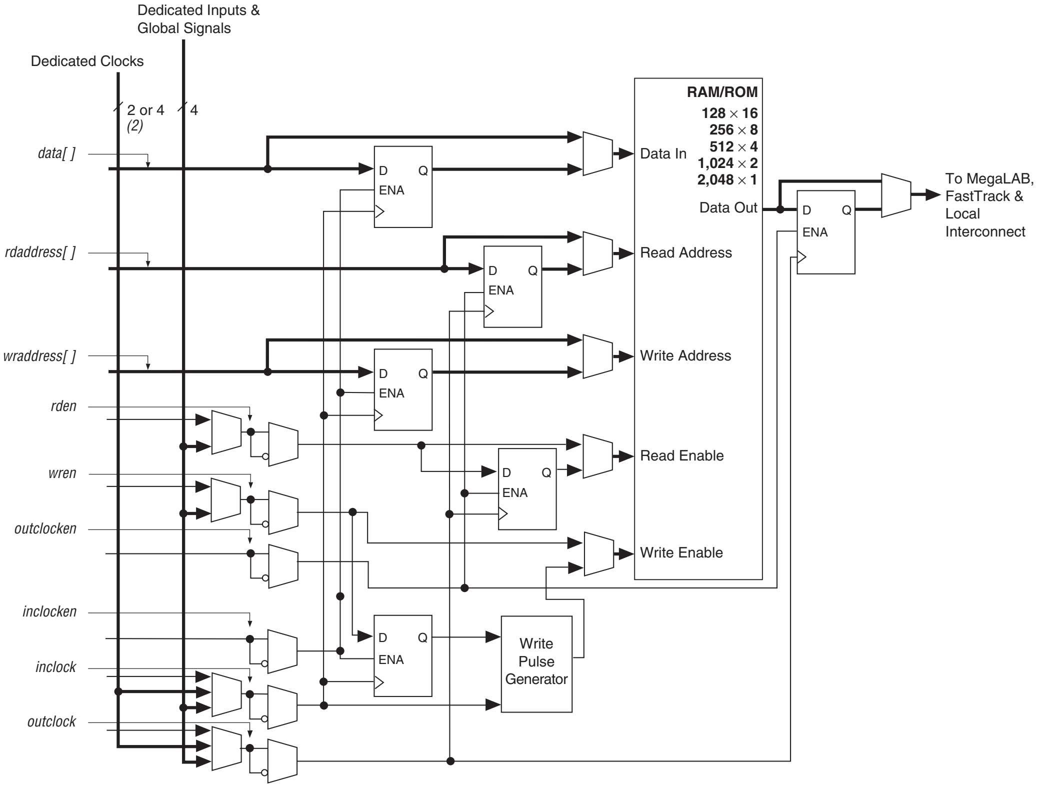
Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, `WE`, and write address. The other clock controls all registers associated with reading: read enable (`RE`), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*

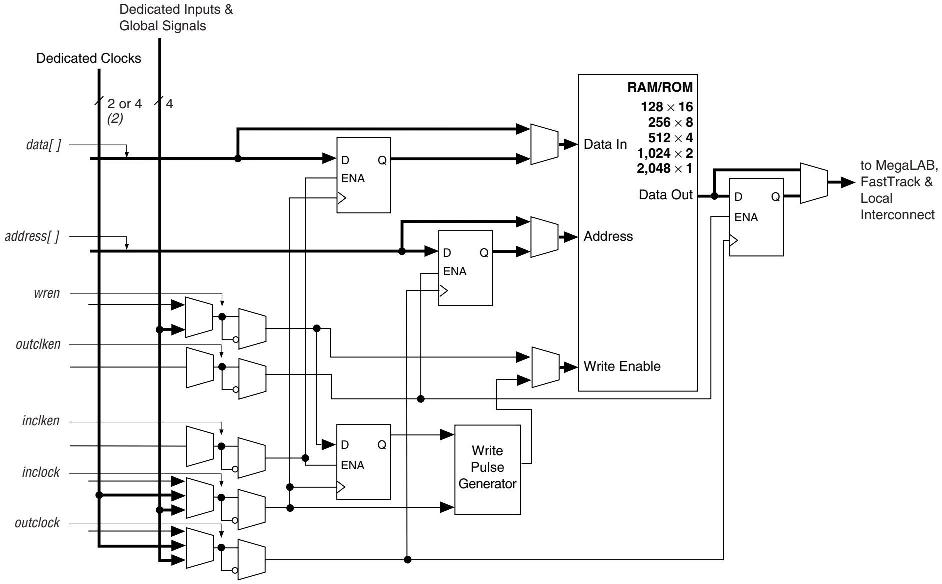


Notes to Figure 20:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

(2) APEX 20KE devices have four dedicated clocks.

Figure 22. ESB in Single-Port Mode *Note (1)*



Notes to Figure 22:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

(2) APEX 20KE devices have four dedicated clocks.

Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

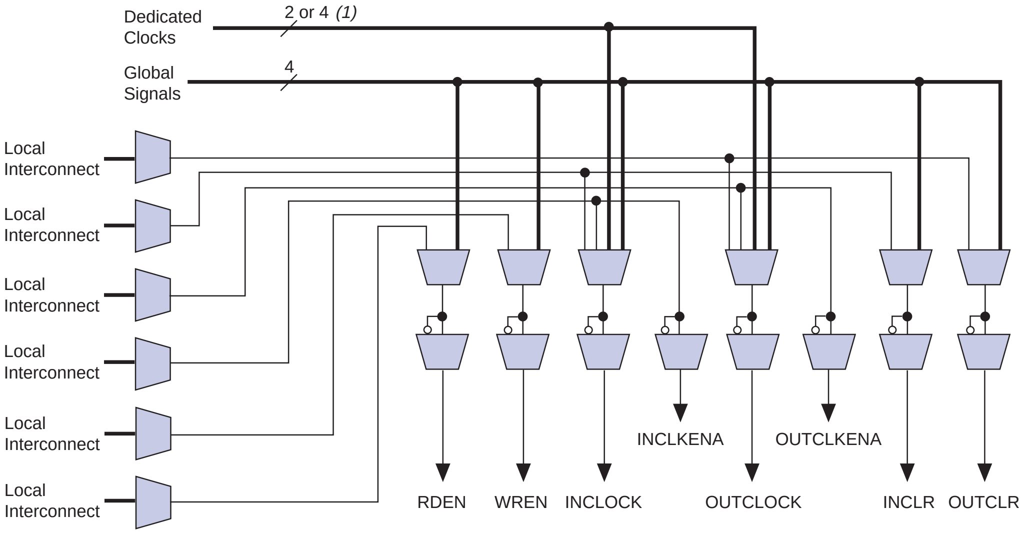
CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, `WE`, and `RE` signals. The global signals and the local interconnect can drive the `WE` and `RE` signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the `WE` and `RE` signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

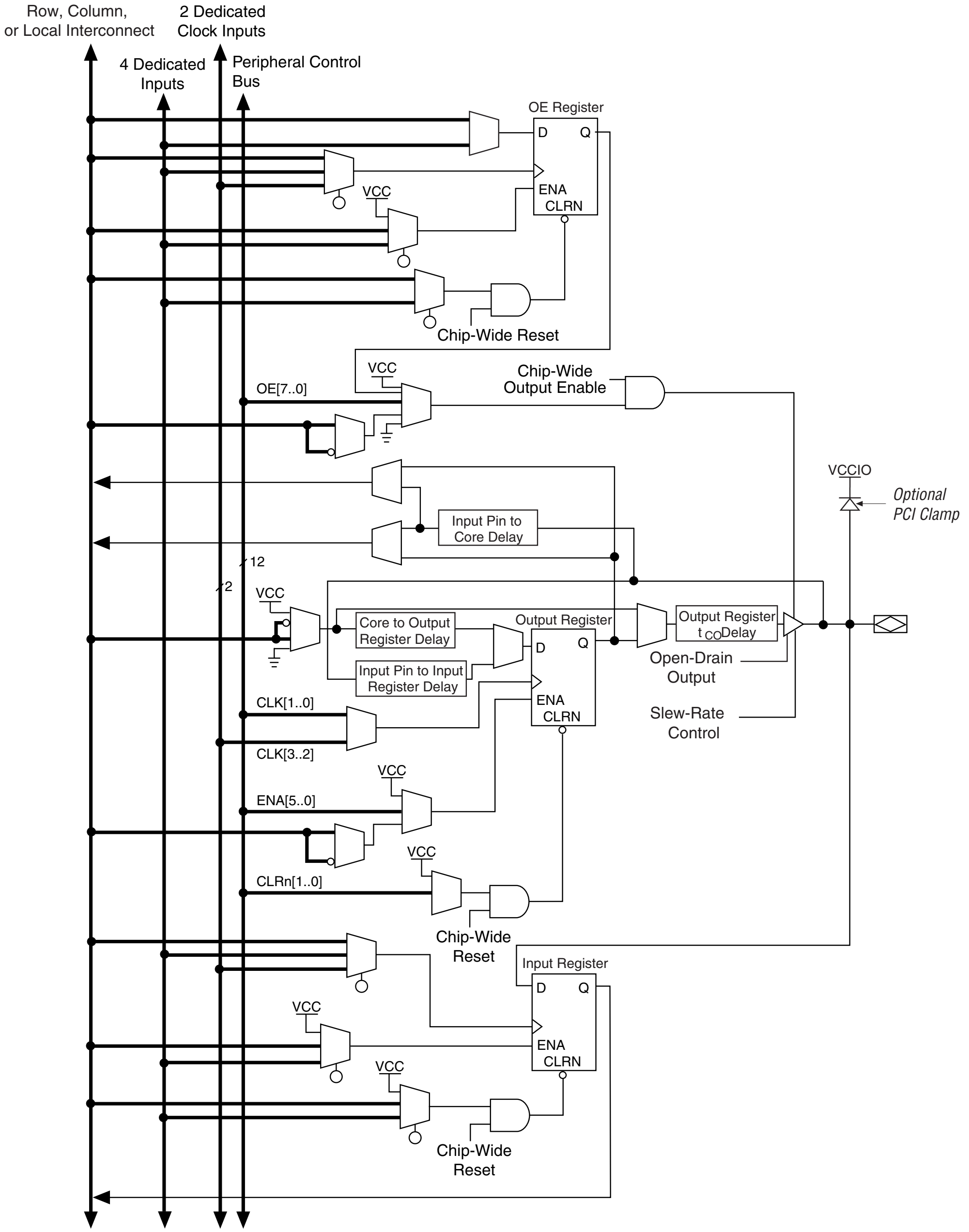
Figure 24. ESB Control Signal Generation



Note to Figure 24:
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Figure 25. APEX 20K Bidirectional I/O Registers *Note (1)*

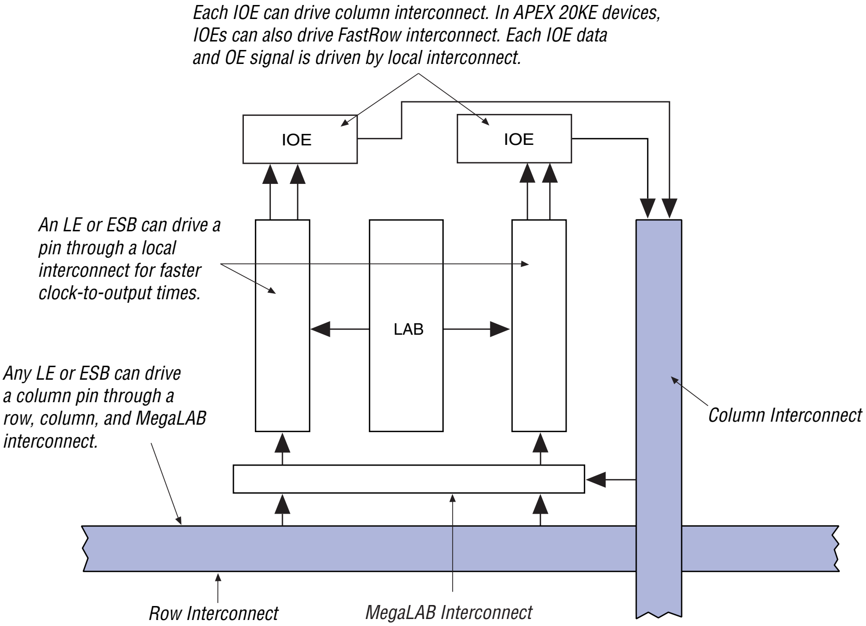


Note to Figure 25:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own `VCCIO` pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same `VCCIO` for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same `VCCIO` voltage level. For example, when `VCCIO` is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of `VCC` pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The APEX 20K `VCCINT` pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The `VCCIO` pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ *(1)*	✓ *(1)*	✓		
3.3	✓	✓	✓ *(1)*	✓ *(2)*	✓	✓

Notes to Table 12:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

Table 19. APEX 20K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS *(1)*	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`.
IDCODE	Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions *(1)*	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 19:

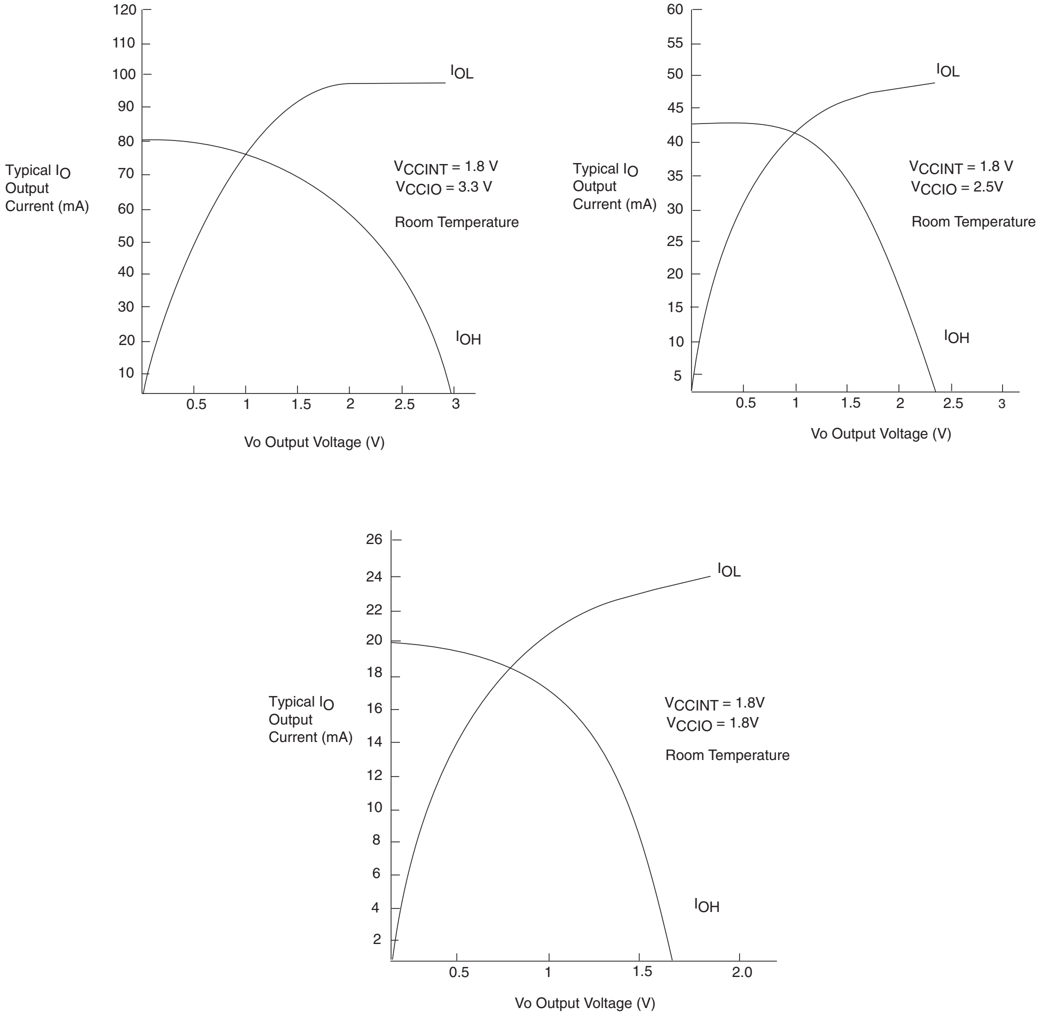
(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(11)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(11)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(11)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(11)*			0.7	V
I_I	Input pin leakage current	V_I = 5.75 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.75 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade *(12)*		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades *(12)*		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(13)*	20		50	W
		V_{CCIO} = 2.375 V *(13)*	30		80	W

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices Note (1)



Note to Figure 35:

(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Table 39. APEX 20KE External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{XZBIDIRPLL}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{ZXBIDIRPLL}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

Note to Tables 38 and 39:

(1) These timing parameters are sample-tested only.

Notes to Tables 43 through 48:
(1) This parameter is measured without using ClockLock or ClockBoost circuits.
(2) This parameter is measured using ClockLock or ClockBoost circuits.

Tables 49 through 54 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K30E APEX 20KE devices.

Table 49. EP20K30E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.02		0.02		ns
t_H	0.11		0.16		0.23		ns
t_{CO}		0.32		0.45		0.67	ns
t_{LUT}		0.85		1.20		1.77	ns

Table 76. EP20K200E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.44		2.65		ns
t_{CL}	1.36		2.44		2.65		ns
t_{CLRP}	0.18		0.19		0.21		ns
t_{PREP}	0.18		0.19		0.21		ns
t_{ESBCH}	1.36		2.44		2.65		ns
t_{ESBCL}	1.36		2.44		2.65		ns
t_{ESBWP}	1.18		1.48		1.76		ns
t_{ESBRP}	0.95		1.17		1.41		ns

Table 77. EP20K200E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.24		2.35		2.47		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{INSUPLL}$	2.13		2.07		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.01	0.50	3.36	-	-	ns

Table 78. EP20K200E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.81		3.19		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{XZBIDIR}$		7.51		8.32		8.67	ns
$t_{ZXBIDIR}$		7.51		8.32		8.67	ns
$t_{INSUBIDIRPLL}$	3.30		3.64		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{XZBIDIRPLL}$		5.40		6.05		-	ns
$t_{ZXBIDIRPLL}$		5.40		6.05		-	ns

Tables 79 through 84 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

Table 79. EP20K300E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.17		0.18		ns
t_H	0.31		0.33		0.38		ns
t_{CO}		0.28		0.38		0.51	ns
t_{LUT}		0.79		1.07		1.43	ns

Table 94. EP20K600E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.00		2.50		2.75		ns
t_{CL}	2.00		2.50		2.75		ns
t_{CLRP}	0.18		0.26		0.34		ns
t_{PREP}	0.18		0.26		0.34		ns
t_{ESBCH}	2.00		2.50		2.75		ns
t_{ESBCL}	2.00		2.50		2.75		ns
t_{ESBWP}	1.17		1.68		2.18		ns
t_{ESBRP}	0.95		1.35		1.76		ns

Table 95. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.74		2.74		2.87		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.51	2.00	6.06	2.00	6.61	ns
$t_{INSUPLL}$	1.86		1.96		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.62	0.50	2.91	-	-	ns

Table 96. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	0.64		0.98		1.08		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.51	2.00	6.06	2.00	6.61	ns
$t_{XZBIDIR}$		6.10		6.74		7.10	ns
$t_{ZXBIDIR}$		6.10		6.74		7.10	ns
$t_{INSUBIDIRPLL}$	2.26		2.68		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.62	0.50	2.91	-	-	ns
$t_{XZBIDIRPLL}$		3.21		3.59		-	ns
$t_{ZXBIDIRPLL}$		3.21		3.59		-	ns

Table 110. Selectable I/O Standard Output Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		–0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		–0.48		–0.48		–0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

Version 5.1

APEX 20K Programmable Logic Device Family Data Sheet version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

Version 5.0

APEX 20K Programmable Logic Device Family Data Sheet version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for $t_{ESBDATAH}$ parameter.

Version 4.3

APEX 20K Programmable Logic Device Family Data Sheet version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

Version 4.2

APEX 20K Programmable Logic Device Family Data Sheet version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.

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