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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1152
Number of Logic Elements/Cells	11520
Total RAM Bits	147456
Number of I/O	-
Number of Gates	728000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k300eqc208-2

Table 5. APEX 20K FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 *(3)*	
EP20K400E				488 *(3)*	
EP20K600E				508 *(3)*	588
EP20K1000E				508 *(3)*	708
EP20K1500E					808

Notes to Tables 4 and 5:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 7. APEX 20K FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

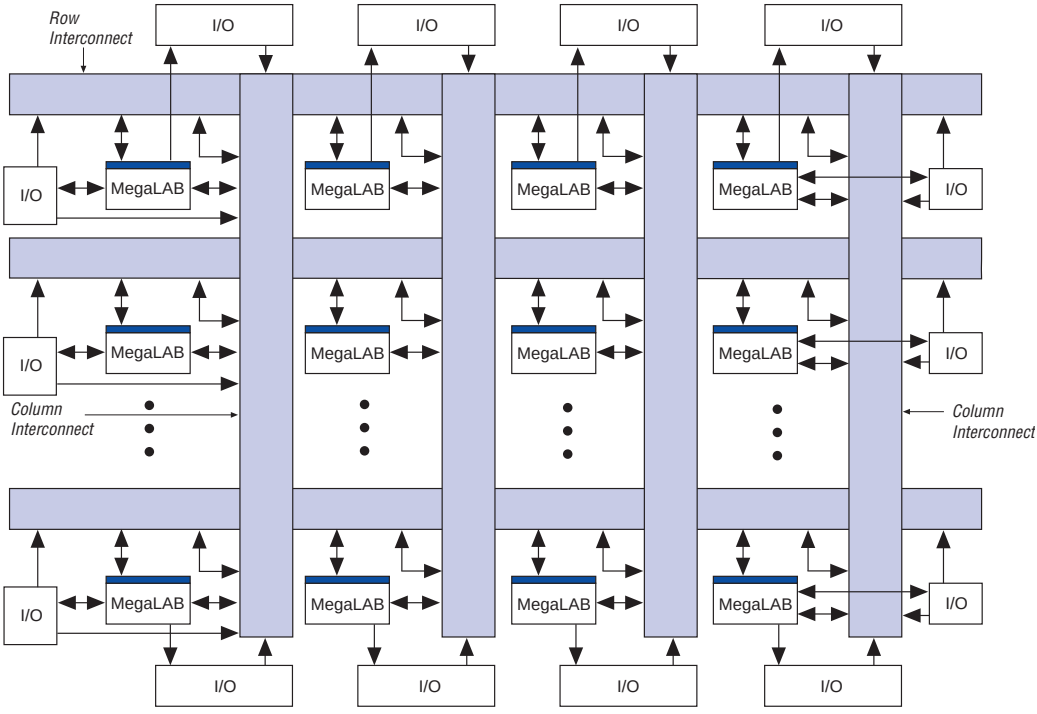
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX 20K Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Table 9. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin								✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ (1)				

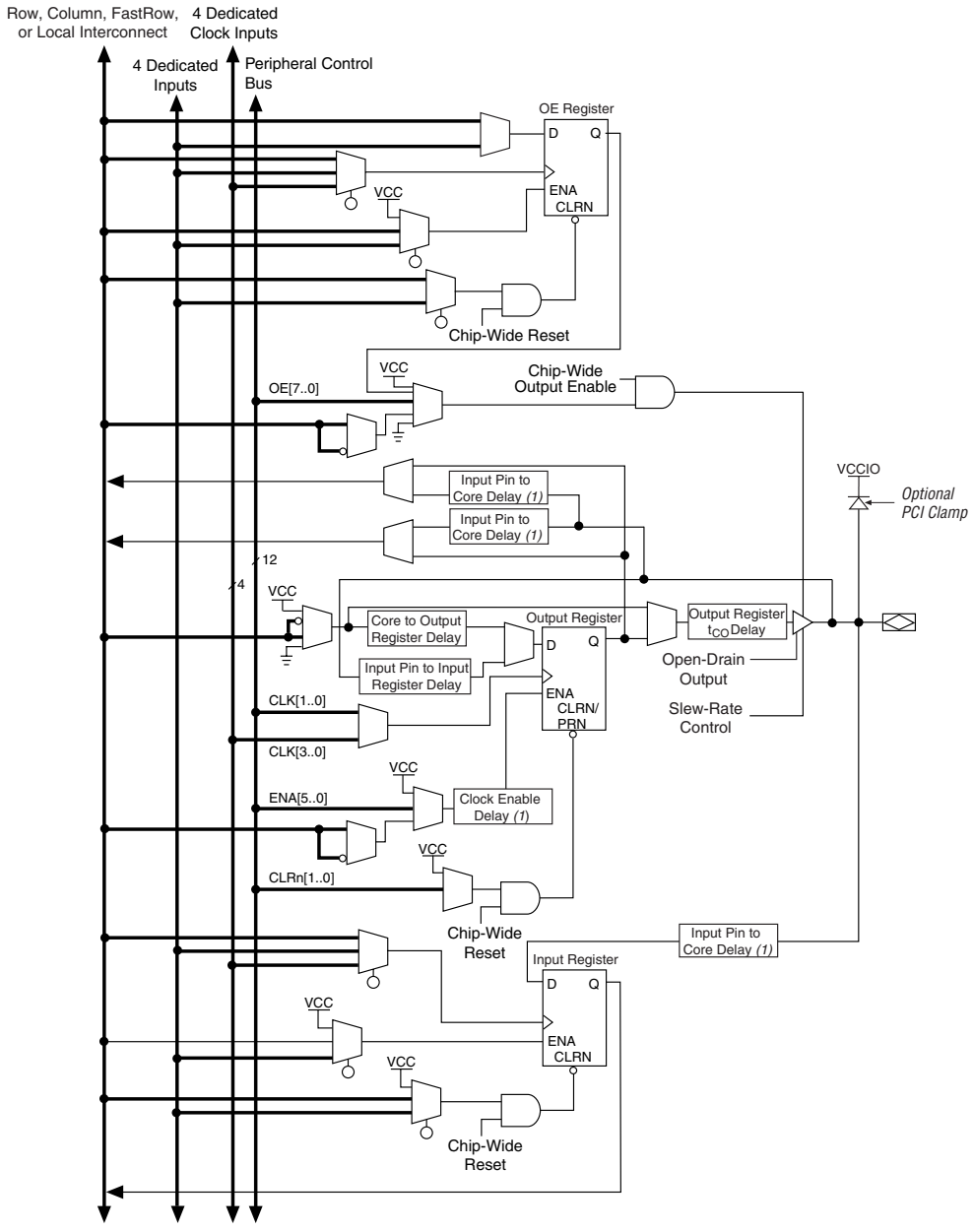
Note to Table 9:
(1) This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

Figure 26. APEX 20KE Bidirectional I/O Registers *Notes (1), (2)*



Notes to Figure 26:

(1) This programmable delay has four settings: off and three levels of delay.

(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

Notes to Table 12:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 *(1)*

Note to Table 20:
(1) This device does not support JTAG boundary scan testing.

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(11)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(11)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(11)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(11)*			0.7	V
I_I	Input pin leakage current	V_I = 5.75 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.75 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade *(12)*		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades *(12)*		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(13)*	20		50	W
		V_{CCIO} = 2.375 V *(13)*	30		80	W

Figure 37. APEX 20KE f_{MAX} Timing Model

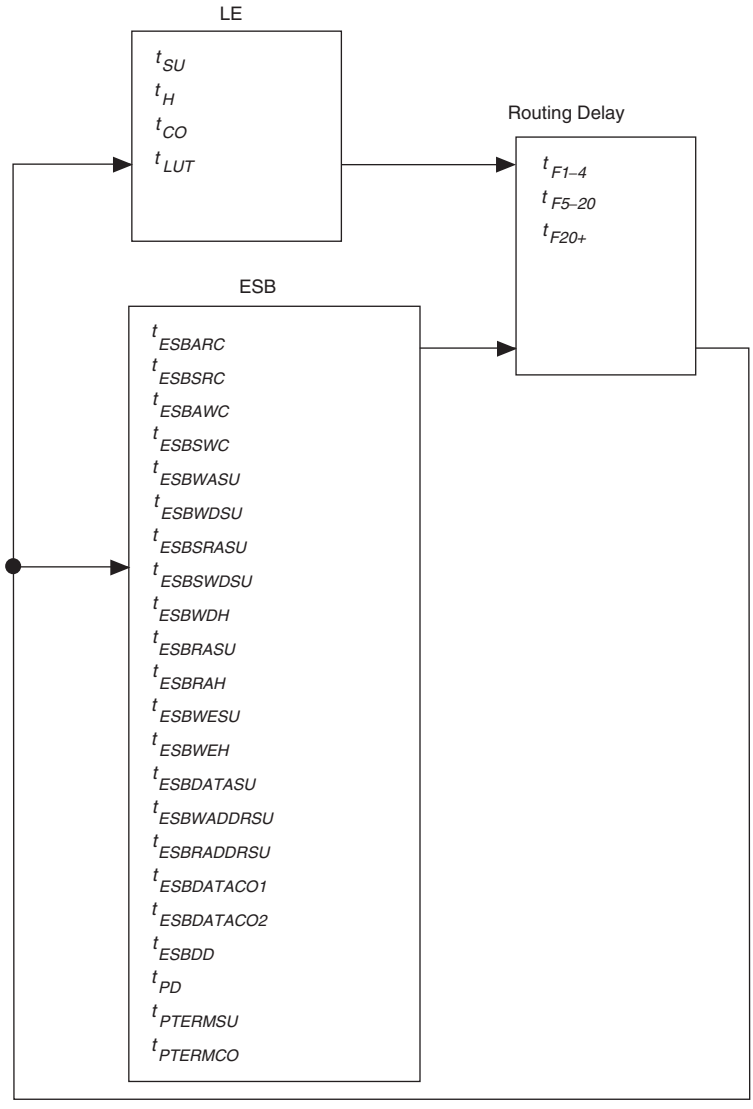


Table 41. EP20K200 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.4		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.3		2.8		3.2		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.3		2.8		3.2		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.0		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.9		2.3		2.6		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	–	ns

Table 50. EP20K30E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.03		2.86		4.24	ns
t_{ESBSRC}		2.58		3.49		5.02	ns
t_{ESBAWC}		3.88		5.45		8.08	ns
t_{ESBSWC}		4.08		5.35		7.48	ns
$t_{ESBWASU}$	1.77		2.49		3.68		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.95		2.74		4.05		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.96		2.75		4.07		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.80		2.73		4.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.48		1.17		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.30		0.80		1.64		ns
$t_{ESBRADDRSU}$	0.37		0.90		1.78		ns
$t_{ESBDATACO1}$		1.11		1.32		1.67	ns
$t_{ESBDATACO2}$		2.65		3.73		5.53	ns
t_{ESBDD}		3.88		5.45		8.08	ns
t_{PD}		1.91		2.69		3.98	ns
$t_{PTERMSU}$	1.04		1.71		2.82		ns
$t_{PTERMCO}$		1.13		1.34		1.69	ns

Table 51. EP20K30E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.31	ns
t_{F5-20}		1.03		1.14		1.30	ns
t_{F20+}		1.42		1.54		1.77	ns

Table 60. EP20K60E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.77		2.91		3.11		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{XZBIDIR}$		6.47		7.44		8.65	ns
$t_{ZXBIDIR}$		6.47		7.44		8.65	ns
$t_{INSUBIDIRPLL}$	3.44		3.24		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.37	0.50	3.69	-	-	ns
$t_{XZBIDIRPLL}$		5.00		5.82		-	ns
$t_{ZXBIDIRPLL}$		5.00		5.82		-	ns

Tables 61 through 66 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

Table 61. EP20K100E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.28		0.34	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 78. EP20K200E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.81		3.19		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{XZBIDIR}$		7.51		8.32		8.67	ns
$t_{ZXBIDIR}$		7.51		8.32		8.67	ns
$t_{INSUBIDIRPLL}$	3.30		3.64		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{XZBIDIRPLL}$		5.40		6.05		-	ns
$t_{ZXBIDIRPLL}$		5.40		6.05		-	ns

Tables 79 through 84 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

Table 79. EP20K300E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.17		0.18		ns
t_{H}	0.31		0.33		0.38		ns
t_{CO}		0.28		0.38		0.51	ns
t_{LUT}		0.79		1.07		1.43	ns

Table 90. EP20K400E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.93		3.23		3.44		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{XZBIDIR}$		5.95		6.77		7.12	ns
$t_{ZXBIDIR}$		5.95		6.77		7.12	ns
$t_{INSUBIDIRPLL}$	4.31		4.76		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.25	0.50	2.45	-	-	ns
$t_{XZBIDIRPLL}$		2.94		3.43		-	ns
$t_{ZXBIDIRPLL}$		2.94		3.43		-	ns

Tables 91 through 96 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K600E APEX 20KE devices.

Table 91. EP20K600E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.16		0.17		ns
t_{H}	0.29		0.33		0.37		ns
t_{CO}		0.65		0.38		0.49	ns
t_{LUT}		0.70		1.00		1.30	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.47		3.68		3.99		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{XZBIDIR}$		6.91		7.62		8.38	ns
$t_{ZXBIDIR}$		6.91		7.62		8.38	ns
$t_{INSUBIDIRPLL}$	3.05		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.67	0.50	2.99			ns
$t_{XZBIDIRPLL}$		3.41		3.80			ns
$t_{ZXBIDIRPLL}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		–0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		–0.24		–0.23		–0.19	ns
SSTL-3 Class I		–0.32		–0.21		–0.47	ns
SSTL-3 Class II		–0.08		0.03		–0.23	ns
SSTL-2 Class I		–0.17		–0.06		–0.32	ns
SSTL-2 Class II		–0.16		–0.05		–0.31	ns
LVDS		–0.12		–0.12		–0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 111. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information

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