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Understanding [Embedded - FPGAs (Field Programmable Gate Array)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	1152
Number of Logic Elements/Cells	11520
Total RAM Bits	147456
Number of I/O	-
Number of Gates	728000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k300erc208-2x

Table 2. Additional APEX 20K Device Features *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

Note to Tables 1 and 2:

(1)   The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

Additional Features

■ Designed for low-power operation
   – 1.8-V and 2.5-V supply voltage (see Table 3)
   – MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
   – ESB offering programmable power-saving mode

Table 3. APEX 20K Supply Voltages

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V$_{CCINT}$)	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V$_{CCIO}$)	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)*

Note to Table 3:

(1)   APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure

Row Interconnect

MegaLAB Interconnect

LEs drive local MegaLAB, row, and column interconnects.

To/From Adjacent LAB, ESB, or IOEs

To/From Adjacent LAB, ESB, or IOEs

Column Interconnect

Local Interconnect

The 10 LEs in the LAB are driven by two local interconnect areas. These LEs can drive two local interconnect areas.

Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element

Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.
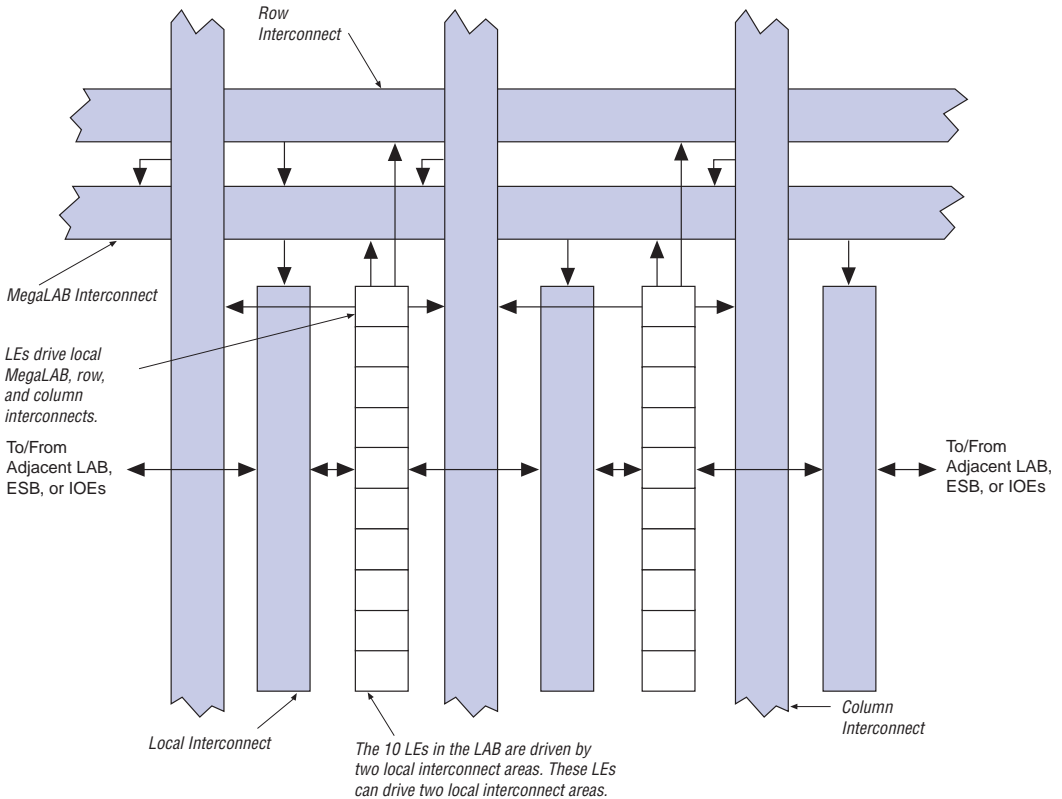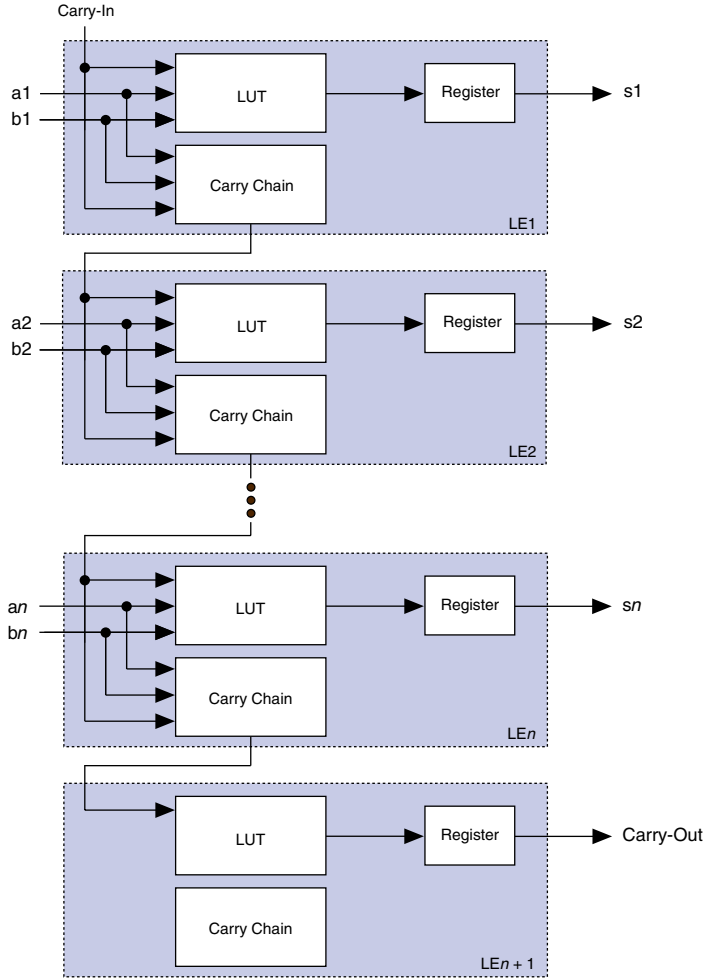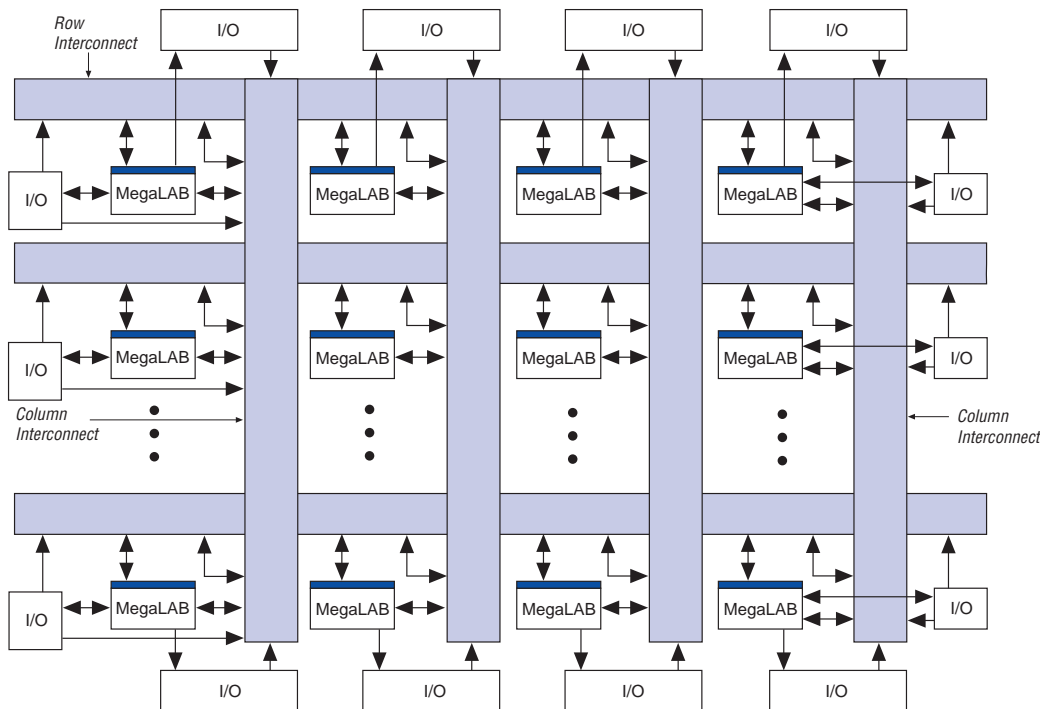
Figure 6. APEX 20K Carry Chain

Figure 9. APEX 20K Interconnect Structure

A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

Table 10. APEX 20K Programmable Delay Chains

Programmable Delays	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27 shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect

Any LE can drive a pin through the row, column, and MegaLAB interconnect.

Each IOE can drive local, MegaLAB, row, and column interconnect. Each IOE data and OE signal is driven by the local interconnect.

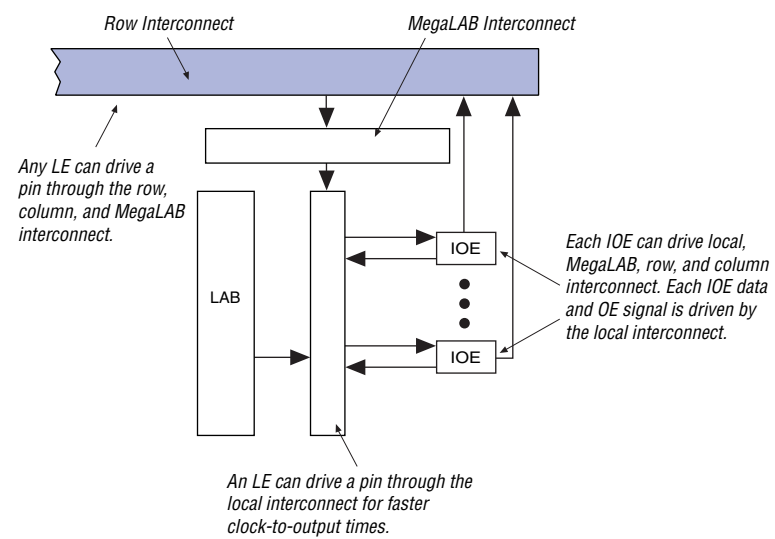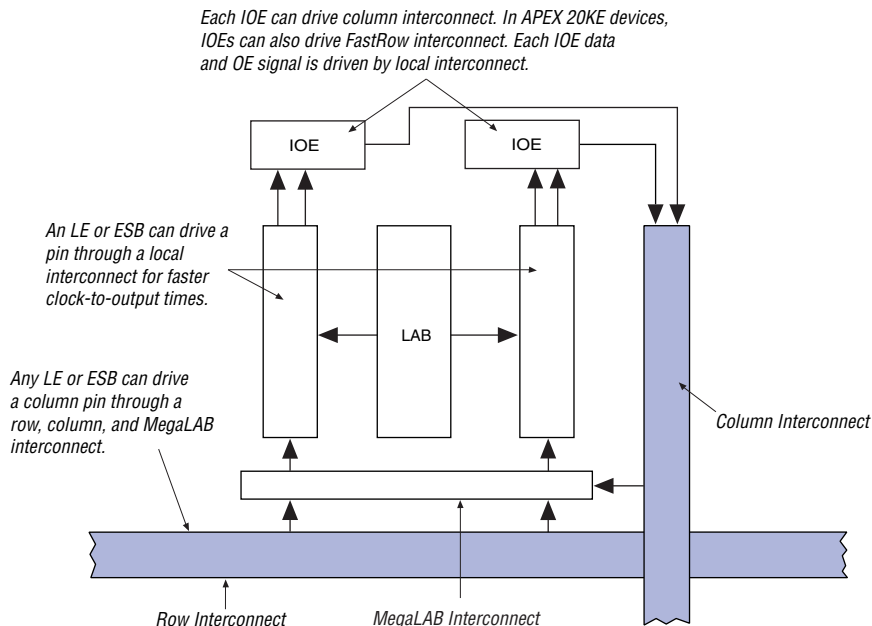*An LE can drive a pin through the local interconnect for faster clock-to-output times.*

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect

Each IOE can drive column interconnect. In APEX 20KE devices, IOEs can also drive FastRow interconnect. Each IOE data and OE signal is driven by local interconnect.

An LE or ESB can drive a pin through a local interconnect for faster clock-to-output times.

Any LE or ESB can drive a column pin through a row, column, and MegaLAB interconnect.

IOE

IOE

LAB

Column Interconnect

Row Interconnect

MegaLAB Interconnect

Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock (5)		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:
(1)   The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2)   All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3)   During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4)   The jitter specification is measured under long-term observation.
(5)   If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) (1)		25,000 (2)	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock (3)		10	µs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock (4)		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Table 18. APEX 20KE Clock Input & Output Parameters *(Part 1 of 2)* *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f$_{VCO}$ *(4)*	Voltage controlled oscillator operating range		200	500	200	500	MHz
f$_{CLOCK0}$	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f$_{CLOCK1}$	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f$_{CLOCK0\_EXT}$	Output clock frequency for external clock0 output	3.3-V LVTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
f$_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTL	20	245	20	226	MHz
		2.5-V LVTTL	20	234	20	221	MHz
		1.8-V LVTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the f_{MAX} timing model for APEX 20K devices.

Figure 36. APEX 20K f_{MAX} Timing Model

LE

t_{SU}
t_H
t_{CO}
t_{LUT}

Routing Delay

$t_{F1—4}$
$t_{F5—20}$
t_{F20+}

ESB

t_{ESBRC}
t_{ESBWC}
$t_{ESBWESU}$
$t_{ESBDATASU}$
$t_{ESBADDRSU}$
$t_{ESBDATACO1}$
$t_{ESBDATACO2}$
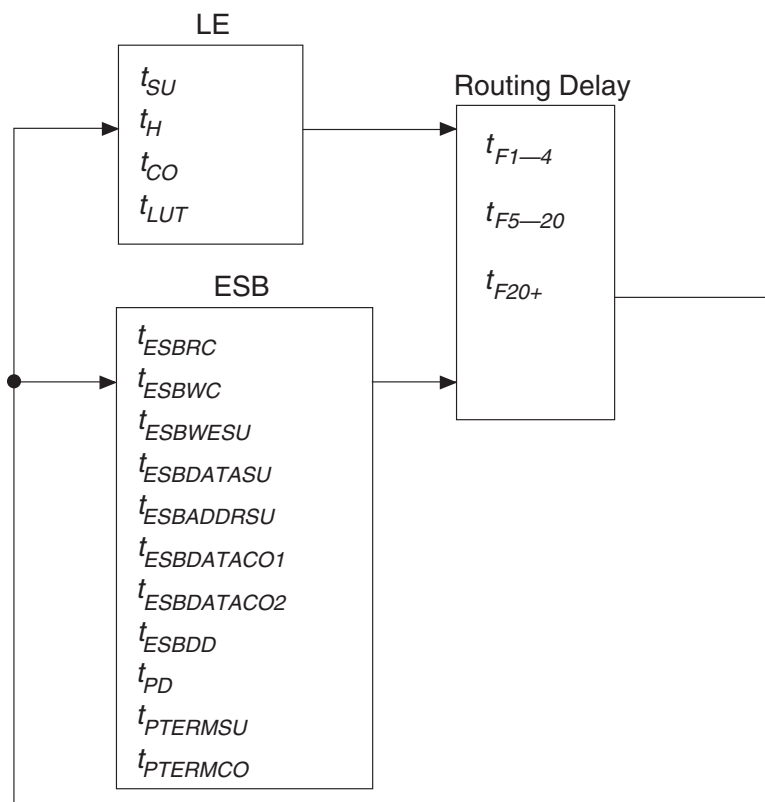t_{ESBDD}
t_{PD}
$t_{PTERMSU}$
$t_{PTERMCO}$

Figure 37 shows the f_{MAX} timing model for APEX 20KE devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Table 31. APEX 20K f_{MAX} Timing Parameters (Part 2 of 2)

Symbol	Parameter
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
t_{F1-4}	Fanout delay using local interconnect
t_{F5-20}	Fanout delay using MegaLab Interconnect
t_{F20+}	Fanout delay using FastTrack Interconnect
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

Table 32. APEX 20K External Timing Parameters   Note (1)

Symbol	Clock Parameter
t_{INSU}	Setup time with global clock at IOE register
t_{INH}	Hold time with global clock at IOE register
t_{OUTCO}	Clock-to-output delay with global clock at IOE register

Table 33. APEX 20K External Bidirectional Timing Parameters   Note (1)

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF

Table 36. APEX 20KE Routing Timing Microparameters *Note (1)*

Symbol	Parameter
t_{F1-4}	Fanout delay using Local Interconnect
t_{F5-20}	Fanout delay estimate using MegaLab Interconnect
t_{F20+}	Fanout delay estimate using FastTrack Interconnect

Note to Table 36:
(1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 37. APEX 20KE Functional Timing Microparameters

Symbol	Parameter
TCH	Minimum clock high time from clock pin
TCL	Minimum clock low time from clock pin
TCLRP	LE clear Pulse Width
TPREP	LE preset pulse width
TESBCH	Clock high time for ESB
TESBCL	Clock low time for ESB
TESBWP	Write pulse width
TESBRP	Read pulse width

Tables 38 and 39 describe the APEX 20KE external timing parameters.

Table 38. APEX 20KE External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF

Table 41. EP20K200 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_H	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.4		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 69. EP20K160E f$_{MAX}$ Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.25		0.26		0.28	ns
t$_{F5-20}$		1.00		1.18		1.35	ns
t$_{F20+}$		1.95		2.19		2.30	ns

Table 70. EP20K160E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{CH}$	1.34		1.43		1.55		ns
t$_{CL}$	1.34		1.43		1.55		ns
t$_{CLRP}$	0.18		0.19		0.21		ns
t$_{PREP}$	0.18		0.19		0.21		ns
t$_{ESBCH}$	1.34		1.43		1.55		ns
t$_{ESBCL}$	1.34		1.43		1.55		ns
t$_{ESBWP}$	1.15		1.45		1.73		ns
t$_{ESBRP}$	0.93		1.15		1.38		ns

Table 71. EP20K160E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSU}$	2.23		2.34		2.47		ns
t$_{INH}$	0.00		0.00		0.00		ns
t$_{OUTCO}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
t$_{INSUPLL}$	2.12		2.07		-		ns
t$_{INHPLL}$	0.00		0.00		-		ns
t$_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns

Table 80. EP20K300E f$_{MAX}$ ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{ESBARC}$		1.79		2.44		3.25	ns
t$_{ESBSRC}$		2.40		3.12		4.01	ns
t$_{ESBAWC}$		3.41		4.65		6.20	ns
t$_{ESBSWC}$		3.68		4.68		5.93	ns
t$_{ESBWASU}$	1.55		2.12		2.83		ns
t$_{ESBWAH}$	0.00		0.00		0.00		ns
t$_{ESBWDSU}$	1.71		2.33		3.11		ns
t$_{ESBWDH}$	0.00		0.00		0.00		ns
t$_{ESBRASU}$	1.72		2.34		3.13		ns
t$_{ESBRAH}$	0.00		0.00		0.00		ns
t$_{ESBWESU}$	1.63		2.36		3.28		ns
t$_{ESBWEH}$	0.00		0.00		0.00		ns
t$_{ESBDATASU}$	0.07		0.39		0.80		ns
t$_{ESBDATAH}$	0.13		0.13		0.13		ns
t$_{ESBWADDRSU}$	0.27		0.67		1.17		ns
t$_{ESBRADDRSU}$	0.34		0.75		1.28		ns
t$_{ESBDATACO1}$		1.03		1.20		1.40	ns
t$_{ESBDATACO2}$		2.33		3.18		4.24	ns
t$_{ESBDD}$		3.41		4.65		6.20	ns
t$_{PD}$		1.68		2.29		3.06	ns
t$_{PTERMSU}$	0.96		1.48		2.14		ns
t$_{PTERMCO}$		1.05		1.22		1.42	ns

Table 81. EP20K300E f$_{MAX}$ Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.22		0.24		0.26	ns
t$_{F5-20}$		1.33		1.43		1.58	ns
t$_{F20+}$		3.63		3.93		4.35	ns

Table 98. EP20K1000E f_MAX ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_ESBARC		1.78		2.02		1.95	ns
t_ESBSRC		2.52		2.91		3.14	ns
t_ESBAWC		3.52		4.11		4.40	ns
t_ESBSWC		3.23		3.84		4.16	ns
t_ESBWASU	0.62		0.67		0.61		ns
t_ESBWAH	0.41		0.55		0.55		ns
t_ESBWDSU	0.77		0.79		0.81		ns
t_ESBWDH	0.41		0.55		0.55		ns
t_ESBRASU	1.74		1.92		1.85		ns
t_ESBRAH	0.00		0.01		0.23		ns
t_ESBWESU	2.07		2.28		2.41		ns
t_ESBWEH	0.00		0.00		0.00		ns
t_ESBDATASU	0.25		0.27		0.29		ns
t_ESBDATAH	0.13		0.13		0.13		ns
t_ESBWADDRSU	0.11		0.04		0.11		ns
t_ESBRADDRSU	0.14		0.11		0.16		ns
t_ESBDATACO1		1.29		1.50		1.63	ns
t_ESBDATACO2		2.55		2.99		3.22	ns
t_ESBDD		3.12		3.57		3.85	ns
t_PD		1.84		2.13		2.32	ns
t_PTERMSU	1.08		1.19		1.32		ns
t_PTERMCO		1.31		1.53		1.66	ns

Table 110. Selectable I/O Standard Output Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		−0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		−0.48		−0.48		−0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 111. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the *Altera Digital Library* for pin-out information

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.