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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                     |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                            |
| Number of LABs/CLBs            | 120                                                                                                                                 |
| Number of Logic Elements/Cells | 1200                                                                                                                                |
| Total RAM Bits                 | 24576                                                                                                                               |
| Number of I/O                  | 93                                                                                                                                  |
| Number of Gates                | 113000                                                                                                                              |
| Voltage - Supply               | 1.71V ~ 1.89V                                                                                                                       |
| Mounting Type                  | Surface Mount                                                                                                                       |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                     |
| Package / Case                 | 144-BGA                                                                                                                             |
| Supplier Device Package        | 144-FBGA (13x13)                                                                                                                    |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/ep20k30efc144-2">https://www.e-xfl.com/product-detail/intel/ep20k30efc144-2</a> |

**Table 2. Additional APEX 20K Device Features** *Note (1)*

| Feature               | EP20K300E | EP20K400  | EP20K400E | EP20K600E | EP20K1000E | EP20K1500E |
|-----------------------|-----------|-----------|-----------|-----------|------------|------------|
| Maximum system gates  | 728,000   | 1,052,000 | 1,052,000 | 1,537,000 | 1,772,000  | 2,392,000  |
| Typical gates         | 300,000   | 400,000   | 400,000   | 600,000   | 1,000,000  | 1,500,000  |
| LEs                   | 11,520    | 16,640    | 16,640    | 24,320    | 38,400     | 51,840     |
| ESBs                  | 72        | 104       | 104       | 152       | 160        | 216        |
| Maximum RAM bits      | 147,456   | 212,992   | 212,992   | 311,296   | 327,680    | 442,368    |
| Maximum macrocells    | 1,152     | 1,664     | 1,664     | 2,432     | 2,560      | 3,456      |
| Maximum user I/O pins | 408       | 502       | 488       | 588       | 708        | 808        |

*Note to Tables 1 and 2:*

- (1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

**Table 3. APEX 20K Supply Voltages**

| Feature                                               | Device                           |                                                                                                                                |
|-------------------------------------------------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------|
|                                                       | EP20K100<br>EP20K200<br>EP20K400 | EP20K30E<br>EP20K60E<br>EP20K100E<br>EP20K160E<br>EP20K200E<br>EP20K300E<br>EP20K400E<br>EP20K600E<br>EP20K1000E<br>EP20K1500E |
| Internal supply voltage ( $V_{CCINT}$ )               | 2.5 V                            | 1.8 V                                                                                                                          |
| MultiVolt I/O interface voltage levels ( $V_{CCIO}$ ) | 2.5 V, 3.3 V, 5.0 V              | 1.8 V, 2.5 V, 3.3 V, 5.0 V (1)                                                                                                 |

*Note to Table 3:*

- (1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

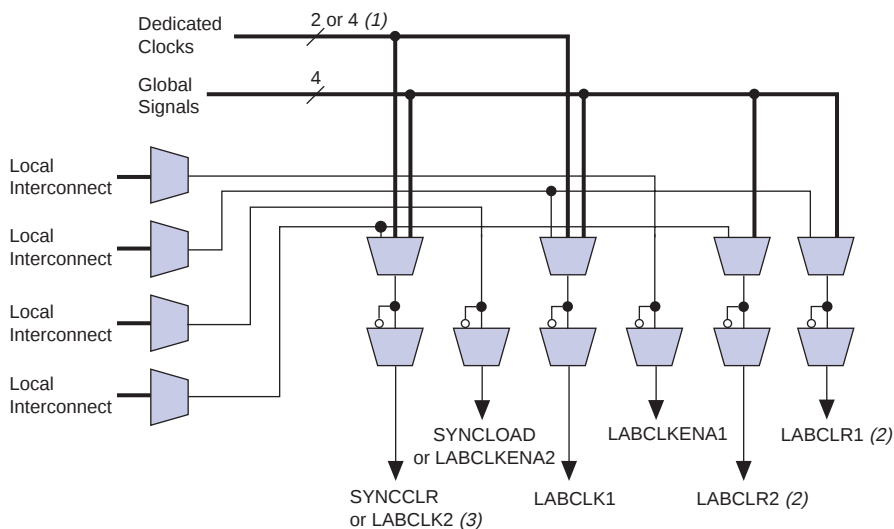
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. **Figure 4** shows the LAB control signal generation circuit.

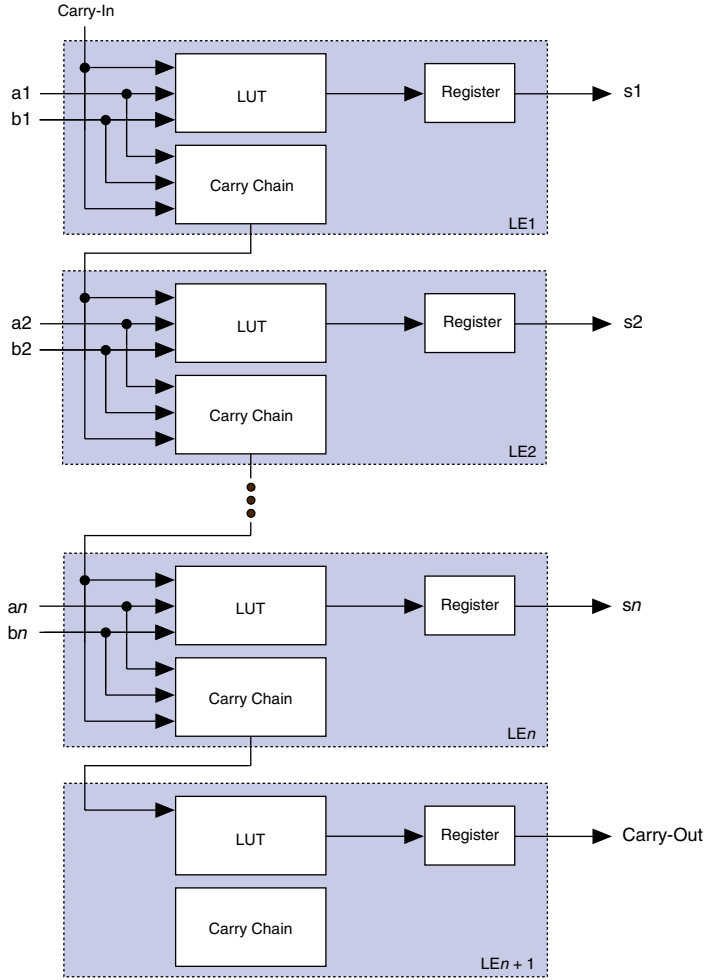
**Figure 4. LAB Control Signal Generation**



**Notes to Figure 4:**

- (1) APEX 20KE devices have four dedicated clocks.
- (2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
- (3) The SYNCLD signal can be generated by the local interconnect or global signals.

Figure 6. APEX 20K Carry Chain



### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

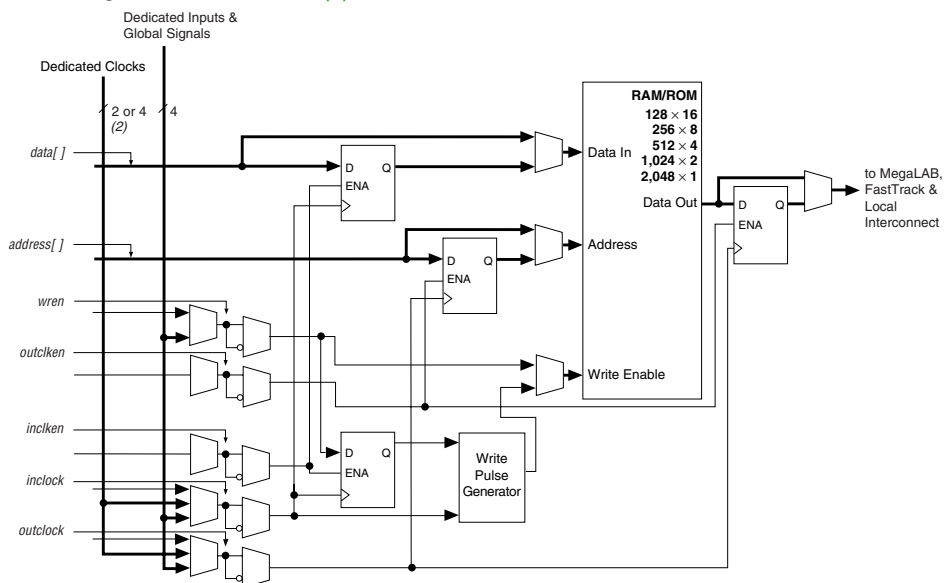
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

**Figure 22. ESB in Single-Port Mode** *Note (1)*



Notes to **Figure 22:**

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. [Figure 23](#) shows the CAM block diagram.

**Figure 23. APEX 20KE CAM Block Diagram**

CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

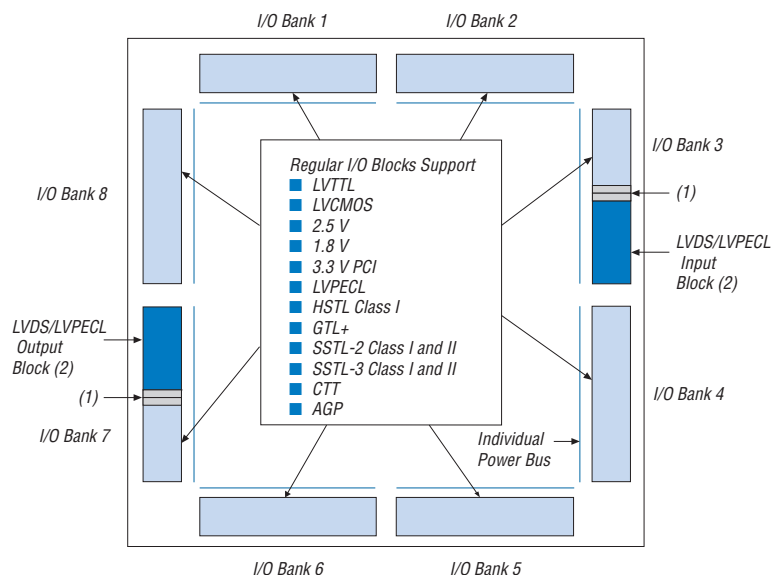
When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing “don’t care” bits into words of the memory. The “don’t-care” bit can be used as a mask for CAM comparisons; any bit set to “don’t-care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t-care” bits are used, a third clock cycle is required.

**Figure 29. APEX 20KE I/O Banks**

**Notes to Figure 29:**

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with  $V_{CCIO}$  set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the  $V_{CCIO}$  and  $V_{CCINT}$  power supplies may be powered in any order.



For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

## MultiVolt I/O Interface

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V VCCINT level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

| <b>Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support</b> |                          |            |            |                           |            |            |
|----------------------------------------------------------------|--------------------------|------------|------------|---------------------------|------------|------------|
| <b>V<sub>CCIO</sub> (V)</b>                                    | <b>Input Signals (V)</b> |            |            | <b>Output Signals (V)</b> |            |            |
|                                                                | <b>2.5</b>               | <b>3.3</b> | <b>5.0</b> | <b>2.5</b>                | <b>3.3</b> | <b>5.0</b> |
| 2.5                                                            | ✓                        | ✓(1)       | ✓(1)       | ✓                         |            |            |
| 3.3                                                            | ✓                        | ✓          | ✓(1)       | ✓(2)                      | ✓          | ✓          |

**Notes to Table 12:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V<sub>CCIO</sub>.
- (2) When V<sub>CCIO</sub> = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V<sub>IH</sub> of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I<sub>OL</sub> current specification should be considered when selecting a pull-up resistor.

### *Clock Phase & Delay Adjustment*

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

### *LVDS Support*

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

### *Lock Signals*

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

## **ClockLock & ClockBoost Timing Parameters**

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. [Figure 30](#) shows the incoming and generated clock specifications.



For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in [Table 19](#). Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

**Table 19. APEX 20K JTAG Instructions**

| JTAG Instruction           | Description                                                                                                                                                                                                                          |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SAMPLE/PRELOAD             | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer. |
| EXTEST                     | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.                                                               |
| BYPASS (1)                 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.                                          |
| USERCODE                   | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.                                                                                            |
| IDCODE                     | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.                                                                                                                |
| ICR Instructions           | Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.                                         |
| SignalTap Instructions (1) | Monitors internal device operation with the SignalTap embedded logic analyzer.                                                                                                                                                       |

**Note to Table 19:**

(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)** *Notes (2), (7), (8)*

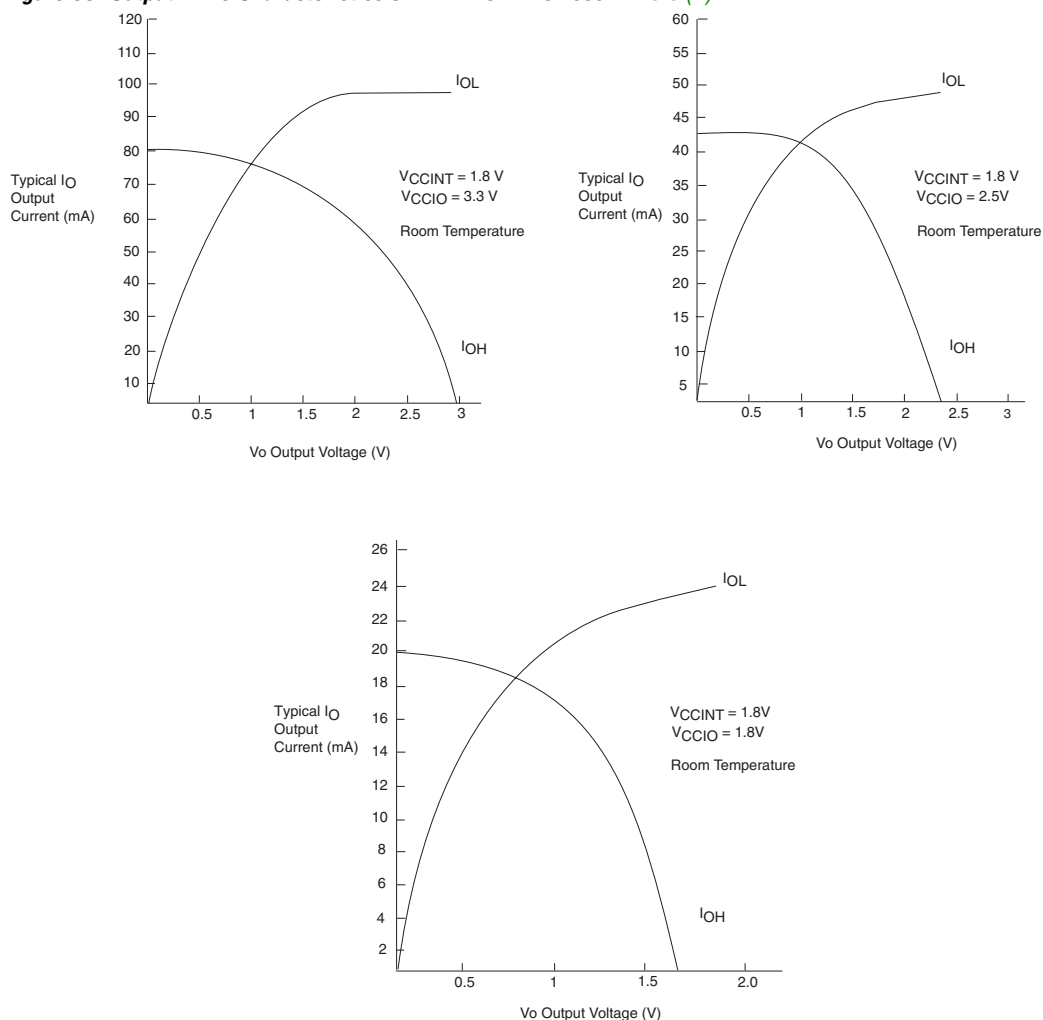
| Symbol     | Parameter                                                            | Conditions                                                                          | Min | Typ | Max                   | Unit          |
|------------|----------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----|-----|-----------------------|---------------|
| $V_{OL}$   | 3.3-V low-level TTL output voltage                                   | $I_{OL} = 12 \text{ mA DC}$ ,<br>$V_{CCIO} = 3.00 \text{ V}$ (11)                   |     |     | 0.45                  | V             |
|            | 3.3-V low-level CMOS output voltage                                  | $I_{OL} = 0.1 \text{ mA DC}$ ,<br>$V_{CCIO} = 3.00 \text{ V}$ (11)                  |     |     | 0.2                   | V             |
|            | 3.3-V low-level PCI output voltage                                   | $I_{OL} = 1.5 \text{ mA DC}$ ,<br>$V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (11) |     |     | $0.1 \times V_{CCIO}$ | V             |
|            | 2.5-V low-level output voltage                                       | $I_{OL} = 0.1 \text{ mA DC}$ ,<br>$V_{CCIO} = 2.30 \text{ V}$ (11)                  |     |     | 0.2                   | V             |
|            |                                                                      | $I_{OL} = 1 \text{ mA DC}$ ,<br>$V_{CCIO} = 2.30 \text{ V}$ (11)                    |     |     | 0.4                   | V             |
|            |                                                                      | $I_{OL} = 2 \text{ mA DC}$ ,<br>$V_{CCIO} = 2.30 \text{ V}$ (11)                    |     |     | 0.7                   | V             |
| $I_I$      | Input pin leakage current                                            | $V_I = 5.75 \text{ to } -0.5 \text{ V}$                                             | -10 |     | 10                    | $\mu\text{A}$ |
| $I_{OZ}$   | Tri-stated I/O pin leakage current                                   | $V_O = 5.75 \text{ to } -0.5 \text{ V}$                                             | -10 |     | 10                    | $\mu\text{A}$ |
| $I_{CC0}$  | $V_{CC}$ supply current (standby)<br>(All ESBs in power-down mode)   | $V_I = \text{ground}$ , no load, no<br>toggling inputs, -1 speed<br>grade (12)      |     | 10  |                       | mA            |
|            |                                                                      | $V_I = \text{ground}$ , no load, no<br>toggling inputs,<br>-2, -3 speed grades (12) |     | 5   |                       | mA            |
| $R_{CONF}$ | Value of I/O pin pull-up resistor<br>before and during configuration | $V_{CCIO} = 3.0 \text{ V}$ (13)                                                     | 20  |     | 50                    | W             |
|            |                                                                      | $V_{CCIO} = 2.375 \text{ V}$ (13)                                                   | 30  |     | 80                    | W             |

**Table 28. APEX 20KE Device Recommended Operating Conditions**

| Symbol      | Parameter                                           | Conditions         | Min           | Max           | Unit |
|-------------|-----------------------------------------------------|--------------------|---------------|---------------|------|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | (3), (4)           | 1.71 (1.71)   | 1.89 (1.89)   | V    |
| $V_{CCIO}$  | Supply voltage for output buffers, 3.3-V operation  | (3), (4)           | 3.00 (3.00)   | 3.60 (3.60)   | V    |
|             | Supply voltage for output buffers, 2.5-V operation  | (3), (4)           | 2.375 (2.375) | 2.625 (2.625) | V    |
|             | Supply voltage for output buffers, 1.8-V operation  | (3), (4)           | 1.71 (1.71)   | 1.89 (1.89)   | V    |
| $V_I$       | Input voltage                                       | (5), (6)           | −0.5          | 4.0           | V    |
| $V_O$       | Output voltage                                      |                    | 0             | $V_{CCIO}$    | V    |
| $T_J$       | Junction temperature                                | For commercial use | 0             | 85            | °C   |
|             |                                                     | For industrial use | −40           | 100           | °C   |
| $t_R$       | Input rise time                                     |                    |               | 40            | ns   |
| $t_F$       | Input fall time                                     |                    |               | 40            | ns   |

Figure 35 shows the output drive characteristics of APEX 20KE devices.

**Figure 35. Output Drive Characteristics of APEX 20KE Devices** *Note (1)*



**Note to Figure 35:**

(1) These are transient (AC) currents.

## Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

**Table 31. APEX 20K  $t_{MAX}$  Timing Parameters (Part 2 of 2)**

| Symbol                  | Parameter                                          |
|-------------------------|----------------------------------------------------|
| $t_{ESB\text{DATA}CO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$             | ESB data-in to data-out delay for RAM mode         |
| $t_{PD}$                | ESB macrocell input to non-registered output       |
| $t_{PTERMSU}$           | ESB macrocell register setup time before clock     |
| $t_{PTERMCO}$           | ESB macrocell register clock-to-output delay       |
| $t_{F1-4}$              | Fanout delay using local interconnect              |
| $t_{F5-20}$             | Fanout delay using MegaLab Interconnect            |
| $t_{F20+}$              | Fanout delay using FastTrack Interconnect          |
| $t_{CH}$                | Minimum clock high time from clock pin             |
| $t_{CL}$                | Minimum clock low time from clock pin              |
| $t_{CLRP}$              | LE clear pulse width                               |
| $t_{PREP}$              | LE preset pulse width                              |
| $t_{ESBCH}$             | Clock high time                                    |
| $t_{ESBCL}$             | Clock low time                                     |
| $t_{ESBWP}$             | Write pulse width                                  |
| $t_{ESBRP}$             | Read pulse width                                   |

Tables 32 and 33 describe APEX 20K external timing parameters.

**Table 32. APEX 20K External Timing Parameters Note (1)**

| Symbol      | Clock Parameter                                         |
|-------------|---------------------------------------------------------|
| $t_{INSU}$  | Setup time with global clock at IOE register            |
| $t_{INH}$   | Hold time with global clock at IOE register             |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register |

**Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)**

| Symbol                  | Parameter                                                                                  | Conditions |
|-------------------------|--------------------------------------------------------------------------------------------|------------|
| $t_{INSUBIDIR}$         | Setup time for bidirectional pins with global clock at same-row or same-column LE register |            |
| $t_{INH\text{BIDIR}}$   | Hold time for bidirectional pins with global clock at same-row or same-column LE register  |            |
| $t_{OUTCO\text{BIDIR}}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register             | C1 = 10 pF |
| $t_{XZ\text{BIDIR}}$    | Synchronous IOE output buffer disable delay                                                | C1 = 10 pF |
| $t_{ZXBIDIR}$           | Synchronous IOE output buffer enable delay, slow slew rate = off                           | C1 = 10 pF |

**Table 36. APEX 20KE Routing Timing Microparameters** *Note (1)*

| Symbol      | Parameter                                          |
|-------------|----------------------------------------------------|
| $t_{F1-4}$  | Fanout delay using Local Interconnect              |
| $t_{F5-20}$ | Fanout delay estimate using MegaLab Interconnect   |
| $t_{F20+}$  | Fanout delay estimate using FastTrack Interconnect |

*Note to Table 36:*

- (1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

**Table 37. APEX 20KE Functional Timing Microparameters**

| Symbol | Parameter                              |
|--------|----------------------------------------|
| TCH    | Minimum clock high time from clock pin |
| TCL    | Minimum clock low time from clock pin  |
| TCLRP  | LE clear Pulse Width                   |
| TPREP  | LE preset pulse width                  |
| TESBCH | Clock high time for ESB                |
| TESBCL | Clock low time for ESB                 |
| TESBWP | Write pulse width                      |
| TESBRP | Read pulse width                       |

Tables 38 and 39 describe the APEX 20KE external timing parameters.

**Table 38. APEX 20KE External Timing Parameters** *Note (1)*

| Symbol         | Clock Parameter                                                | Conditions |
|----------------|----------------------------------------------------------------|------------|
| $t_{INSU}$     | Setup time with global clock at IOE input register             |            |
| $t_{INH}$      | Hold time with global clock at IOE input register              |            |
| $t_{OUTCO}$    | Clock-to-output delay with global clock at IOE output register | C1 = 10 pF |
| $t_{INSUPLL}$  | Setup time with PLL clock at IOE input register                |            |
| $t_{INHPLL}$   | Hold time with PLL clock at IOE input register                 |            |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register    | C1 = 10 pF |

Tables 40 through 42 show the  $f_{\text{MAX}}$  timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 40. EP20K100  $f_{\text{MAX}}$  Timing Parameters**

| Symbol                  | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Units |
|-------------------------|----------------|-----|----------------|-----|----------------|-----|-------|
|                         | Min            | Max | Min            | Max | Min            | Max |       |
| $t_{\text{SU}}$         | 0.5            |     | 0.6            |     | 0.8            |     | ns    |
| $t_{\text{H}}$          | 0.7            |     | 0.8            |     | 1.0            |     | ns    |
| $t_{\text{CO}}$         |                | 0.3 |                | 0.4 |                | 0.5 | ns    |
| $t_{\text{LUT}}$        |                | 0.8 |                | 1.0 |                | 1.3 | ns    |
| $t_{\text{ESBRC}}$      |                | 1.7 |                | 2.1 |                | 2.4 | ns    |
| $t_{\text{ESBWC}}$      |                | 5.7 |                | 6.9 |                | 8.1 | ns    |
| $t_{\text{ESBWESU}}$    | 3.3            |     | 3.9            |     | 4.6            |     | ns    |
| $t_{\text{ESBDATASU}}$  | 2.2            |     | 2.7            |     | 3.1            |     | ns    |
| $t_{\text{ESBDATAH}}$   | 0.6            |     | 0.8            |     | 0.9            |     | ns    |
| $t_{\text{ESBADDRSU}}$  | 2.4            |     | 2.9            |     | 3.3            |     | ns    |
| $t_{\text{ESBDATACO1}}$ |                | 1.3 |                | 1.6 |                | 1.8 | ns    |
| $t_{\text{ESBDATACO2}}$ |                | 2.6 |                | 3.1 |                | 3.6 | ns    |
| $t_{\text{ESBDD}}$      |                | 2.5 |                | 3.3 |                | 3.6 | ns    |
| $t_{\text{PD}}$         |                | 2.5 |                | 3.0 |                | 3.6 | ns    |
| $t_{\text{PTERMSU}}$    | 2.3            |     | 2.6            |     | 3.2            |     | ns    |
| $t_{\text{PTERMCO}}$    |                | 1.5 |                | 1.8 |                | 2.1 | ns    |
| $t_{\text{F1-4}}$       |                | 0.5 |                | 0.6 |                | 0.7 | ns    |
| $t_{\text{F5-20}}$      |                | 1.6 |                | 1.7 |                | 1.8 | ns    |
| $t_{\text{F20+}}$       |                | 2.2 |                | 2.2 |                | 2.3 | ns    |
| $t_{\text{CH}}$         | 2.0            |     | 2.5            |     | 3.0            |     | ns    |
| $t_{\text{CL}}$         | 2.0            |     | 2.5            |     | 3.0            |     | ns    |
| $t_{\text{CLRP}}$       | 0.3            |     | 0.4            |     | 0.4            |     | ns    |
| $t_{\text{PREP}}$       | 0.5            |     | 0.5            |     | 0.5            |     | ns    |
| $t_{\text{ESBCH}}$      | 2.0            |     | 2.5            |     | 3.0            |     | ns    |
| $t_{\text{ESBCL}}$      | 2.0            |     | 2.5            |     | 3.0            |     | ns    |
| $t_{\text{ESBWP}}$      | 1.6            |     | 1.9            |     | 2.2            |     | ns    |
| $t_{\text{ESBRP}}$      | 1.0            |     | 1.3            |     | 1.4            |     | ns    |

**Table 68. EP20K160E  $t_{MAX}$  ESB Timing Microparameters**

| Symbol           | -1    |      | -2    |      | -3   |      | Unit |
|------------------|-------|------|-------|------|------|------|------|
|                  | Min   | Max  | Min   | Max  | Min  | Max  |      |
| $t_{ESBARC}$     |       | 1.65 |       | 2.02 |      | 2.11 | ns   |
| $t_{ESBSRC}$     |       | 2.21 |       | 2.70 |      | 3.11 | ns   |
| $t_{ESBAWC}$     |       | 3.04 |       | 3.79 |      | 4.42 | ns   |
| $t_{ESBSWC}$     |       | 2.81 |       | 3.56 |      | 4.10 | ns   |
| $t_{ESBWASU}$    | 0.54  |      | 0.66  |      | 0.73 |      | ns   |
| $t_{ESBWAH}$     | 0.36  |      | 0.45  |      | 0.47 |      | ns   |
| $t_{ESBWDSU}$    | 0.68  |      | 0.81  |      | 0.94 |      | ns   |
| $t_{ESBWDH}$     | 0.36  |      | 0.45  |      | 0.47 |      | ns   |
| $t_{ESBRASU}$    | 1.58  |      | 1.87  |      | 2.06 |      | ns   |
| $t_{ESBRAH}$     | 0.00  |      | 0.00  |      | 0.01 |      | ns   |
| $t_{ESBWESU}$    | 1.41  |      | 1.71  |      | 2.00 |      | ns   |
| $t_{ESBWEH}$     | 0.00  |      | 0.00  |      | 0.00 |      | ns   |
| $t_{ESBDATASU}$  | -0.02 |      | -0.03 |      | 0.09 |      | ns   |
| $t_{ESBDATAH}$   | 0.13  |      | 0.13  |      | 0.13 |      | ns   |
| $t_{ESBWADDRSU}$ | 0.14  |      | 0.17  |      | 0.35 |      | ns   |
| $t_{ESBRADDRSU}$ | 0.21  |      | 0.27  |      | 0.43 |      | ns   |
| $t_{ESBDATACO1}$ |       | 1.04 |       | 1.30 |      | 1.46 | ns   |
| $t_{ESBDATACO2}$ |       | 2.15 |       | 2.70 |      | 3.16 | ns   |
| $t_{ESBDD}$      |       | 2.69 |       | 3.35 |      | 3.97 | ns   |
| $t_{PD}$         |       | 1.55 |       | 1.93 |      | 2.29 | ns   |
| $t_{PTERMSU}$    | 1.01  |      | 1.23  |      | 1.52 |      | ns   |
| $t_{PTERMCO}$    |       | 1.06 |       | 1.32 |      | 1.04 | ns   |

**Table 90. EP20K400E External Bidirectional Timing Parameters**

| Symbol                     | -1 Speed Grade |      | -2 Speed Grade |      | -3 Speed Grade |      | Unit |
|----------------------------|----------------|------|----------------|------|----------------|------|------|
|                            | Min            | Max  | Min            | Max  | Min            | Max  |      |
| $t_{\text{INSUBIDIR}}$     | 2.93           |      | 3.23           |      | 3.44           |      | ns   |
| $t_{\text{INHBIDIR}}$      | 0.00           |      | 0.00           |      | 0.00           |      | ns   |
| $t_{\text{OUTCOBIDIR}}$    | 2.00           | 5.25 | 2.00           | 5.79 | 2.00           | 6.32 | ns   |
| $t_{\text{XZBIDIR}}$       |                | 5.95 |                | 6.77 |                | 7.12 | ns   |
| $t_{\text{ZXBIDIR}}$       |                | 5.95 |                | 6.77 |                | 7.12 | ns   |
| $t_{\text{INSUBIDIRPLL}}$  | 4.31           |      | 4.76           |      | -              |      | ns   |
| $t_{\text{INHBIDIRPLL}}$   | 0.00           |      | 0.00           |      | -              |      | ns   |
| $t_{\text{OUTCOBIDIRPLL}}$ | 0.50           | 2.25 | 0.50           | 2.45 | -              | -    | ns   |
| $t_{\text{XZBIDIRPLL}}$    |                | 2.94 |                | 3.43 |                | -    | ns   |
| $t_{\text{ZXBIDIRPLL}}$    |                | 2.94 |                | 3.43 |                | -    | ns   |

Tables 91 through 96 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K600E APEX 20KE devices.

**Table 91. EP20K600E  $f_{\text{MAX}}$  LE Timing Microparameters**

| Symbol           | -1 Speed Grade |      | -2 Speed Grade |      | -3 Speed Grade |      | Unit |
|------------------|----------------|------|----------------|------|----------------|------|------|
|                  | Min            | Max  | Min            | Max  | Min            | Max  |      |
| $t_{\text{SU}}$  | 0.16           |      | 0.16           |      | 0.17           |      | ns   |
| $t_{\text{H}}$   | 0.29           |      | 0.33           |      | 0.37           |      | ns   |
| $t_{\text{CO}}$  |                | 0.65 |                | 0.38 |                | 0.49 | ns   |
| $t_{\text{LUT}}$ |                | 0.70 |                | 1.00 |                | 1.30 | ns   |

**Table 98. EP20K1000E  $f_{MAX}$  ESB Timing Microparameters**

| Symbol           | -1 Speed Grade |      | -2 Speed Grade |      | -3 Speed Grade |      | Unit |
|------------------|----------------|------|----------------|------|----------------|------|------|
|                  | Min            | Max  | Min            | Max  | Min            | Max  |      |
| $t_{ESBARC}$     |                | 1.78 |                | 2.02 |                | 1.95 | ns   |
| $t_{ESBSRC}$     |                | 2.52 |                | 2.91 |                | 3.14 | ns   |
| $t_{ESBAWC}$     |                | 3.52 |                | 4.11 |                | 4.40 | ns   |
| $t_{ESBSWC}$     |                | 3.23 |                | 3.84 |                | 4.16 | ns   |
| $t_{ESBWASU}$    | 0.62           |      | 0.67           |      | 0.61           |      | ns   |
| $t_{ESBWAH}$     | 0.41           |      | 0.55           |      | 0.55           |      | ns   |
| $t_{ESBWDSU}$    | 0.77           |      | 0.79           |      | 0.81           |      | ns   |
| $t_{ESBWDH}$     | 0.41           |      | 0.55           |      | 0.55           |      | ns   |
| $t_{ESBRASU}$    | 1.74           |      | 1.92           |      | 1.85           |      | ns   |
| $t_{ESBRAH}$     | 0.00           |      | 0.01           |      | 0.23           |      | ns   |
| $t_{ESBWESU}$    | 2.07           |      | 2.28           |      | 2.41           |      | ns   |
| $t_{ESBWEH}$     | 0.00           |      | 0.00           |      | 0.00           |      | ns   |
| $t_{ESBDATASU}$  | 0.25           |      | 0.27           |      | 0.29           |      | ns   |
| $t_{ESBDATAH}$   | 0.13           |      | 0.13           |      | 0.13           |      | ns   |
| $t_{ESBWADDRSU}$ | 0.11           |      | 0.04           |      | 0.11           |      | ns   |
| $t_{ESBRADDRSU}$ | 0.14           |      | 0.11           |      | 0.16           |      | ns   |
| $t_{ESBDATACO1}$ |                | 1.29 |                | 1.50 |                | 1.63 | ns   |
| $t_{ESBDATACO2}$ |                | 2.55 |                | 2.99 |                | 3.22 | ns   |
| $t_{ESBDD}$      |                | 3.12 |                | 3.57 |                | 3.85 | ns   |
| $t_{PD}$         |                | 1.84 |                | 2.13 |                | 2.32 | ns   |
| $t_{PTERMSU}$    | 1.08           |      | 1.19           |      | 1.32           |      | ns   |
| $t_{PTERMCO}$    |                | 1.31 |                | 1.53 |                | 1.66 | ns   |

**Table 110. Selectable I/O Standard Output Delays**

| Symbol          | -1 Speed Grade |       | -2 Speed Grade |       | -3 Speed Grade |       | Unit |
|-----------------|----------------|-------|----------------|-------|----------------|-------|------|
|                 | Min            | Max   | Min            | Max   | Min            | Max   | Min  |
| LVC MOS         |                | 0.00  |                | 0.00  |                | 0.00  | ns   |
| LVTTL           |                | 0.00  |                | 0.00  |                | 0.00  | ns   |
| 2.5 V           |                | 0.00  |                | 0.09  |                | 0.10  | ns   |
| 1.8 V           |                | 2.49  |                | 2.98  |                | 3.03  | ns   |
| PCI             |                | −0.03 |                | 0.17  |                | 0.16  | ns   |
| GTL+            |                | 0.75  |                | 0.75  |                | 0.76  | ns   |
| SSTL-3 Class I  |                | 1.39  |                | 1.51  |                | 1.50  | ns   |
| SSTL-3 Class II |                | 1.11  |                | 1.23  |                | 1.23  | ns   |
| SSTL-2 Class I  |                | 1.35  |                | 1.48  |                | 1.47  | ns   |
| SSTL-2 Class II |                | 1.00  |                | 1.12  |                | 1.12  | ns   |
| LVDS            |                | −0.48 |                | −0.48 |                | −0.48 | ns   |
| CTT             |                | 0.00  |                | 0.00  |                | 0.00  | ns   |
| AGP             |                | 0.00  |                | 0.00  |                | 0.00  | ns   |

## Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at <http://www.altera.com>.

## Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to  $V_{CCIO}$  by a built-in weak pull-up resistor.