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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	120
Number of Logic Elements/Cells	1200
Total RAM Bits	24576
Number of I/O	92
Number of Gates	113000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k30efc144-3">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k30efc144-3</a>

**Table 5. APEX 20K FineLine BGA Package Options & I/O Count** *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

**Notes to Tables 4 and 5:**

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

**Table 6. APEX 20K QFP, BGA & PGA Package Sizes**

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm <sup>2</sup> )	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

**Table 7. APEX 20K FineLine BGA Package Sizes**

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm <sup>2</sup> )	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

## General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an “E” suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). [Table 8](#) compares the features included in APEX 20K and APEX 20KE devices.

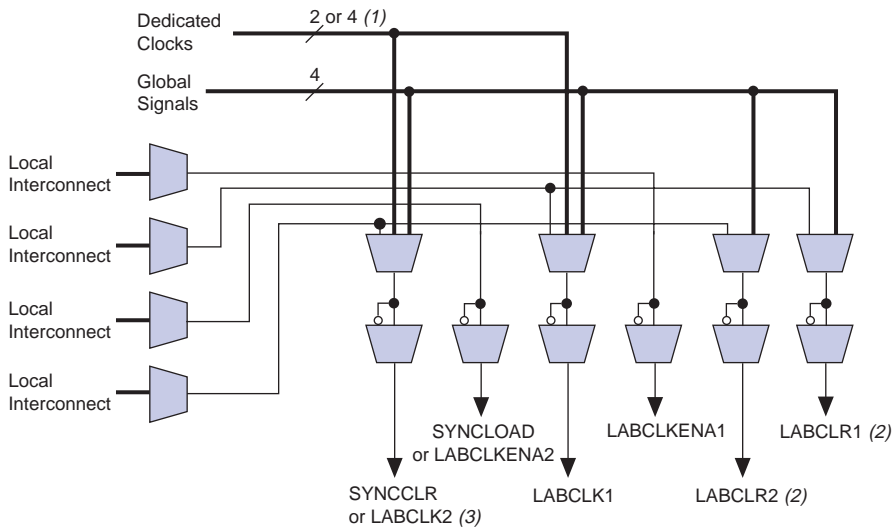
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. **Figure 4** shows the LAB control signal generation circuit.

**Figure 4. LAB Control Signal Generation**



**Notes to Figure 4:**

- (1) APEX 20KE devices have four dedicated clocks.
- (2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
- (3) The SYNCCLR signal can be generated by the local interconnect or global signals.

### *LE Operating Modes*

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

### **FastTrack Interconnect**

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).

Figure 10. FastTrack Connection to Local Interconnect

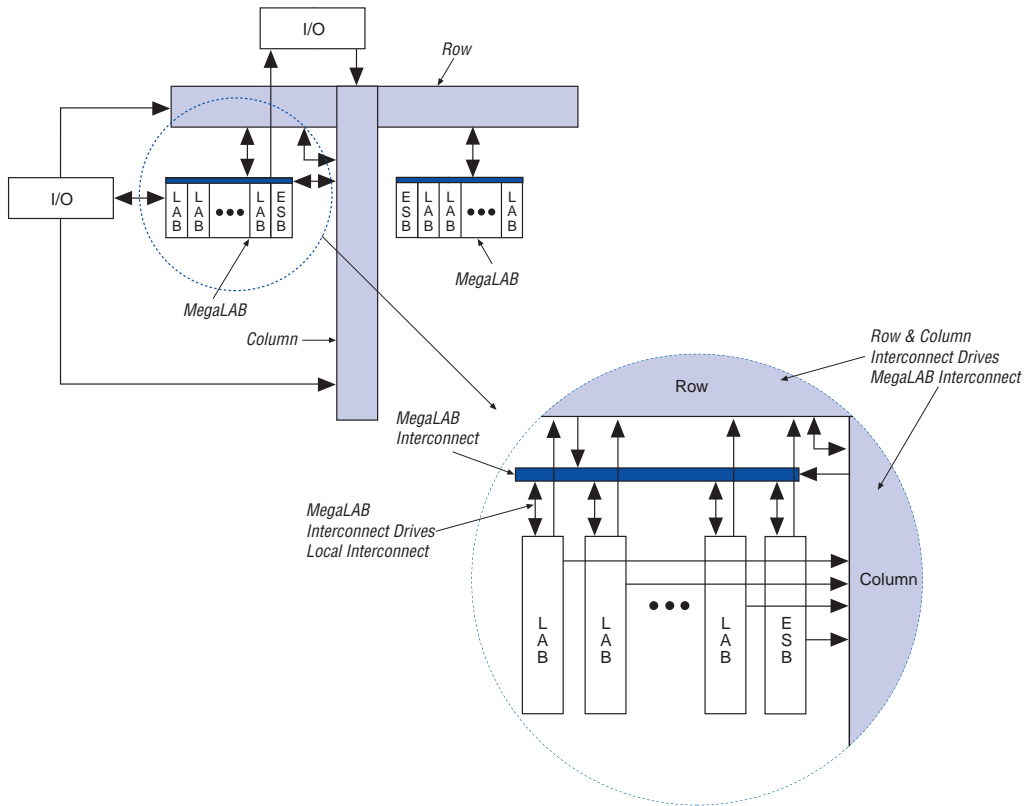
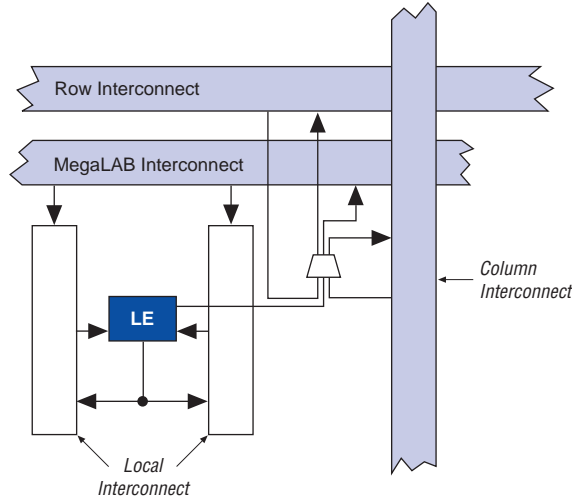


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

**Figure 11. Driving the FastTrack Interconnect**



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABs in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.



**Table 9. APEX 20K Routing Scheme**

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin								✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ (1)				

Note to **Table 9**:

(1) This connection is supported in APEX 20KE devices only.

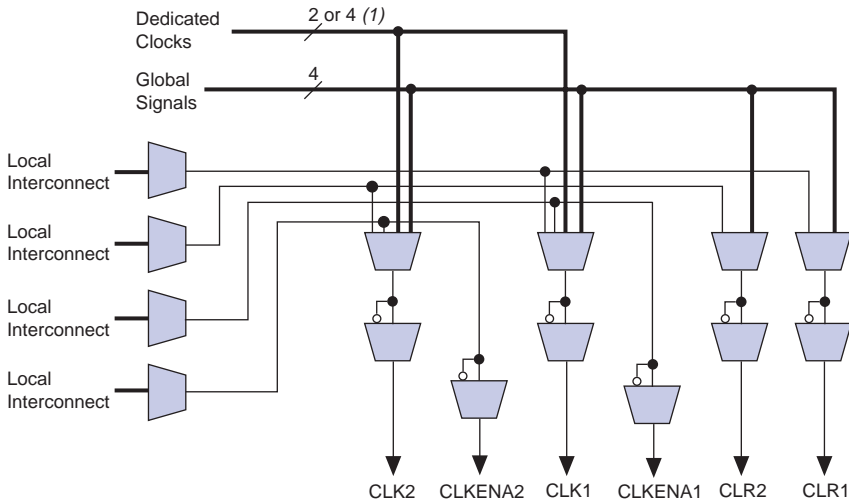
### Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. **Figure 13** shows the ESB in product-term mode.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. **Figure 15** shows the ESB control logic when implementing product-terms.

**Figure 15. ESB Product-Term Mode Control Logic**



**Note to Figure 15:**

(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring expanders to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. **Figure 16** shows the APEX 20K parallel expanders.

**Figure 23. APEX 20KE CAM Block Diagram**



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing “don’t care” bits into words of the memory. The “don’t-care” bit can be used as a mask for CAM comparisons; any bit set to “don’t-care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t-care” bits are used, a third clock cycle is required.

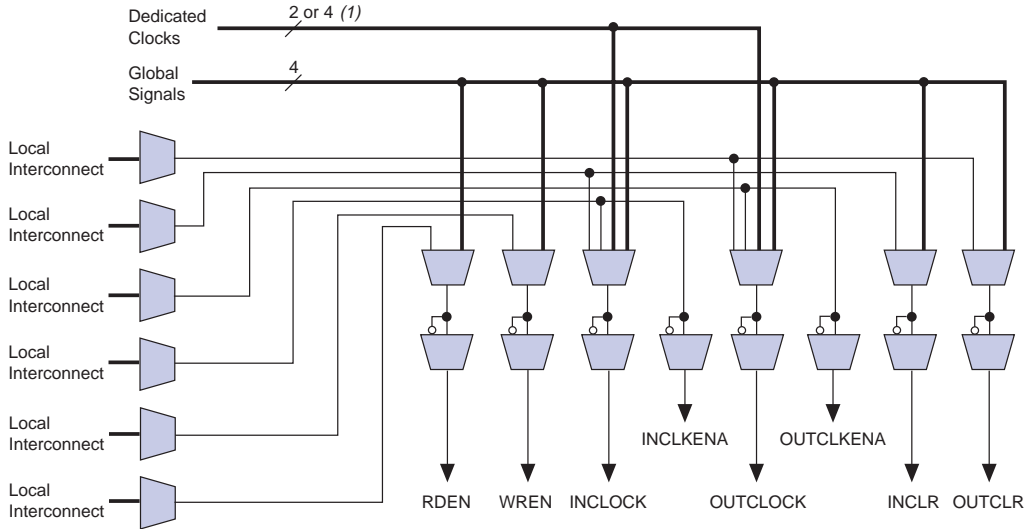


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

### Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. [Figure 24](#) shows the ESB control signal generation logic.

**Figure 24. ESB Control Signal Generation**



**Note to Figure 24:**

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

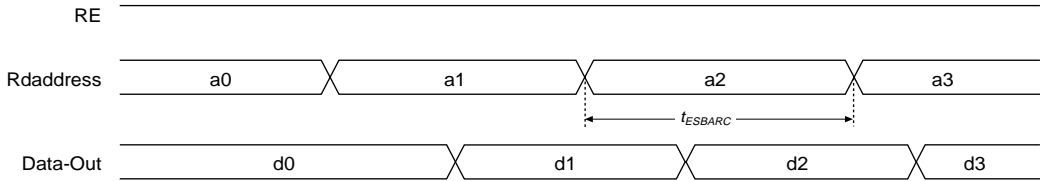
**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)** *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	3.3-V low-level TTL output voltage	I <sub>OL</sub> = 12 mA DC, V <sub>CCIO</sub> = 3.00 V (11)			0.45	V
	3.3-V low-level CMOS output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (11)			0.2	V
	3.3-V low-level PCI output voltage	I <sub>OL</sub> = 1.5 mA DC, V <sub>CCIO</sub> = 3.00 to 3.60 V (11)			0.1 × V <sub>CCIO</sub>	V
	2.5-V low-level output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 2.30 V (11)			0.2	V
I <sub>OL</sub> = 1 mA DC, V <sub>CCIO</sub> = 2.30 V (11)				0.4	V	
I <sub>OL</sub> = 2 mA DC, V <sub>CCIO</sub> = 2.30 V (11)				0.7	V	
I <sub>I</sub>	Input pin leakage current	V <sub>I</sub> = 5.75 to -0.5 V	-10		10	μA
I <sub>OZ</sub>	Tri-stated I/O pin leakage current	V <sub>O</sub> = 5.75 to -0.5 V	-10		10	μA
I <sub>CC0</sub>	V <sub>CC</sub> supply current (standby) (All ESBs in power-down mode)	V <sub>I</sub> = ground, no load, no toggling inputs, -1 speed grade (12)		10		mA
		V <sub>I</sub> = ground, no load, no toggling inputs, -2, -3 speed grades (12)		5		mA
R <sub>CONF</sub>	Value of I/O pin pull-up resistor before and during configuration	V <sub>CCIO</sub> = 3.0 V (13)	20		50	W
		V <sub>CCIO</sub> = 2.375 V (13)	30		80	W

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms

**ESB Asynchronous Read**



**ESB Asynchronous Write**

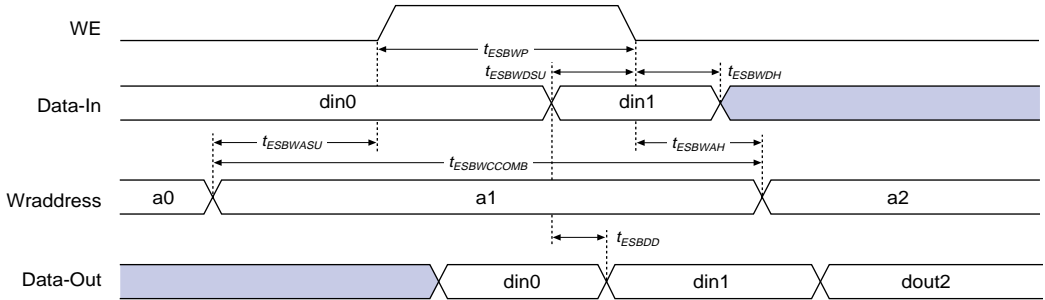


Figure 39. ESB Synchronous Timing Waveforms

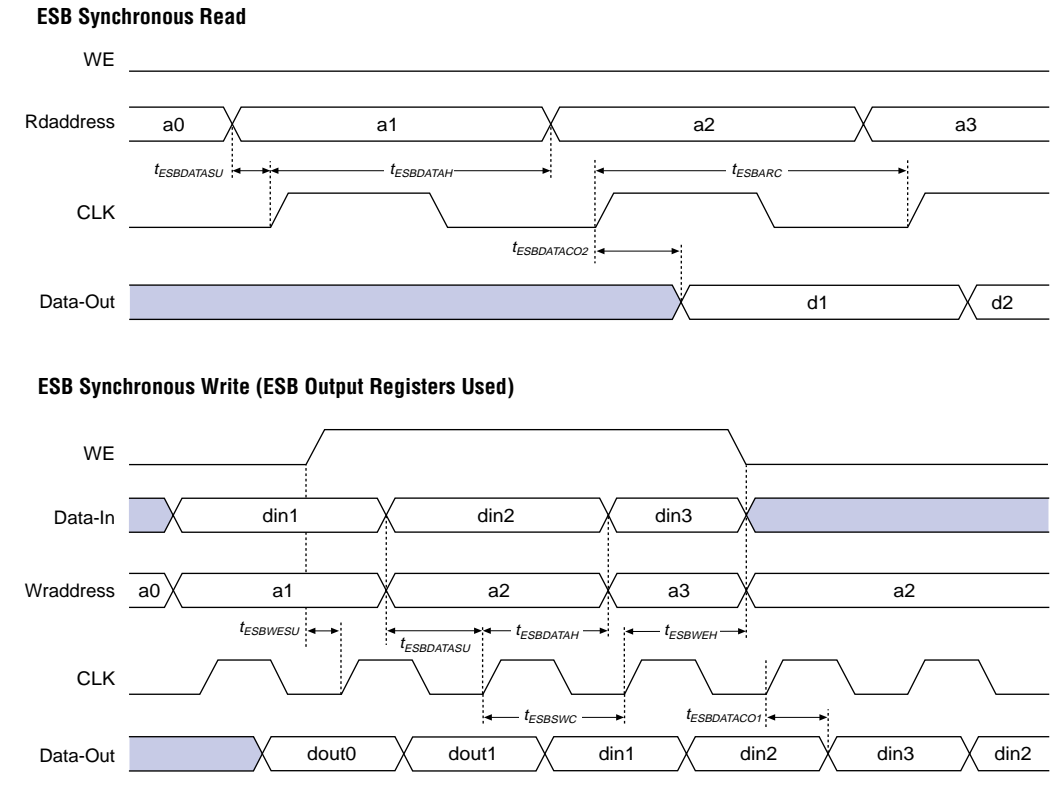


Figure 40 shows the timing model for bidirectional I/O pin timing.

**Table 31. APEX 20K  $t_{MAX}$  Timing Parameters (Part 2 of 2)**

Symbol	Parameter
$t_{ESB\text{DATA}CO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
$t_{F1-4}$	Fanout delay using local interconnect
$t_{F5-20}$	Fanout delay using MegaLab Interconnect
$t_{F20+}$	Fanout delay using FastTrack Interconnect
$t_{CH}$	Minimum clock high time from clock pin
$t_{CL}$	Minimum clock low time from clock pin
$t_{CLRP}$	LE clear pulse width
$t_{PREP}$	LE preset pulse width
$t_{ESBCH}$	Clock high time
$t_{ESBCL}$	Clock low time
$t_{ESBWP}$	Write pulse width
$t_{ESBRP}$	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

**Table 32. APEX 20K External Timing Parameters Note (1)**

Symbol	Clock Parameter
$t_{INSU}$	Setup time with global clock at IOE register
$t_{INH}$	Hold time with global clock at IOE register
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE register

**Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)**

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INH\text{BIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCO\text{BIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZ\text{BIDIR}}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{ZX\text{BIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF



**Table 42. EP20K400  $f_{MAX}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.1		0.3		0.6		ns
$t_H$	0.5		0.8		0.9		ns
$t_{CO}$		0.1		0.4		0.6	ns
$t_{LUT}$		1.0		1.2		1.4	ns
$t_{ESBRC}$		1.7		2.1		2.4	ns
$t_{ESBWC}$		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
$t_{ESBDD}$		2.5		3.3		3.6	ns
$t_{PD}$		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
$t_{F1-4}$		0.4		0.5		0.6	ns
$t_{F5-20}$		2.6		2.8		2.9	ns
$t_{F20+}$		3.7		3.8		3.9	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns
$t_{CLRP}$	0.5		0.6		0.8		ns
$t_{PREP}$	0.5		0.5		0.5		ns
$t_{ESBCH}$	2.0		2.5		3.0		ns
$t_{ESBCL}$	2.0		2.5		3.0		ns
$t_{ESBWP}$	1.5		1.9		2.2		ns
$t_{ESBRP}$	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 52. EP20K30E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	0.55		0.78		1.15		ns
t <sub>CL</sub>	0.55		0.78		1.15		ns
t <sub>CLRP</sub>	0.22		0.31		0.46		ns
t <sub>PREP</sub>	0.22		0.31		0.46		ns
t <sub>ESBCH</sub>	0.55		0.78		1.15		ns
t <sub>ESBCL</sub>	0.55		0.78		1.15		ns
t <sub>ESBWP</sub>	1.43		2.01		2.97		ns
t <sub>ESBRP</sub>	1.15		1.62		2.39		ns

**Table 53. EP20K30E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.02		2.13		2.24		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>INSUPLL</sub>	2.11		2.23		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns

**Table 54. EP20K30E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	1.85		1.77		1.54		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>XZBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>ZXBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>INSUBIDIRPLL</sub>	4.12		4.24		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns
t <sub>XZBIDIRPLL</sub>		5.21		5.99		-	ns
t <sub>ZXBIDIRPLL</sub>		5.21		5.99		-	ns

Tables 55 through 60 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

**Table 55. EP20K60E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.17		0.15		0.16		ns
$t_H$	0.32		0.33		0.39		ns
$t_{CO}$		0.29		0.40		0.60	ns
$t_{LUT}$		0.77		1.07		1.59	ns

**Table 69. EP20K160E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.26		0.28	ns
$t_{F5-20}$		1.00		1.18		1.35	ns
$t_{F20+}$		1.95		2.19		2.30	ns

**Table 70. EP20K160E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.34		1.43		1.55		ns
$t_{CL}$	1.34		1.43		1.55		ns
$t_{CLRP}$	0.18		0.19		0.21		ns
$t_{PREP}$	0.18		0.19		0.21		ns
$t_{ESBCH}$	1.34		1.43		1.55		ns
$t_{ESBCL}$	1.34		1.43		1.55		ns
$t_{ESBWP}$	1.15		1.45		1.73		ns
$t_{ESBRP}$	0.93		1.15		1.38		ns

**Table 71. EP20K160E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.23		2.34		2.47		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{INSUPLL}$	2.12		2.07		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns

**Table 108. EP20K1500E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	3.47		3.68		3.99		ns
t <sub>INHIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	6.18	2.00	6.81	2.00	7.36	ns
t <sub>XZBIDIR</sub>		6.91		7.62		8.38	ns
t <sub>ZXBIDIR</sub>		6.91		7.62		8.38	ns
t <sub>INSUBIDIRPLL</sub>	3.05		3.26				ns
t <sub>INHIDIRPLL</sub>	0.00		0.00				ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.67	0.50	2.99			ns
t <sub>XZBIDIRPLL</sub>		3.41		3.80			ns
t <sub>ZXBIDIRPLL</sub>		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

**Table 109. Selectable I/O Standard Input Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		-0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		-0.24		-0.23		-0.19	ns
SSTL-3 Class I		-0.32		-0.21		-0.47	ns
SSTL-3 Class II		-0.08		0.03		-0.23	ns
SSTL-2 Class I		-0.17		-0.06		-0.32	ns
SSTL-2 Class II		-0.16		-0.05		-0.31	ns
LVDS		-0.12		-0.12		-0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns