Intel - EP20K30ETC144-2N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	120
Number of Logic Elements/Cells	1200
Total RAM Bits	24576
Number of I/O	92
Number of Gates	113000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k30etc144-2n

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 10. FastTrack Connection to Local Interconnect

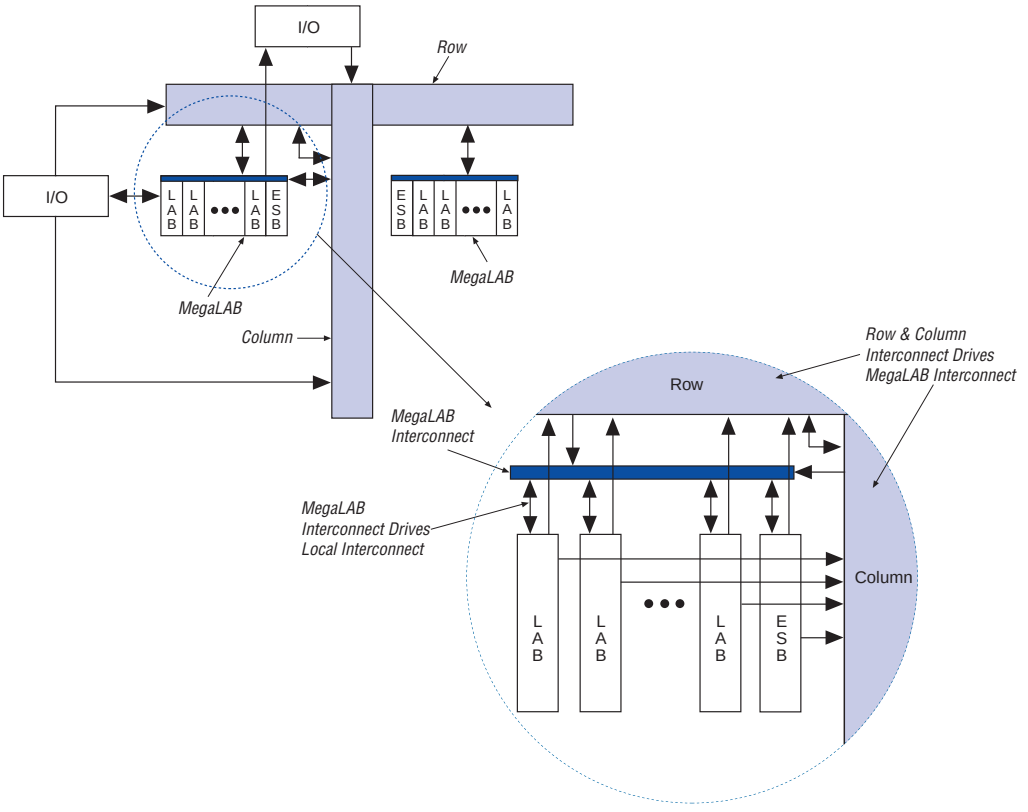


Figure 12. APEX 20KE FastRow Interconnect

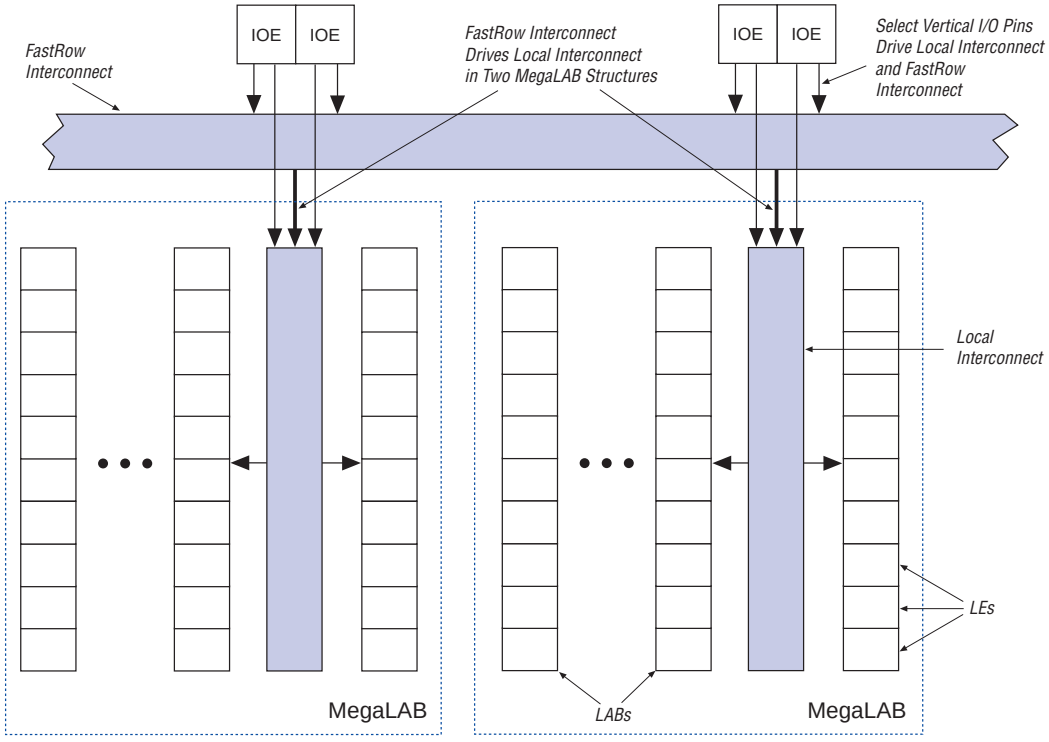
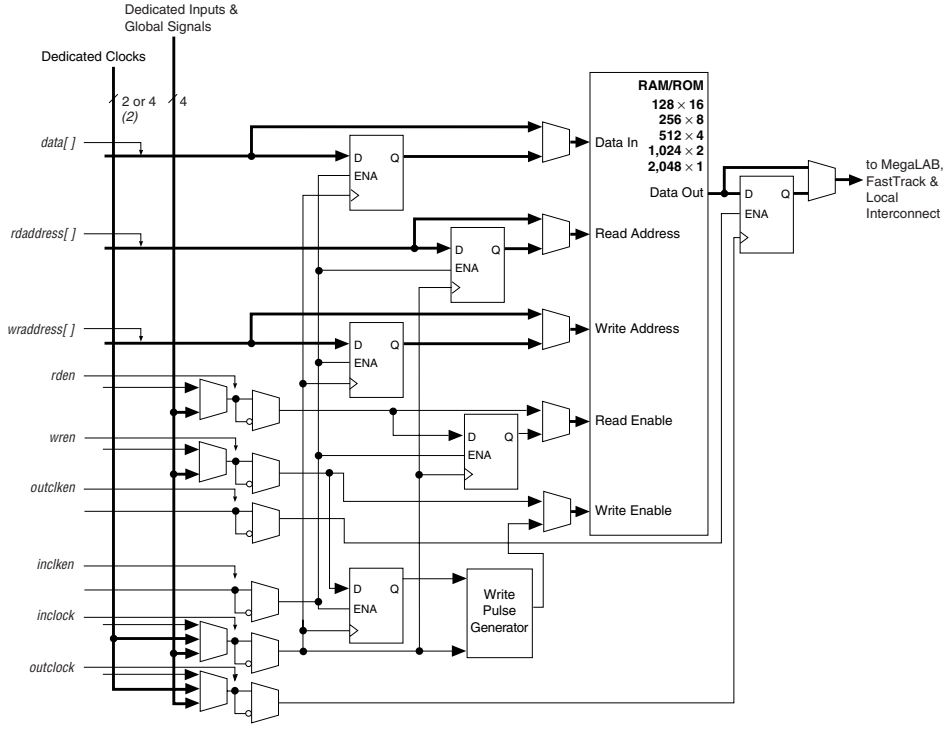


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode *Note (1)*



Notes to Figure 21:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Single-Port Mode

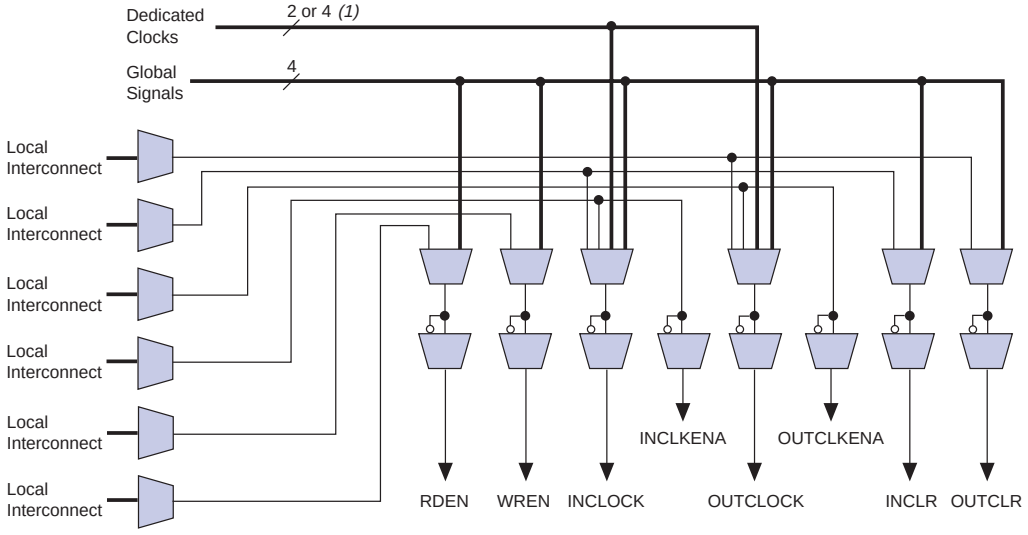
The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

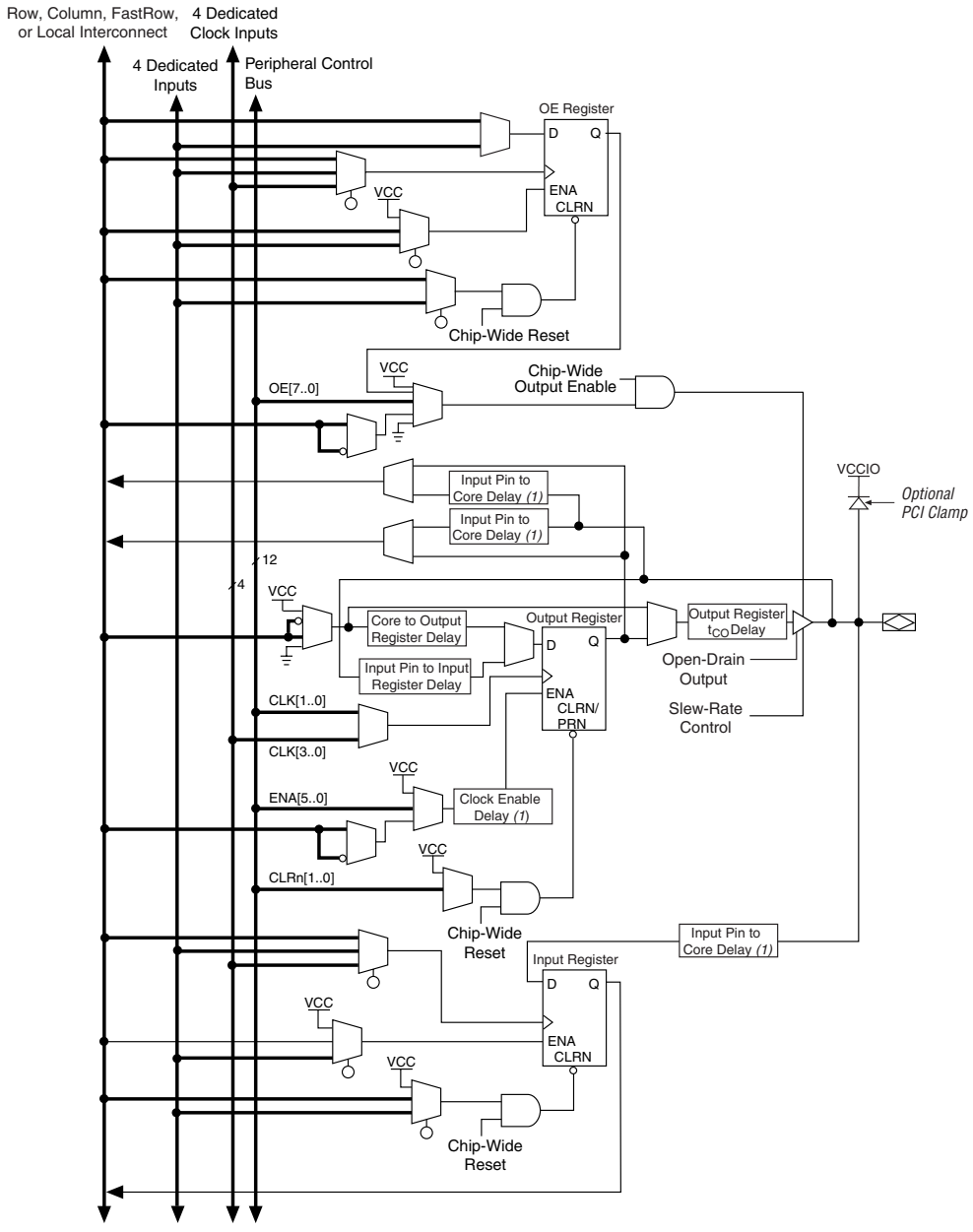
Figure 24. ESB Control Signal Generation



Note to Figure 24:
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Figure 26. APEX 20KE Bidirectional I/O Registers *Notes (1), (2)*



Notes to Figure 26:

(1) This programmable delay has four settings: off and three levels of delay.

(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

Notes to Table 12:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

Table 13. APEX 20KE MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓	*(2)*			✓ *(3)*	

Notes to Table 13:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

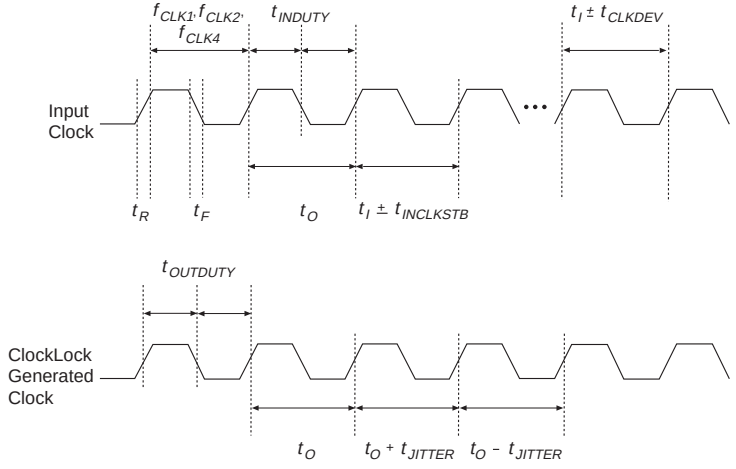
(3) When V_{CCIO} = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

Figure 30. Specifications for the Incoming & Generated Clocks *Note (1)*



Note to Figure 30:
(1) The tI parameter refers to the nominal input clock period; the tO parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	180	MHz
f_{CLK1} *(1)*	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	180 *(1)*	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	90	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	48	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) *(2)*		25,000 *(3)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ClockBoost to acquire lock *(4)*		10	µs

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock *(5)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:

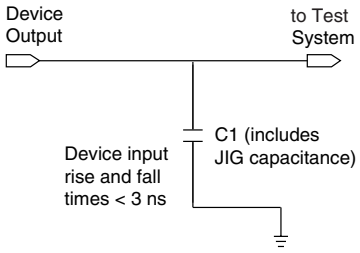
(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)*		25,000 *(2)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock *(3)*		10	µs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock *(4)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Figure 32. APEX 20K AC Test Conditions *Note (1)*



Note to Figure 32:

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the f_{MAX} timing model for APEX 20K devices.

Figure 36. APEX 20K f_{MAX} Timing Model

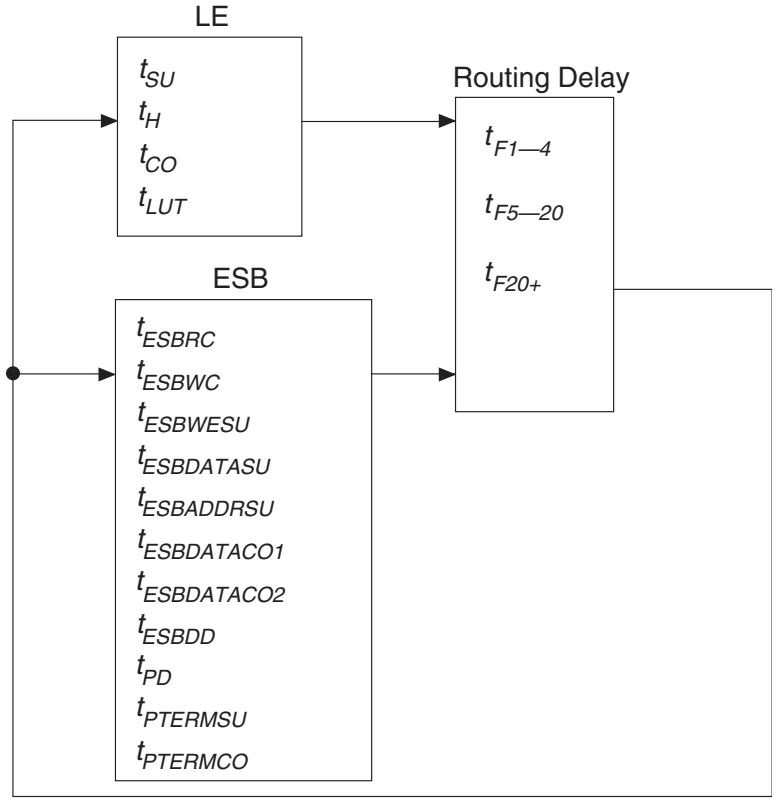
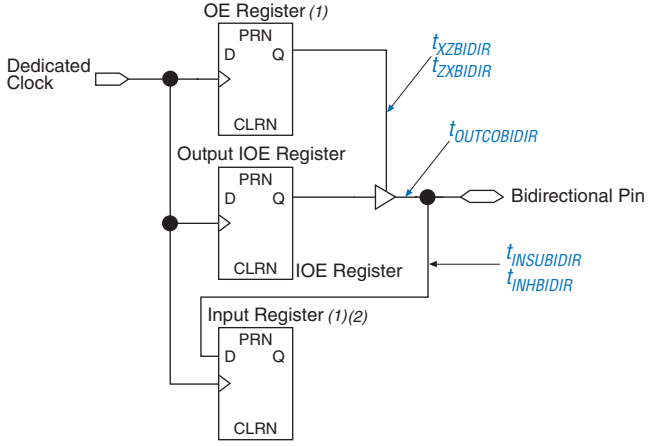


Figure 37 shows the f_{MAX} timing model for APEX 20KE devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Figure 40. Synchronous Bidirectional Pin External Timing



Notes to Figure 40:

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the f_{MAX} timing parameters shown in Figure 36 on page 68.

Table 31. APEX 20K f_{MAX} Timing Parameters (Part 1 of 2)

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in
t_{ESBRC}	ESB Asynchronous read cycle time
t_{ESBWC}	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBADDRSU}$	ESB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers

Table 41. EP20K200 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.4		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 46. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.9		2.3		2.6		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.1		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Table 47. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.4		1.8		2.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
t_{INSU} (2)	0.4		1.0		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	3.1	0.5	4.1	–	–	ns

Table 48. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.4		1.8		2.0		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{XZBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{ZXBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{INSUBIDIR}$ (2)	0.5		1.0		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.1	0.5	4.1	–	–	ns
$t_{XZBIDIR}$ (2)		6.2		7.6		–	ns
$t_{ZXBIDIR}$ (2)		6.2		7.6		–	ns

Table 80. EP20K300E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.79		2.44		3.25	ns
t_{ESBSRC}		2.40		3.12		4.01	ns
t_{ESBAWC}		3.41		4.65		6.20	ns
t_{ESBSWC}		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
t_{ESBDD}		3.41		4.65		6.20	ns
t_{PD}		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

Table 81. EP20K300E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.24		0.26	ns
t_{F5-20}		1.33		1.43		1.58	ns
t_{F20+}		3.63		3.93		4.35	ns

Tables 85 through 90 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

Table 85. EP20K400E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.23		0.23		ns
t_{H}	0.23		0.23		0.23		ns
t_{CO}		0.25		0.29		0.32	ns
t_{LUT}		0.70		0.83		1.01	ns

Table 99. EP20K1000E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.27		0.27		0.27	ns
t_{F5-20}		1.45		1.63		1.75	ns
t_{F20+}		4.15		4.33		4.97	ns

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 101. EP20K1000E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.70		2.84		2.97		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{INSUPLL}$	1.64		2.09		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 107. EP20K1500E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.09		3.30		3.58		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{INSUPLL}$	1.94		2.08		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.67	0.50	2.99	-	-	ns

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