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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 120 |
| Number of Logic Elements/Cells | 1200 |
| Total RAM Bits | 24576 |
| Number of I/O | 92 |
| Number of Gates | 113000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k30etc144-2x |

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

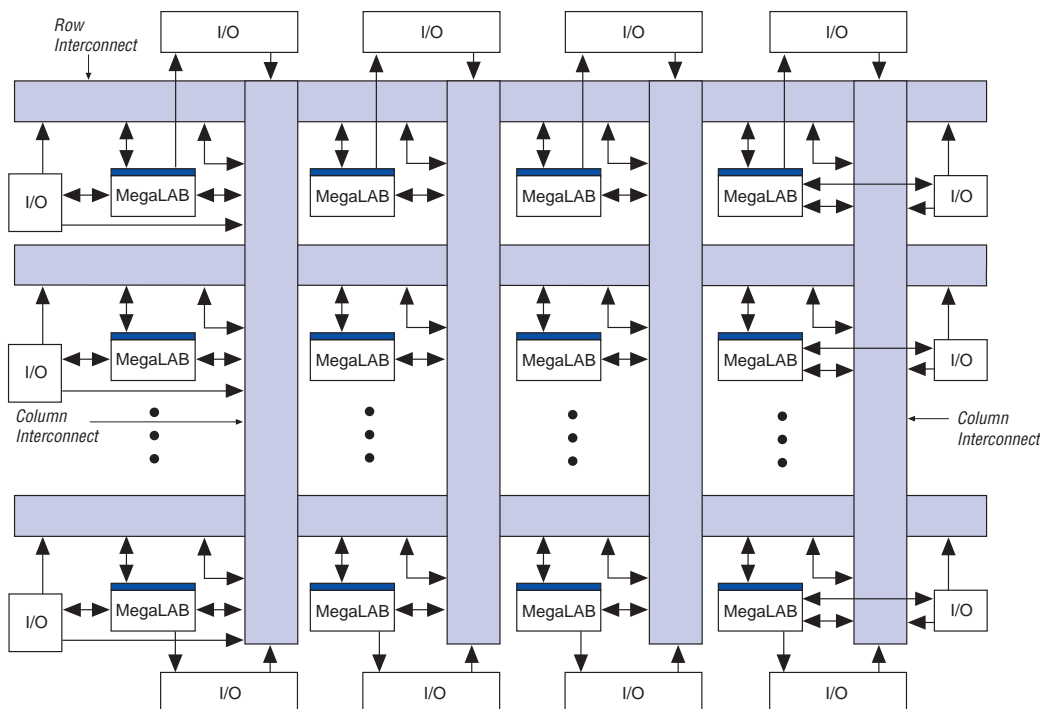
Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).

Figure 9. APEX 20K Interconnect Structure

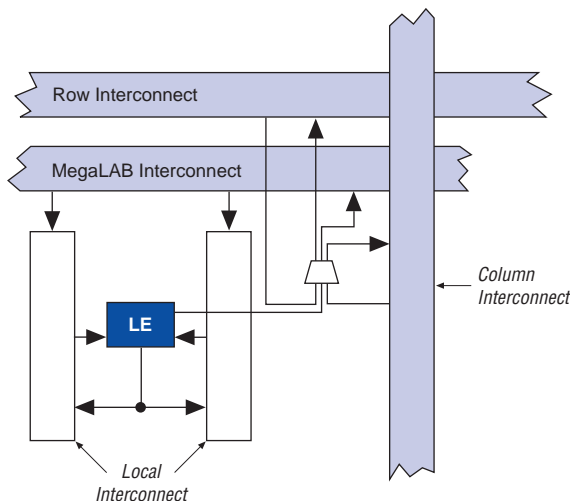
A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

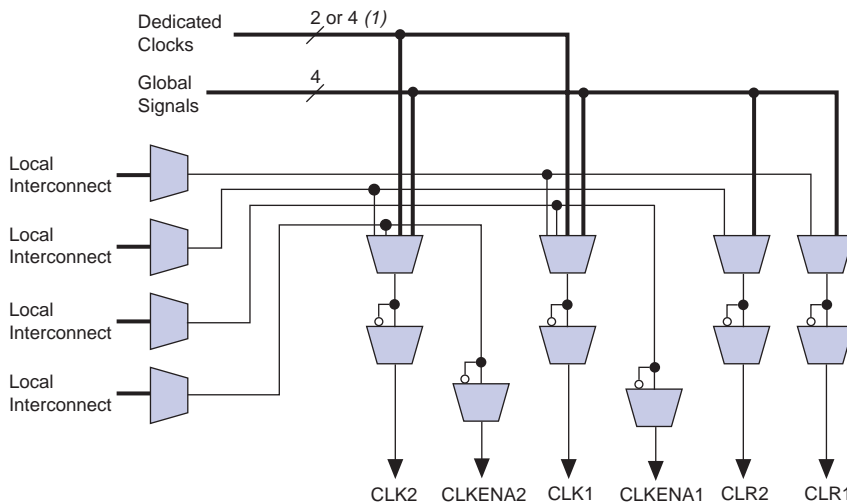
Figure 11. Driving the FastTrack Interconnect



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABs in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Note to Figure 15:

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

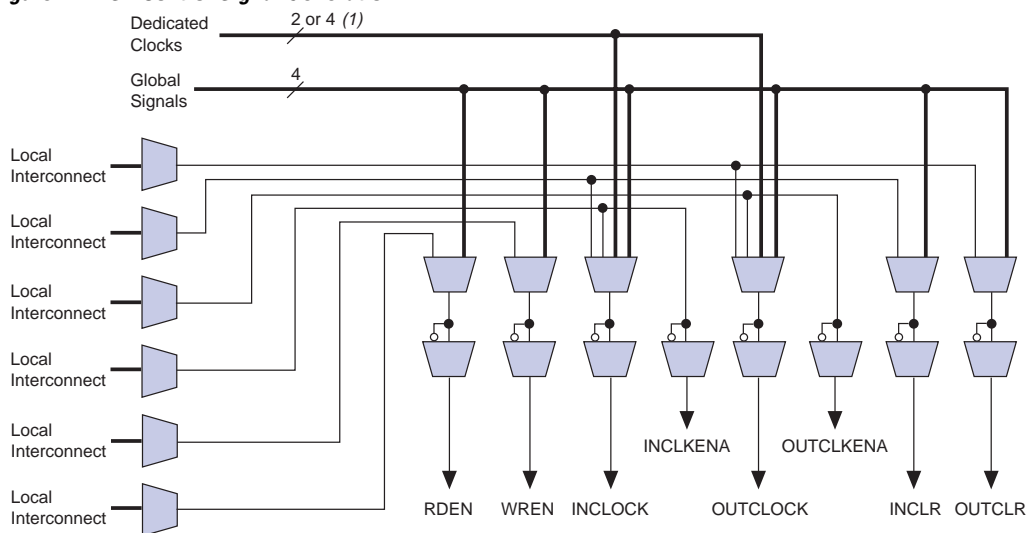


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. [Figure 24](#) shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



Note to Figure 24:

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

| Table 10. APEX 20K Programmable Delay Chains | |
|---|---|
| Programmable Delays | Quartus II Logic Option |
| Input pin to core delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input register |
| Core to output register delay | Decrease input delay to output register |
| Output register t_{CO} delay | Increase delay to output pin |

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in [Table 19](#). Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

Table 19. APEX 20K JTAG Instructions

| JTAG Instruction | Description |
|----------------------------|--|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS (1) | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| ICR Instructions | Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor. |
| SignalTap Instructions (1) | Monitors internal device operation with the SignalTap embedded logic analyzer. |

Note to Table 19:

(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) Notes (2), (7), (8)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|--|---|-----|-----|-----------------------|---------------|
| V_{OL} | 3.3-V low-level TTL output voltage | $I_{OL} = 12 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (11) | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (11) | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL} = 1.5 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (11) | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11) | | | 0.2 | V |
| | | $I_{OL} = 1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11) | | | 0.4 | V |
| | | $I_{OL} = 2 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11) | | | 0.7 | V |
| I_I | Input pin leakage current | $V_I = 5.75 \text{ to } -0.5 \text{ V}$ | -10 | | 10 | μA |
| I_{OZ} | Tri-stated I/O pin leakage current | $V_O = 5.75 \text{ to } -0.5 \text{ V}$ | -10 | | 10 | μA |
| I_{CC0} | V_{CC} supply current (standby) (All ESBs in power-down mode) | $V_I = \text{ground}$, no load, no toggling inputs, -1 speed grade (12) | | 10 | | mA |
| | | $V_I = \text{ground}$, no load, no toggling inputs, -2, -3 speed grades (12) | | 5 | | mA |
| R_{CONF} | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO} = 3.0 \text{ V}$ (13) | 20 | | 50 | W |
| | | $V_{CCIO} = 2.375 \text{ V}$ (13) | 30 | | 80 | W |

Table 29. APEX 20KE Device DC Operating Conditions *Notes (7), (8), (9)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|---|--|---------------------------------|-----|---------------------------------|------------|
| V_{IH} | High-level LVTTL, CMOS, or 3.3-V PCI input voltage | | 1.7, $0.5 \times V_{CCIO}$ (10) | | 4.1 | V |
| V_{IL} | Low-level LVTTL, CMOS, or 3.3-V PCI input voltage | | -0.5 | | $0.8, 0.3 \times V_{CCIO}$ (10) | V |
| V_{OH} | 3.3-V high-level LVTTL output voltage | $I_{OH} = -12$ mA DC, $V_{CCIO} = 3.00$ V (11) | 2.4 | | | V |
| | 3.3-V high-level LVCMOS output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (11) | $V_{CCIO} - 0.2$ | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (11) | $0.9 \times V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (11) | 2.1 | | | V |
| | | $I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (11) | 2.0 | | | V |
| | | $I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (11) | 1.7 | | | V |
| V_{OL} | 3.3-V low-level LVTTL output voltage | $I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (12) | | | 0.4 | V |
| | 3.3-V low-level LVCMOS output voltage | $I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (12) | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (12) | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (12) | | | 0.2 | V |
| | | $I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (12) | | | 0.4 | V |
| | | $I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (12) | | | 0.7 | V |
| I_I | Input pin leakage current | $V_I = 4.1$ to -0.5 V (13) | -10 | | 10 | μ A |
| I_{OZ} | Tri-stated I/O pin leakage current | $V_O = 4.1$ to -0.5 V (13) | -10 | | 10 | μ A |
| I_{CC0} | V_{CC} supply current (standby) (All ESBs in power-down mode) | $V_I =$ ground, no load, no toggling inputs, -1 speed grade | | 10 | | mA |
| | | $V_I =$ ground, no load, no toggling inputs, -2, -3 speed grades | | 5 | | mA |
| R_{CONF} | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO} = 3.0$ V (14) | 20 | | 50 | k Ω |
| | | $V_{CCIO} = 2.375$ V (14) | 30 | | 80 | k Ω |
| | | $V_{CCIO} = 1.71$ V (14) | 60 | | 150 | k Ω |

Figure 37. APEX 20KE t_{MAX} Timing Model

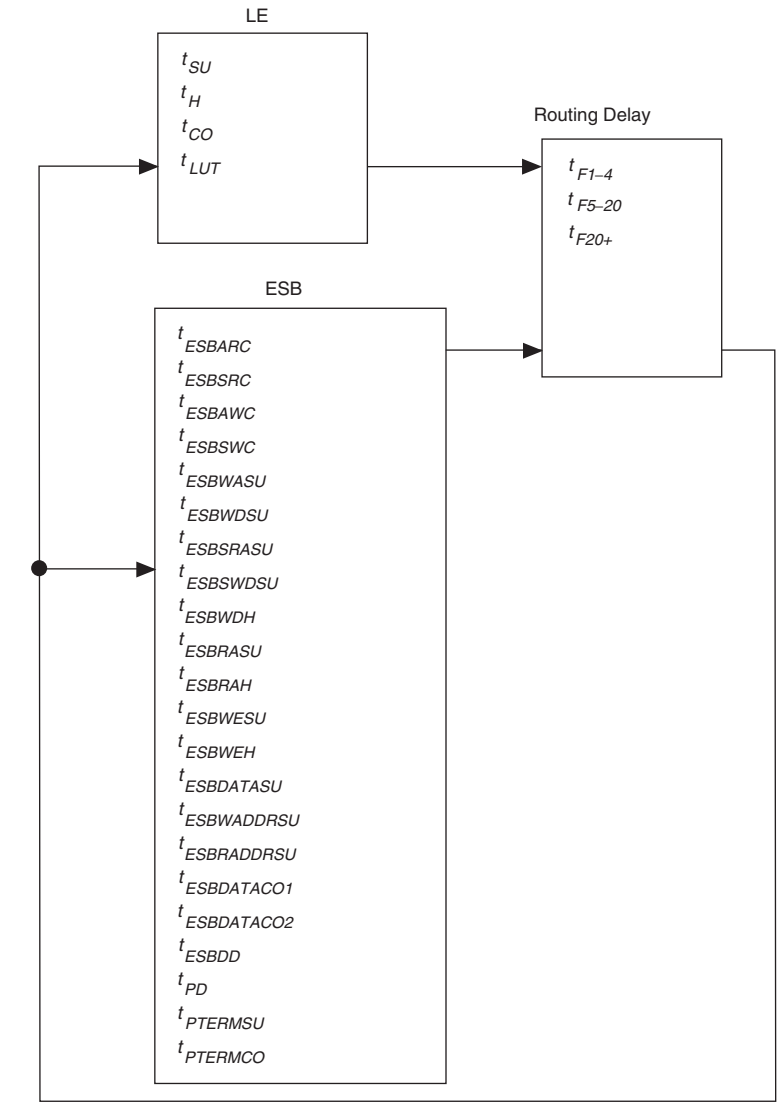
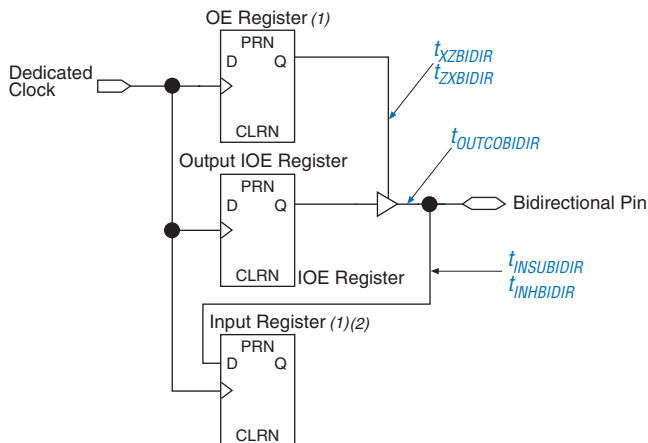


Figure 40. Synchronous Bidirectional Pin External Timing**Notes to Figure 40:**

- (1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.
- (2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the f_{MAX} timing parameters shown in Figure 36 on page 68.

Table 31. APEX 20K f_{MAX} Timing Parameters (Part 1 of 2)

| Symbol | Parameter |
|------------------|--|
| t_{SU} | LE register setup time before clock |
| t_H | LE register hold time after clock |
| t_{CO} | LE register clock-to-output delay |
| t_{LUT} | LUT delay for data-in |
| t_{ESBRC} | ESB Asynchronous read cycle time |
| t_{ESBWC} | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |

Table 43. EP20K100 External Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|------------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSU} (1) | 2.3 | | 2.8 | | 3.2 | | ns |
| t _{INH} (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{OUTCO} (1) | 2.0 | 4.5 | 2.0 | 4.9 | 2.0 | 6.6 | ns |
| t _{INSU} (2) | 1.1 | | 1.2 | | — | | ns |
| t _{INH} (2) | 0.0 | | 0.0 | | — | | ns |
| t _{OUTCO} (2) | 0.5 | 2.7 | 0.5 | 3.1 | — | 4.8 | ns |

Table 44. EP20K100 External Bidirectional Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-----------------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSUBIDIR} (1) | 2.3 | | 2.8 | | 3.2 | | ns |
| t _{INHBIDIR} (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{OUTCOBIDIR} (1) | 2.0 | 4.5 | 2.0 | 4.9 | 2.0 | 6.6 | ns |
| t _{XZBIDIR} (1) | | 5.0 | | 5.9 | | 6.9 | ns |
| t _{ZXBIDIR} (1) | | 5.0 | | 5.9 | | 6.9 | ns |
| t _{INSUBIDIR} (2) | 1.0 | | 1.2 | | — | | ns |
| t _{INHBIDIR} (2) | 0.0 | | 0.0 | | — | | ns |
| t _{OUTCOBIDIR} (2) | 0.5 | 2.7 | 0.5 | 3.1 | — | — | ns |
| t _{XZBIDIR} (2) | | 4.3 | | 5.0 | | — | ns |
| t _{ZXBIDIR} (2) | | 4.3 | | 5.0 | | — | ns |

Table 45. EP20K200 External Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|------------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSU} (1) | 1.9 | | 2.3 | | 2.6 | | ns |
| t _{INH} (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{OUTCO} (1) | 2.0 | 4.6 | 2.0 | 5.6 | 2.0 | 6.8 | ns |
| t _{INSU} (2) | 1.1 | | 1.2 | | — | | ns |
| t _{INH} (2) | 0.0 | | 0.0 | | — | | ns |
| t _{OUTCO} (2) | 0.5 | 2.7 | 0.5 | 3.1 | — | — | ns |

Tables 67 through 72 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

Table 67. EP20K160E f_{MAX} LE Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|-----------|------|------|------|------|------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{SU} | 0.22 | | 0.24 | | 0.26 | | ns |
| t_H | 0.22 | | 0.24 | | 0.26 | | ns |
| t_{CO} | | 0.25 | | 0.31 | | 0.35 | ns |
| t_{LUT} | | 0.69 | | 0.88 | | 1.12 | ns |

Table 68. EP20K160E t_{MAX} ESB Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|------------------|-------|------|-------|------|------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{ESBARC} | | 1.65 | | 2.02 | | 2.11 | ns |
| t_{ESBSRC} | | 2.21 | | 2.70 | | 3.11 | ns |
| t_{ESBAWC} | | 3.04 | | 3.79 | | 4.42 | ns |
| t_{ESBSWC} | | 2.81 | | 3.56 | | 4.10 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.66 | | 0.73 | | ns |
| t_{ESBWAH} | 0.36 | | 0.45 | | 0.47 | | ns |
| $t_{ESBWDSU}$ | 0.68 | | 0.81 | | 0.94 | | ns |
| t_{ESBWDH} | 0.36 | | 0.45 | | 0.47 | | ns |
| $t_{ESBRASU}$ | 1.58 | | 1.87 | | 2.06 | | ns |
| t_{ESBRAH} | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.41 | | 1.71 | | 2.00 | | ns |
| t_{ESBWEH} | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.02 | | -0.03 | | 0.09 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.14 | | 0.17 | | 0.35 | | ns |
| $t_{ESBRADDRSU}$ | 0.21 | | 0.27 | | 0.43 | | ns |
| $t_{ESBDATACO1}$ | | 1.04 | | 1.30 | | 1.46 | ns |
| $t_{ESBDATACO2}$ | | 2.15 | | 2.70 | | 3.16 | ns |
| t_{ESBDD} | | 2.69 | | 3.35 | | 3.97 | ns |
| t_{PD} | | 1.55 | | 1.93 | | 2.29 | ns |
| $t_{PTERMSU}$ | 1.01 | | 1.23 | | 1.52 | | ns |
| $t_{PTERMCO}$ | | 1.06 | | 1.32 | | 1.04 | ns |

Table 82. EP20K300E Minimum Pulse Width Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|--------------------|------|-----|------|-----|------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{CH} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{CL} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{CLRP} | 0.19 | | 0.26 | | 0.35 | | ns |
| t _{PREP} | 0.19 | | 0.26 | | 0.35 | | ns |
| t _{ESBCH} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{ESBCL} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{ESBWP} | 1.25 | | 1.71 | | 2.28 | | ns |
| t _{ESBRP} | 1.01 | | 1.38 | | 1.84 | | ns |

Table 83. EP20K300E External Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|-----------------------|------|------|------|------|------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSU} | 2.31 | | 2.44 | | 2.57 | | ns |
| t _{INH} | 0.00 | | 0.00 | | 0.00 | | ns |
| t _{OUTCO} | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| t _{INSUPLL} | 1.76 | | 1.85 | | - | | ns |
| t _{INHPLL} | 0.00 | | 0.00 | | - | | ns |
| t _{OUTCOPLL} | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |

Table 84. EP20K300E External Bidirectional Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|----------------------------|------|------|------|------|------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSUBIDIR} | 2.77 | | 2.85 | | 3.11 | | ns |
| t _{INHBIDIR} | 0.00 | | 0.00 | | 0.00 | | ns |
| t _{OUTCOBIDIR} | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| t _{XZBIDIR} | | 7.59 | | 8.30 | | 9.09 | ns |
| t _{ZXBIDIR} | | 7.59 | | 8.30 | | 9.09 | ns |
| t _{INSUBIDIRPLL} | 2.50 | | 2.76 | | - | | ns |
| t _{INHBIDIRPLL} | 0.00 | | 0.00 | | - | | ns |
| t _{OUTCOBIDIRPLL} | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |
| t _{XZBIDIRPLL} | | 5.00 | | 5.43 | | - | ns |
| t _{ZXBIDIRPLL} | | 5.00 | | 5.43 | | - | ns |

Table 94. EP20K600E Minimum Pulse Width Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|--------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{CH} | 2.00 | | 2.50 | | 2.75 | | ns |
| t _{CL} | 2.00 | | 2.50 | | 2.75 | | ns |
| t _{CLRP} | 0.18 | | 0.26 | | 0.34 | | ns |
| t _{PREP} | 0.18 | | 0.26 | | 0.34 | | ns |
| t _{ESBCH} | 2.00 | | 2.50 | | 2.75 | | ns |
| t _{ESBCL} | 2.00 | | 2.50 | | 2.75 | | ns |
| t _{ESBWP} | 1.17 | | 1.68 | | 2.18 | | ns |
| t _{ESBRP} | 0.95 | | 1.35 | | 1.76 | | ns |

Table 95. EP20K600E External Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-----------------------|----------------|------|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSU} | 2.74 | | 2.74 | | 2.87 | | ns |
| t _{INH} | 0.00 | | 0.00 | | 0.00 | | ns |
| t _{OUTCO} | 2.00 | 5.51 | 2.00 | 6.06 | 2.00 | 6.61 | ns |
| t _{INSUPLL} | 1.86 | | 1.96 | | - | | ns |
| t _{INHPLL} | 0.00 | | 0.00 | | - | | ns |
| t _{OUTCOPLL} | 0.50 | 2.62 | 0.50 | 2.91 | - | - | ns |

Table 96. EP20K600E External Bidirectional Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|----------------------------|----------------|------|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSUBIDIR} | 0.64 | | 0.98 | | 1.08 | | ns |
| t _{INHBIDIR} | 0.00 | | 0.00 | | 0.00 | | ns |
| t _{OUTCOBIDIR} | 2.00 | 5.51 | 2.00 | 6.06 | 2.00 | 6.61 | ns |
| t _{XZBIDIR} | | 6.10 | | 6.74 | | 7.10 | ns |
| t _{ZXBIDIR} | | 6.10 | | 6.74 | | 7.10 | ns |
| t _{INSUBIDIRPLL} | 2.26 | | 2.68 | | - | | ns |
| t _{INHBIDIRPLL} | 0.00 | | 0.00 | | - | | ns |
| t _{OUTCOBIDIRPLL} | 0.50 | 2.62 | 0.50 | 2.91 | - | - | ns |
| t _{XZBIDIRPLL} | | 3.21 | | 3.59 | | - | ns |
| t _{ZXBIDIRPLL} | | 3.21 | | 3.59 | | - | ns |

Table 99. EP20K1000E t_{MAX} Routing Delays

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-------------|----------------|------|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{F1-4} | | 0.27 | | 0.27 | | 0.27 | ns |
| t_{F5-20} | | 1.45 | | 1.63 | | 1.75 | ns |
| t_{F20+} | | 4.15 | | 4.33 | | 4.97 | ns |

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{CH} | 1.25 | | 1.43 | | 1.67 | | ns |
| t_{CL} | 1.25 | | 1.43 | | 1.67 | | ns |
| t_{CLRP} | 0.20 | | 0.20 | | 0.20 | | ns |
| t_{PREP} | 0.20 | | 0.20 | | 0.20 | | ns |
| t_{ESBCH} | 1.25 | | 1.43 | | 1.67 | | ns |
| t_{ESBCL} | 1.25 | | 1.43 | | 1.67 | | ns |
| t_{ESBWP} | 1.28 | | 1.51 | | 1.65 | | ns |
| t_{ESBRP} | 1.11 | | 1.29 | | 1.41 | | ns |

Table 101. EP20K1000E External Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|----------------|----------------|------|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{INSU} | 2.70 | | 2.84 | | 2.97 | | ns |
| t_{INH} | 0.00 | | 0.00 | | 0.00 | | ns |
| t_{OUTCO} | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{INSUPLL}$ | 1.64 | | 2.09 | | - | | ns |
| t_{INHPLL} | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | - | - | ns |

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|--------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{CH} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{CL} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{CLRP} | 0.20 | | 0.20 | | 0.20 | | ns |
| t _{PREP} | 0.20 | | 0.20 | | 0.20 | | ns |
| t _{ESBCH} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{ESBCL} | 1.25 | | 1.43 | | 1.67 | | ns |
| t _{ESBWP} | 1.28 | | 1.51 | | 1.65 | | ns |
| t _{ESBRP} | 1.11 | | 1.29 | | 1.41 | | ns |

Table 107. EP20K1500E External Timing Parameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-----------------------|----------------|------|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t _{INSU} | 3.09 | | 3.30 | | 3.58 | | ns |
| t _{INH} | 0.00 | | 0.00 | | 0.00 | | ns |
| t _{OUTCO} | 2.00 | 6.18 | 2.00 | 6.81 | 2.00 | 7.36 | ns |
| t _{INSUPLL} | 1.94 | | 2.08 | | - | | ns |
| t _{INHPLL} | 0.00 | | 0.00 | | - | | ns |
| t _{OUTCOPLL} | 0.50 | 2.67 | 0.50 | 2.99 | - | - | ns |