# Intel - [EP20K400EF27C1XNGZ Datasheet](https://www.e-xfl.com/product-detail/intel/ep20k400ef27c1xngz)

**Understanding [Embedded - FPGAs (Field Programmable Gate Array)](https://www.e-xfl.com)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

## Details

| | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1664 |
| Number of Logic Elements/Cells | 16640 |
| Total RAM Bits | 212992 |
| Number of I/O | 488 |
| Number of Gates | 1052000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k400ef27c1xngz |

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

– Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions

– NativeLink™ integration with popular synthesis, simulation, and timing analysis tools

– Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation

– Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS )
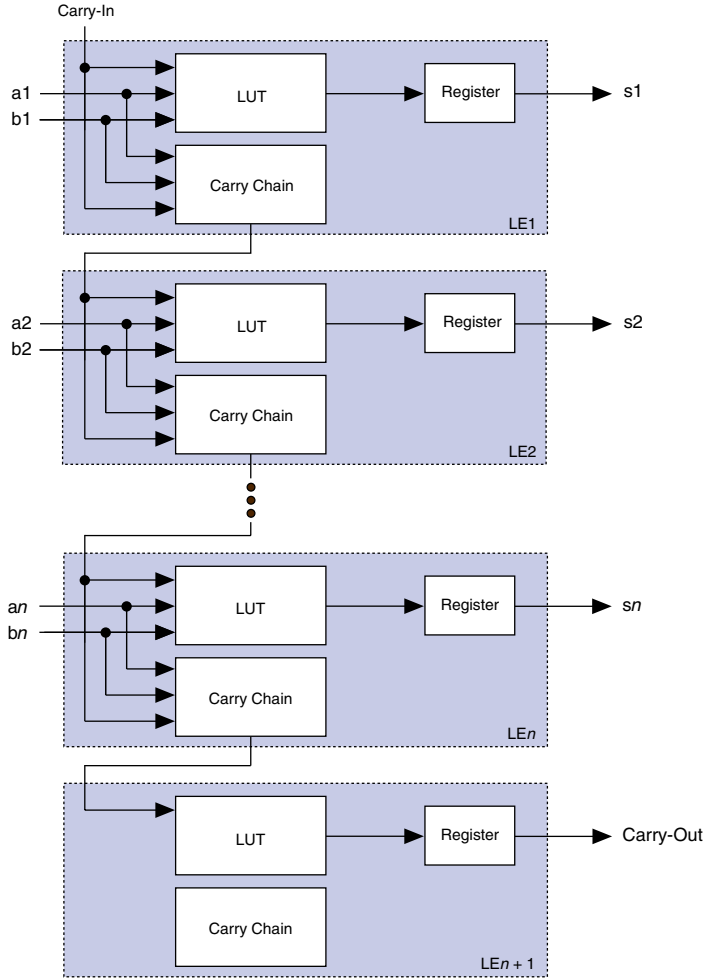
**Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count**    *Notes (1), (2)*

| Device | 144-Pin TQFP | 208-Pin PQFP RQFP | 240-Pin PQFP RQFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| EP20K30E | 92 | 125 | | | | |
| EP20K60E | 92 | 148 | 151 | 196 | | |
| EP20K100 | 101 | 159 | 189 | 252 | | |
| EP20K100E | 92 | 151 | 183 | 246 | | |
| EP20K160E | 88 | 143 | 175 | 271 | | |
| EP20K200 | | 144 | 174 | 277 | | |
| EP20K200E | | 136 | 168 | 271 | 376 | |
| EP20K300E | | | 152 | | 408 | |
| EP20K400 | | | | | 502 | 502 |
| EP20K400E | | | | | 488 | |
| EP20K600E | | | | | 488 | |
| EP20K1000E | | | | | 488 | |
| EP20K1500E | | | | | 488 | |

Altera Corporation

| *Table 8. Comparison of APEX 20K & APEX 20KE Features* | | |
|---|---|---|
| **Feature** | **APEX 20K Devices** | **APEX 20KE Devices** |
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

## Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

*Figure 5. APEX 20K Logic Element*



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

*Figure 6. APEX 20K Carry Chain*

Carry-In

a1
b1

LUT

Carry Chain

Register → s1

LE1

a2
b2

LUT

Carry Chain

Register → s2

LE2

a*n*
b*n*

LUT

Carry Chain

Register → s*n*

LE*n*

LUT
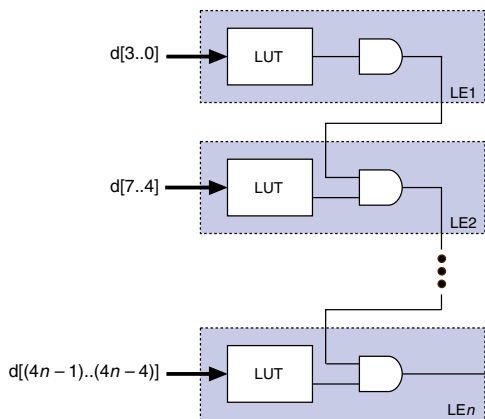
Carry Chain

Register → Carry-Out

LE*n* + 1

### Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.
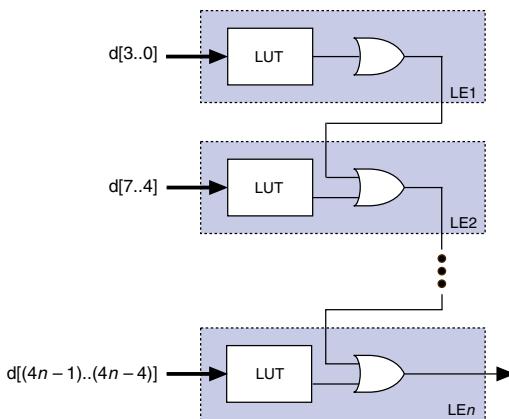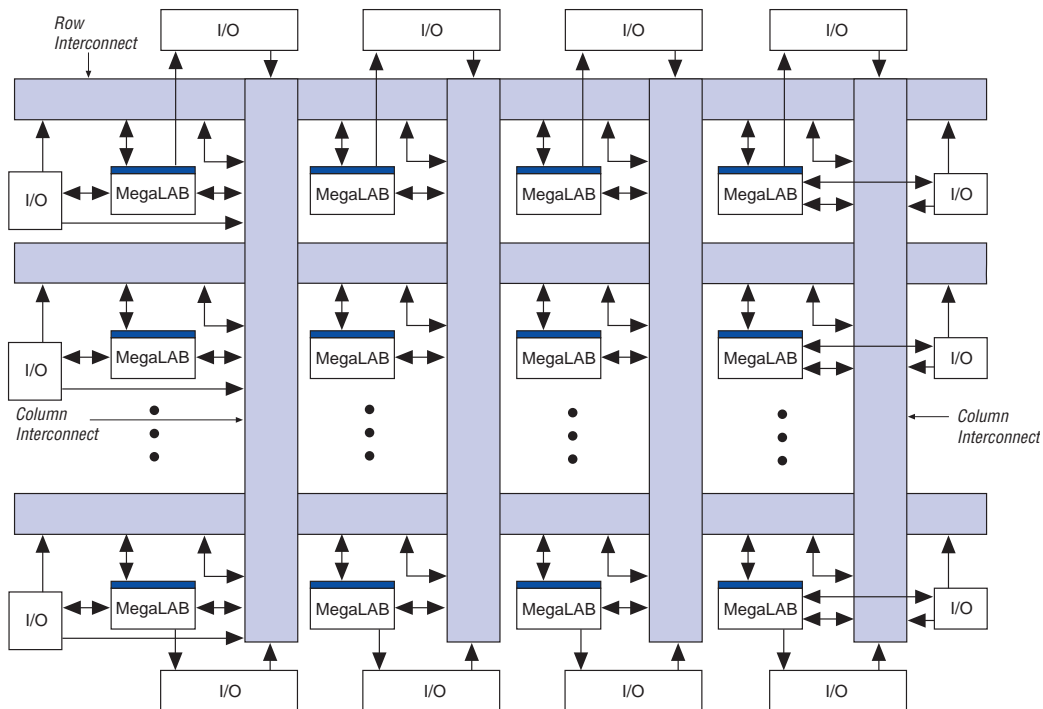
*Figure 7. APEX 20K Cascade Chain*

*Figure 9. APEX 20K Interconnect Structure*



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

### Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

### Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

*Figure 25. APEX 20K Bidirectional I/O Registers* *Note (1)*
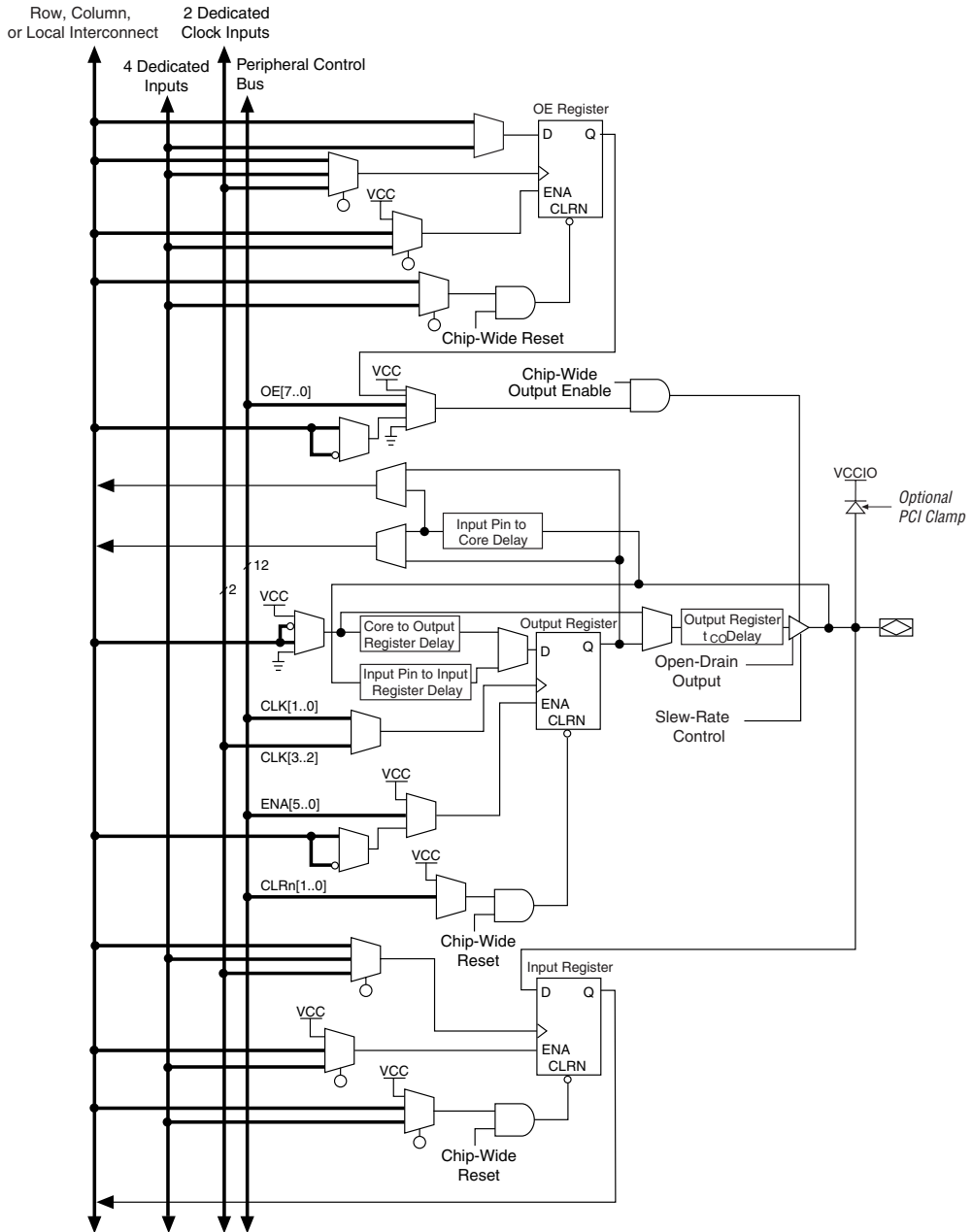


*Note to Figure 25:*
(1)     The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

### Table 11. APEX 20KE Programmable Delay Chains

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input Pin to Core Delay | Decrease input delay to internal cells |
| Input Pin to Input Register Delay | Decrease input delay to input registers |
| Core to Output Register Delay | Decrease input delay to output register |
| Output Register $t_{CO}$ Delay | Increase delay to output pin |
| Clock Enable Delay | Increase clock enable delay |

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27 shows how a row IOE connects to the interconnect.

*Figure 27. Row IOE Connection to the Interconnect*
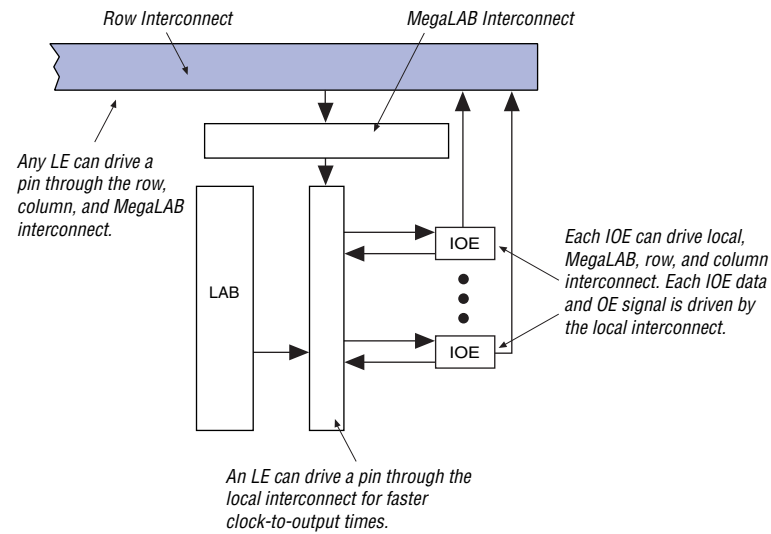
*Clock Phase & Delay Adjustment*

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

*LVDS Support*

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

*Lock Signals*

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

🖙 For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

*Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions*  *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4)*, *(5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4)*, *(5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4)*, *(5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3)*, *(6)* | −0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | °C |
| | | For industrial use | −40 | 100 | °C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions  (Part 1 of 2)*  *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{IH}$ | High-level input voltage | | 1.7, $0.5 \times V_{CCIO}$ *(9)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | −0.5 | | 0.8, $0.3 \times V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V *(10)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V *(10)* | $V_{CCIO} - 0.2$ | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V *(10)* | $0.9 \times V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V *(10)* | 2.1 | | | V |
| | | $I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V *(10)* | 2.0 | | | V |
| | | $I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V *(10)* | 1.7 | | | V |

*Figure 37. APEX 20KE f$_{MAX}$ Timing Model*

LE

$t_{SU}$
$t_{H}$
$t_{CO}$
$t_{LUT}$

Routing Delay

$t_{F1-4}$
$t_{F5-20}$
$t_{F20+}$

ESB

$t_{ESBARC}$
$t_{ESBSRC}$
$t_{ESBAWC}$
$t_{ESBSWC}$
$t_{ESBWASU}$
$t_{ESBWDSU}$
$t_{ESBSRASU}$
$t_{ESBSWDSU}$
$t_{ESBWDH}$
$t_{ESBRASU}$
$t_{ESBRAH}$
$t_{ESBWESU}$
$t_{ESBWEH}$
$t_{ESBDATASU}$
$t_{ESBWADDRSU}$
$t_{ESBRADDRSU}$
$t_{ESBDATACO1}$
$t_{ESBDATACO2}$
$t_{ESBDD}$
$t_{PD}$
$t_{PTERMSU}$
$t_{PTERMCO}$
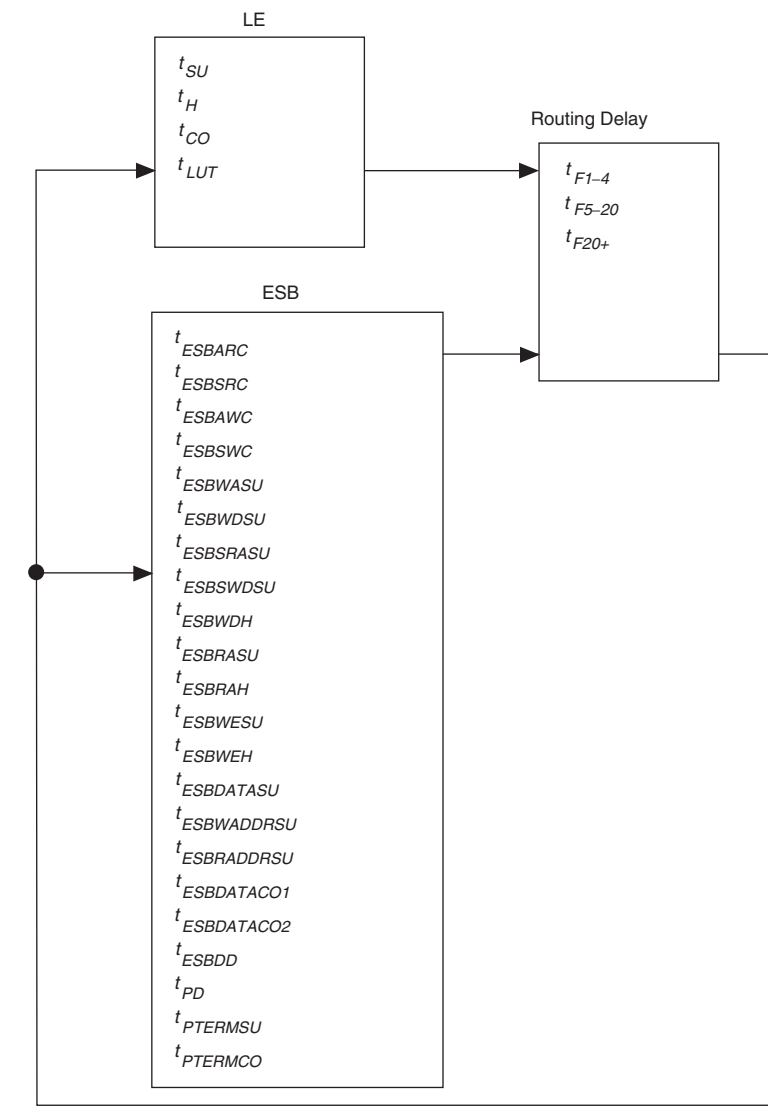
### Table 36. APEX 20KE Routing Timing Microparameters _Note (1)_

| Symbol | Parameter |
|--------|-----------|
| $t_{F1-4}$ | Fanout delay using Local Interconnect |
| $t_{F5-20}$ | Fanout delay estimate using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay estimate using FastTrack Interconnect |

_Note to Table 36:_
(1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

### Table 37. APEX 20KE Functional Timing Microparameters

| Symbol | Parameter |
|--------|-----------|
| TCH | Minimum clock high time from clock pin |
| TCL | Minimum clock low time from clock pin |
| TCLRP | LE clear Pulse Width |
| TPREP | LE preset pulse width |
| TESBCH | Clock high time for ESB |
| TESBCL | Clock low time for ESB |
| TESBWP | Write pulse width |
| TESBRP | Read pulse width |

Tables 38 and 39 describe the APEX 20KE external timing parameters.

### Table 38. APEX 20KE External Timing Parameters _Note (1)_

| Symbol | Clock Parameter | Conditions |
|--------|-----------------|------------|
| $t_{INSU}$ | Setup time with global clock at IOE input register | |
| $t_{INH}$ | Hold time with global clock at IOE input register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE output register | C1 = 10 pF |
| $t_{INSUPLL}$ | Setup time with PLL clock at IOE input register | |
| $t_{INHPLL}$ | Hold time with PLL clock at IOE input register | |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register | C1 = 10 pF |

*Notes to Tables 43 through 48:*
(1)    This parameter is measured without using ClockLock or ClockBoost circuits.
(2)    This parameter is measured using ClockLock or ClockBoost circuits.

Tables 49 through 54 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K30E APEX 20KE devices.

### Table 49. EP20K30E $f_{MAX}$ LE Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.02 | | 0.02 | | ns |
| $t_{H}$ | 0.11 | | 0.16 | | 0.23 | | ns |
| $t_{CO}$ | | 0.32 | | 0.45 | | 0.67 | ns |
| $t_{LUT}$ | | 0.85 | | 1.20 | | 1.77 | ns |

## Table 60. EP20K60E External Bidirectional Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{INSUBIDIR}$ | 2.77 | | 2.91 | | 3.11 | | ns |
| t$_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| t$_{OUTCOBIDIR}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| t$_{XZBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| t$_{ZXBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| t$_{INSUBIDIRPLL}$ | 3.44 | | 3.24 | | - | | ns |
| t$_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| t$_{OUTCOBIDIRPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |
| t$_{XZBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |
| t$_{ZXBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |

Tables 61 through 66 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

## Table 61. EP20K100E f$_{MAX}$ LE Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| t$_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| t$_{CO}$ | | 0.28 | | 0.28 | | 0.34 | ns |
| t$_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

### Table 64. EP20K100E Minimum Pulse Width Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t<sub>CH</sub> | 2.00 | | 2.00 | | 2.00 | | ns |
| t$_{CH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| t$_{CL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| t$_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| t$_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| t$_{ESBCH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| t$_{ESBCL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| t$_{ESBWP}$ | 1.29 | | 1.53 | | 1.66 | | ns |
| t$_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

### Table 65. EP20K100E External Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{INSU}$ | 2.23 | | 2.32 | | 2.43 | | ns |
| t$_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| t$_{OUTCO}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| t$_{INSUPLL}$ | 1.58 | | 1.66 | | - | | ns |
| t$_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| t$_{OUTCOPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |

### Table 66. EP20K100E External Bidirectional Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{INSUBIDIR}$ | 2.74 | | 2.96 | | 3.19 | | ns |
| t$_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| t$_{OUTCOBIDIR}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| t$_{XZBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| t$_{ZXBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| t$_{INSUBIDIRPLL}$ | 4.64 | | 5.03 | | - | | ns |
| t$_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| t$_{OUTCOBIDIRPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |
| t$_{XZBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |
| t$_{ZXBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |

## Table 69. EP20K160E f$_{MAX}$ Routing Delays

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{F1-4}$ | | 0.25 | | 0.26 | | 0.28 | ns |
| t$_{F5-20}$ | | 1.00 | | 1.18 | | 1.35 | ns |
| t$_{F20+}$ | | 1.95 | | 2.19 | | 2.30 | ns |

## Table 70. EP20K160E Minimum Pulse Width Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{CH}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| t$_{CL}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| t$_{CLRP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| t$_{PREP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| t$_{ESBCH}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| t$_{ESBCL}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| t$_{ESBWP}$ | 1.15 | | 1.45 | | 1.73 | | ns |
| t$_{ESBRP}$ | 0.93 | | 1.15 | | 1.38 | | ns |

## Table 71. EP20K160E External Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| t$_{INSU}$ | 2.23 | | 2.34 | | 2.47 | | ns |
| t$_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| t$_{OUTCO}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| t$_{INSUPLL}$ | 2.12 | | 2.07 | | - | | ns |
| t$_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| t$_{OUTCOPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |

Tables 85 through 90 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

### Table 85. EP20K400E $f_{MAX}$ LE Timing Microparameters

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_H$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{CO}$ | | 0.25 | | 0.29 | | 0.32 | ns |
| $t_{LUT}$ | | 0.70 | | 0.83 | | 1.01 | ns |

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# Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

## Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

## Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for $t_{ESBDATAH}$ parameter.

## Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

## Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.