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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	212992
Number of I/O	488
Number of Gates	1052000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k400efi672-2n">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k400efi672-2n</a>

## Functional Description

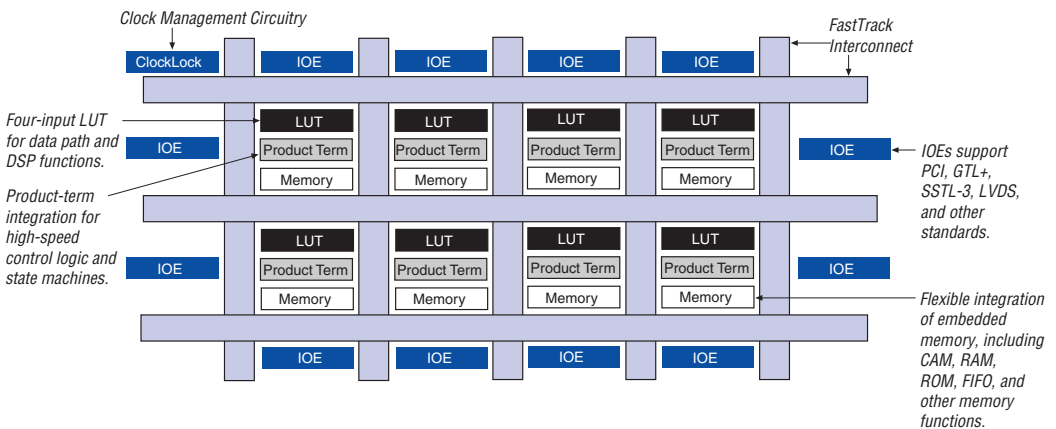
APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack<sup>®</sup> Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX 20K device.

**Figure 1. APEX 20K Device Block Diagram**

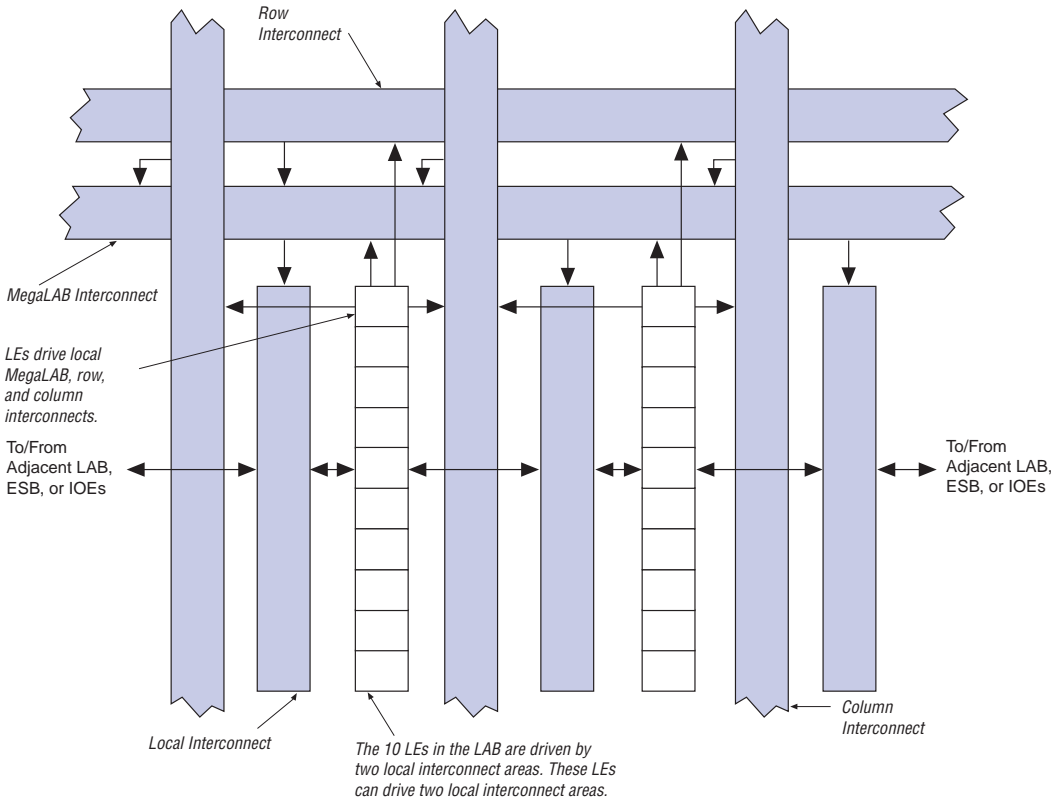


## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

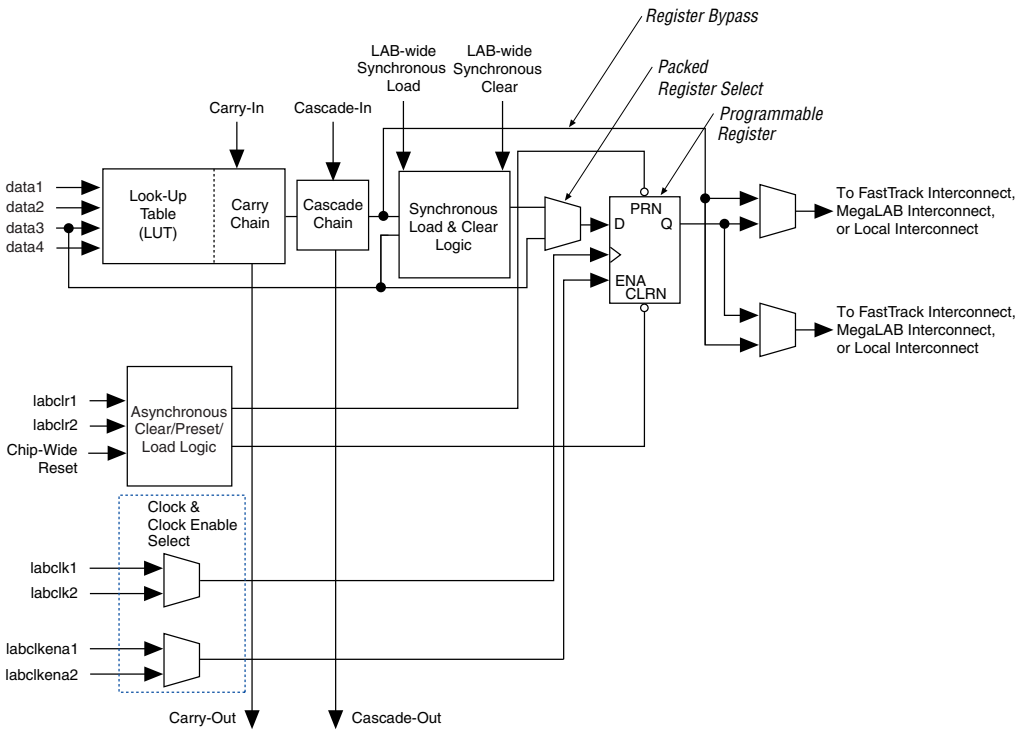
Figure 3. LAB Structure



## Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See [Figure 5](#).

**Figure 5. APEX 20K Logic Element**



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinational functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

### Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan’s inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain

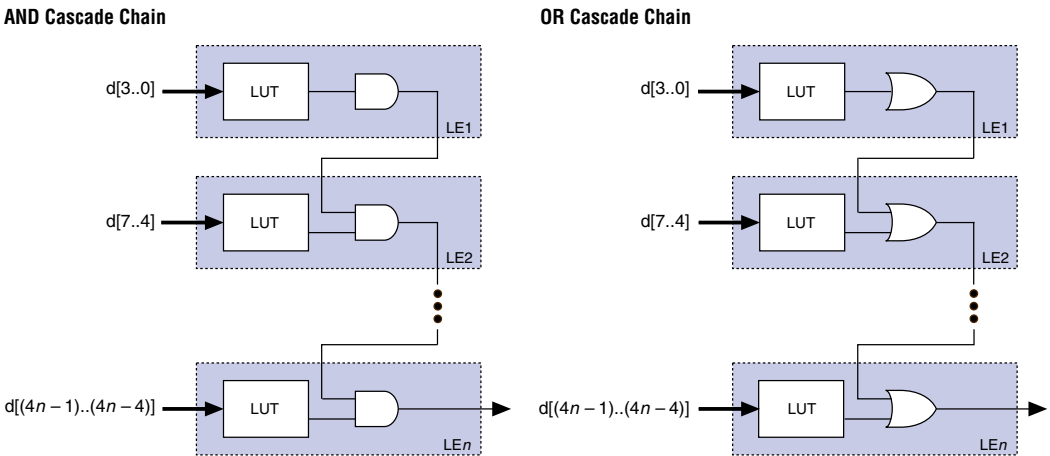
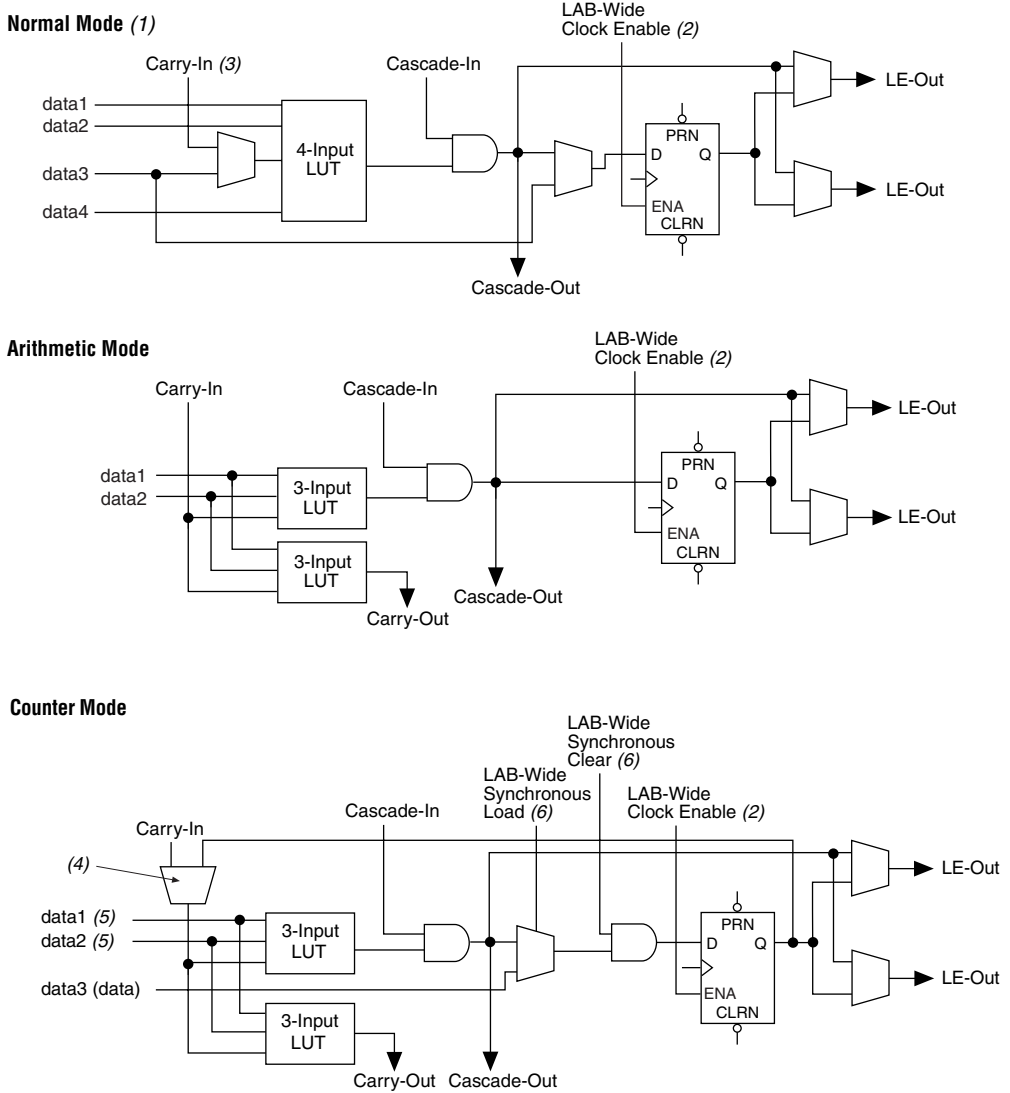


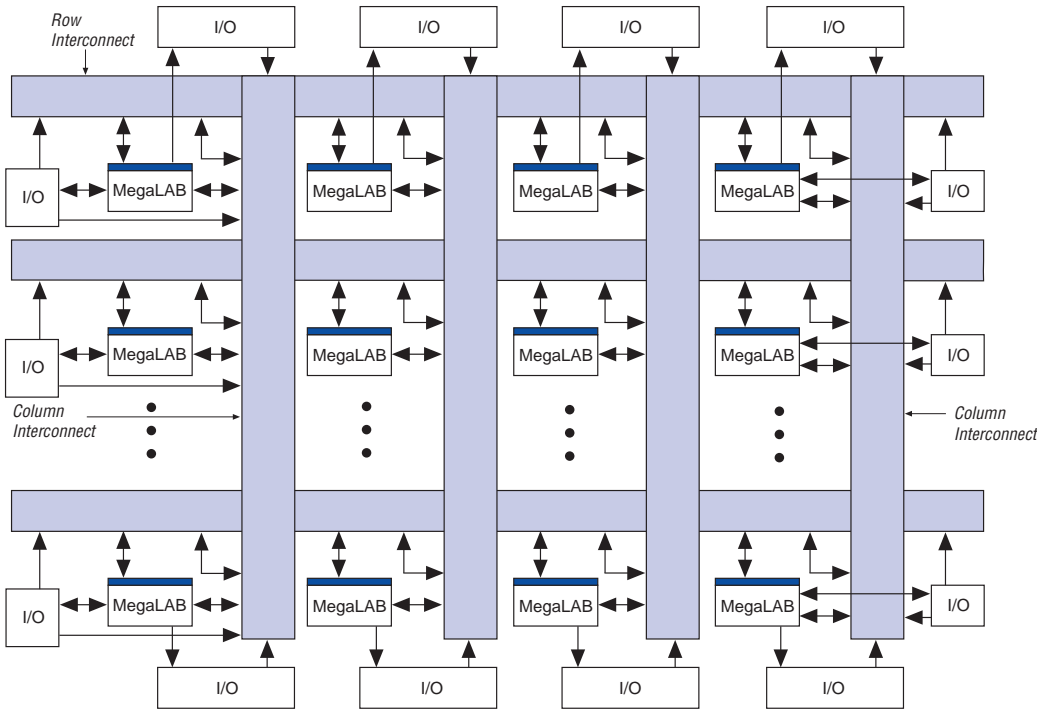
Figure 8. APEX 20K LE Operating Modes



Notes to Figure 8:

- (1) LEs in normal mode support register packing.
- (2) There are two LAB-wide clock enables per LAB.
- (3) When using the carry-in in normal mode, the packed register feature is unavailable.
- (4) A register feedback multiplexer is available on LE1 of each LAB.
- (5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in a LAB.
- (6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in a LAB.

**Figure 9. APEX 20K Interconnect Structure**

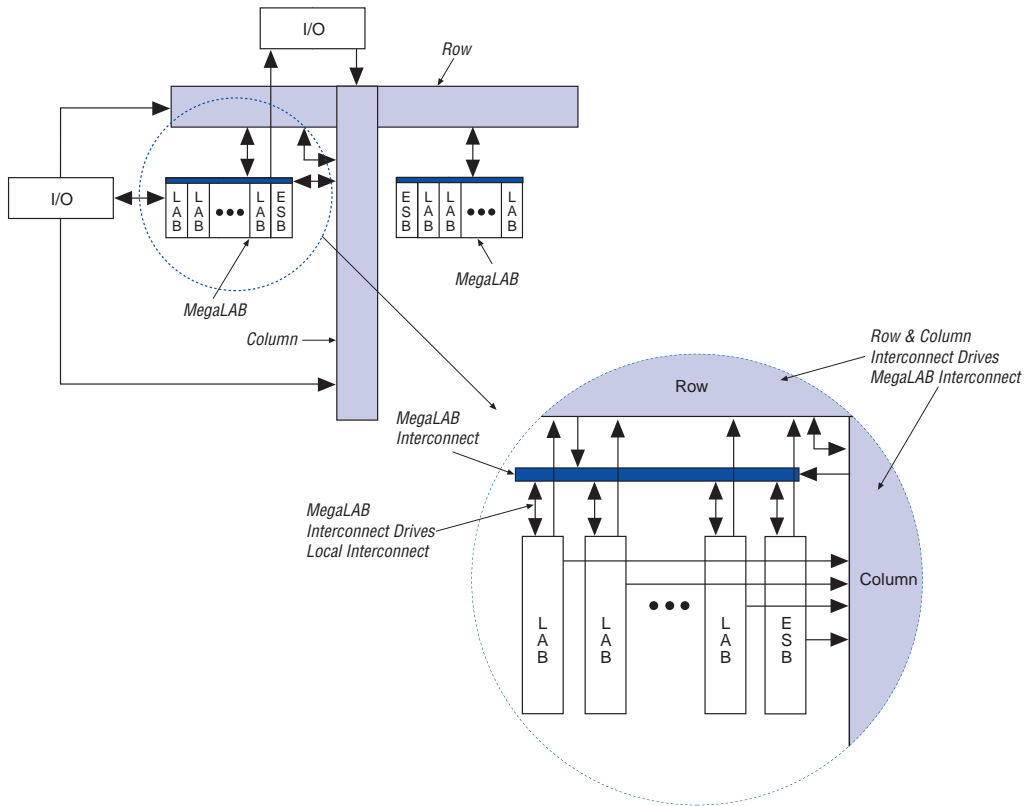


A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

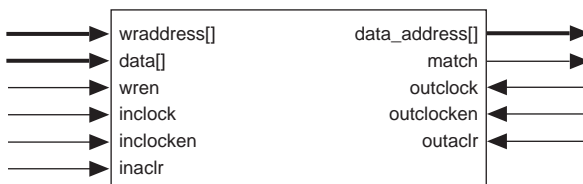
A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect





**Figure 23. APEX 20KE CAM Block Diagram**

CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing “don’t care” bits into words of the memory. The “don’t-care” bit can be used as a mask for CAM comparisons; any bit set to “don’t-care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t-care” bits are used, a third clock cycle is required.

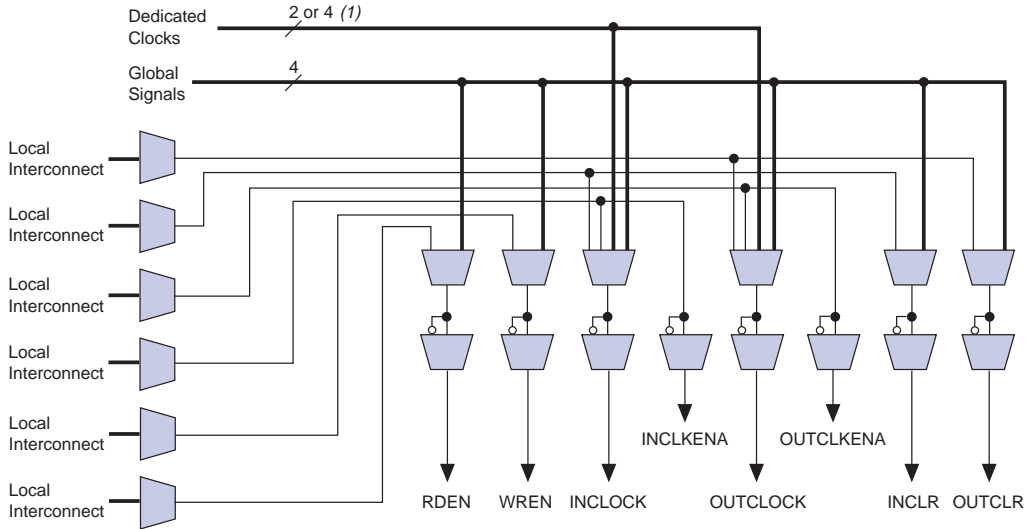


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

### Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. [Figure 24](#) shows the ESB control signal generation logic.

**Figure 24. ESB Control Signal Generation**



**Note to Figure 24:**

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.



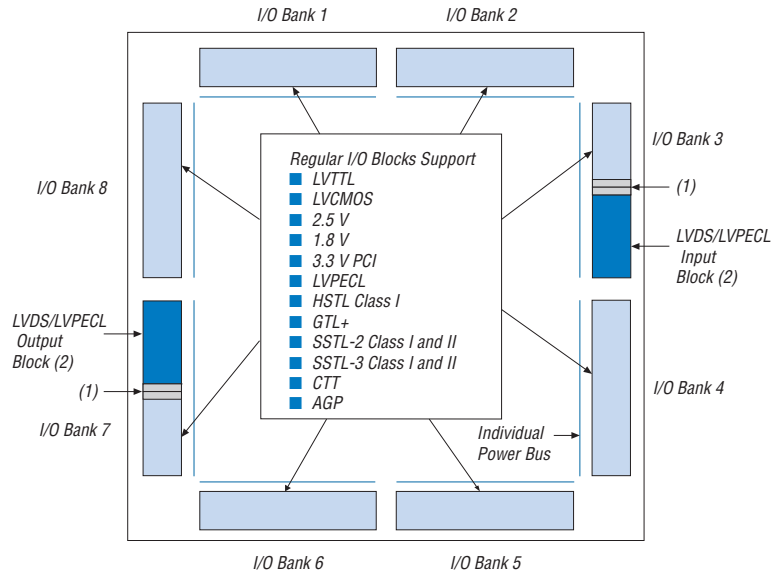
For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate  $V_{REF}$  level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. [Figure 29](#) shows the arrangement of the APEX 20KE I/O banks.

**Figure 29. APEX 20KE I/O Banks**



**Notes to Figure 29:**

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with  $V_{CCIO}$  set to 3.3 V, 2.5 V, or 1.8 V.

**Power Sequencing & Hot Socketing**

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the  $V_{CCIO}$  and  $V_{CCINT}$  power supplies may be powered in any order.



For more information, please refer to the “Power Sequencing Considerations” section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

**Table 19. APEX 20K JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS (1)	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions (1)	Monitors internal device operation with the SignalTap embedded logic analyzer.

**Note to Table 19:**

(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

**Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions** *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V <sub>CCIO</sub>	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V <sub>I</sub>	Input voltage	(3), (6)	-0.5	5.75	V
V <sub>O</sub>	Output voltage		0	V <sub>CCIO</sub>	V
T <sub>J</sub>	Junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
t <sub>R</sub>	Input rise time			40	ns
t <sub>F</sub>	Input fall time			40	ns

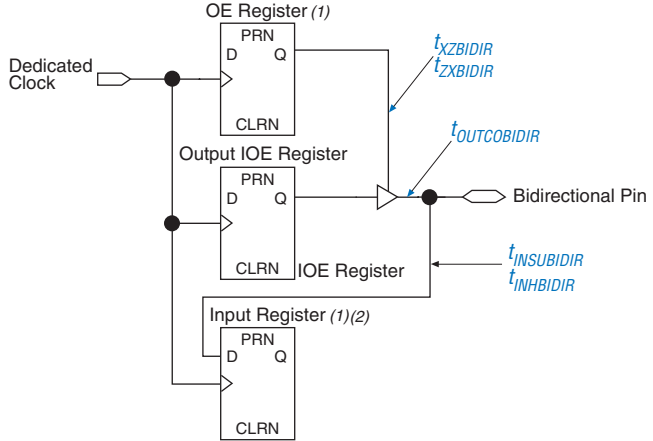
**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)** *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	High-level input voltage		1.7, 0.5 × V <sub>CCIO</sub> (9)		5.75	V
V <sub>IL</sub>	Low-level input voltage		-0.5		0.8, 0.3 × V <sub>CCIO</sub> (9)	V
V <sub>OH</sub>	3.3-V high-level TTL output voltage	I <sub>OH</sub> = -8 mA DC, V <sub>CCIO</sub> = 3.00 V (10)	2.4			V
	3.3-V high-level CMOS output voltage	I <sub>OH</sub> = -0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (10)	V <sub>CCIO</sub> - 0.2			V
	3.3-V high-level PCI output voltage	I <sub>OH</sub> = -0.5 mA DC, V <sub>CCIO</sub> = 3.00 to 3.60 V (10)	0.9 × V <sub>CCIO</sub>			V
	2.5-V high-level output voltage	I <sub>OH</sub> = -0.1 mA DC, V <sub>CCIO</sub> = 2.30 V (10)	2.1			V
		I <sub>OH</sub> = -1 mA DC, V <sub>CCIO</sub> = 2.30 V (10)	2.0			V
		I <sub>OH</sub> = -2 mA DC, V <sub>CCIO</sub> = 2.30 V (10)	1.7			V

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)** *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	3.3-V low-level TTL output voltage	I <sub>OL</sub> = 12 mA DC, V <sub>CCIO</sub> = 3.00 V (11)			0.45	V
	3.3-V low-level CMOS output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (11)			0.2	V
	3.3-V low-level PCI output voltage	I <sub>OL</sub> = 1.5 mA DC, V <sub>CCIO</sub> = 3.00 to 3.60 V (11)			0.1 × V <sub>CCIO</sub>	V
	2.5-V low-level output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 2.30 V (11)			0.2	V
I <sub>OL</sub> = 1 mA DC, V <sub>CCIO</sub> = 2.30 V (11)				0.4	V	
I <sub>OL</sub> = 2 mA DC, V <sub>CCIO</sub> = 2.30 V (11)				0.7	V	
I <sub>I</sub>	Input pin leakage current	V <sub>I</sub> = 5.75 to -0.5 V	-10		10	μA
I <sub>OZ</sub>	Tri-stated I/O pin leakage current	V <sub>O</sub> = 5.75 to -0.5 V	-10		10	μA
I <sub>CC0</sub>	V <sub>CC</sub> supply current (standby) (All ESBs in power-down mode)	V <sub>I</sub> = ground, no load, no toggling inputs, -1 speed grade (12)		10		mA
		V <sub>I</sub> = ground, no load, no toggling inputs, -2, -3 speed grades (12)		5		mA
R <sub>CONF</sub>	Value of I/O pin pull-up resistor before and during configuration	V <sub>CCIO</sub> = 3.0 V (13)	20		50	W
		V <sub>CCIO</sub> = 2.375 V (13)	30		80	W

**Figure 40. Synchronous Bidirectional Pin External Timing**



**Notes to Figure 40:**

- (1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.
- (2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the  $f_{MAX}$  timing parameters shown in Figure 36 on page 68.

<b>Table 31. APEX 20K <math>f_{MAX}</math> Timing Parameters (Part 1 of 2)</b>	
<b>Symbol</b>	<b>Parameter</b>
$t_{SU}$	LE register setup time before clock
$t_{H}$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LUT delay for data-in
$t_{ESBRC}$	ESB Asynchronous read cycle time
$t_{ESBWC}$	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBADDRSU}$	ESB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers



**Table 41. EP20K200  $f_{MAX}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.5		0.6		0.8		ns
$t_H$	0.7		0.8		1.0		ns
$t_{CO}$		0.3		0.4		0.5	ns
$t_{LUT}$		0.8		1.0		1.3	ns
$t_{ESBRC}$		1.7		2.1		2.4	ns
$t_{ESBWC}$		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
$t_{ESBDD}$		2.5		3.3		3.6	ns
$t_{PD}$		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
$t_{F1-4}$		0.5		0.6		0.7	ns
$t_{F5-20}$		1.6		1.7		1.8	ns
$t_{F20+}$		2.2		2.2		2.3	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns
$t_{CLRP}$	0.3		0.4		0.4		ns
$t_{PREP}$	0.4		0.5		0.5		ns
$t_{ESBCH}$	2.0		2.5		3.0		ns
$t_{ESBCL}$	2.0		2.5		3.0		ns
$t_{ESBWP}$	1.6		1.9		2.2		ns
$t_{ESBRP}$	1.0		1.3		1.4		ns

**Table 42. EP20K400  $f_{MAX}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.1		0.3		0.6		ns
$t_H$	0.5		0.8		0.9		ns
$t_{CO}$		0.1		0.4		0.6	ns
$t_{LUT}$		1.0		1.2		1.4	ns
$t_{ESBRC}$		1.7		2.1		2.4	ns
$t_{ESBWC}$		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
$t_{ESBDD}$		2.5		3.3		3.6	ns
$t_{PD}$		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
$t_{F1-4}$		0.4		0.5		0.6	ns
$t_{F5-20}$		2.6		2.8		2.9	ns
$t_{F20+}$		3.7		3.8		3.9	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns
$t_{CLRP}$	0.5		0.6		0.8		ns
$t_{PREP}$	0.5		0.5		0.5		ns
$t_{ESBCH}$	2.0		2.5		3.0		ns
$t_{ESBCL}$	2.0		2.5		3.0		ns
$t_{ESBWP}$	1.5		1.9		2.2		ns
$t_{ESBRP}$	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 57. EP20K60E  $f_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

**Table 62. EP20K100E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.61		1.84		1.97	ns
$t_{ESBSRC}$		2.57		2.97		3.20	ns
$t_{ESBAWC}$		0.52		4.09		4.39	ns
$t_{ESBSWC}$		3.17		3.78		4.09	ns
$t_{ESBWASU}$	0.56		6.41		0.63		ns
$t_{ESBWAH}$	0.48		0.54		0.55		ns
$t_{ESBWDSU}$	0.71		0.80		0.81		ns
$t_{ESBWDH}$	.048		0.54		0.55		ns
$t_{ESBRASU}$	1.57		1.75		1.87		ns
$t_{ESBRAH}$	0.00		0.00		0.20		ns
$t_{ESBWESU}$	1.54		1.72		1.80		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.16		-0.20		-0.20		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.12		0.08		0.13		ns
$t_{ESBRADDRSU}$	0.17		0.15		0.19		ns
$t_{ESBDATACO1}$		1.20		1.39		1.52	ns
$t_{ESBDATACO2}$		2.54		2.99		3.22	ns
$t_{ESBDD}$		3.06		3.56		3.85	ns
$t_{PD}$		1.73		2.02		2.20	ns
$t_{PTERMSU}$	1.11		1.26		1.38		ns
$t_{PTERMCO}$		1.19		1.40		1.08	ns

**Table 63. EP20K100E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.27		0.29	ns
$t_{F5-20}$		1.04		1.26		1.52	ns
$t_{F20+}$		1.12		1.36		1.86	ns

**Table 80. EP20K300E  $f_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.79		2.44		3.25	ns
$t_{ESBSRC}$		2.40		3.12		4.01	ns
$t_{ESBAWC}$		3.41		4.65		6.20	ns
$t_{ESBSWC}$		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
$t_{ESBDD}$		3.41		4.65		6.20	ns
$t_{PD}$		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

**Table 81. EP20K300E  $f_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.24		0.26	ns
$t_{F5-20}$		1.33		1.43		1.58	ns
$t_{F20+}$		3.63		3.93		4.35	ns