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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	212992
Number of I/O	-
Number of Gates	1052000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k400eri240-3

Table 5. APEX 20K FineLine BGA Package Options & I/O Count   Notes (1), (2)

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

Notes to Tables 4 and 5:
(1) I/O counts include dedicated input and clock pins.
(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 7. APEX 20K FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

Table 8. Comparison of APEX 20K & APEX 20KE Features		
Feature	**APEX 20K Devices**	**APEX 20KE Devices**
MultiCore system integration	Full support	Full support
SignalTap logic analysis	Full support	Full support
32/64-Bit, 33-MHz PCI	Full compliance in -1, -2 speed grades	Full compliance in -1, -2 speed grades
32/64-Bit, 66-MHz PCI	-	Full compliance in -1 speed grade
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device Certain devices are 5.0-V tolerant	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction $2\times$ and $4\times$ clock multiplication	Clock delay reduction $m/(n \times v)$ or $m/(n \times k)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVTTL True-LVDS and LVPECL data pins (in EP20K300E and larger devices) LVDS and LVPECL signaling (in all BGA and FineLine BGA devices) LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

Figure 8. APEX 20K LE Operating Modes
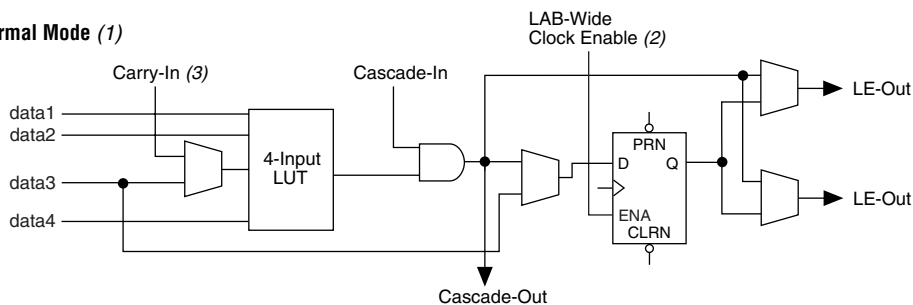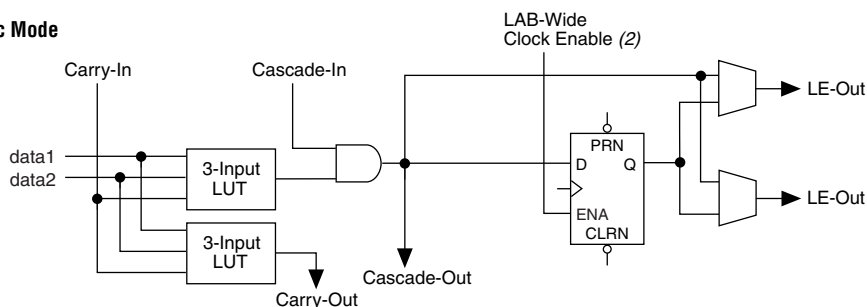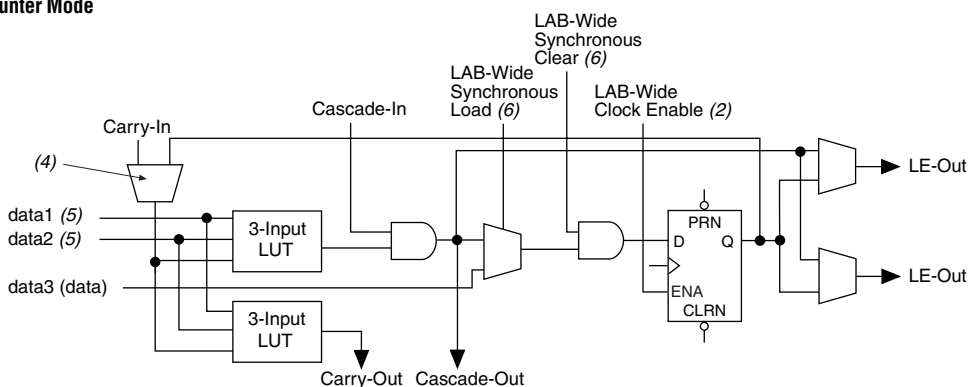
Notes to Figure 8:
(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Table 9. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin								✓	✓ *(1)*
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ *(1)*				

Note to Table 9:

(1)   This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic
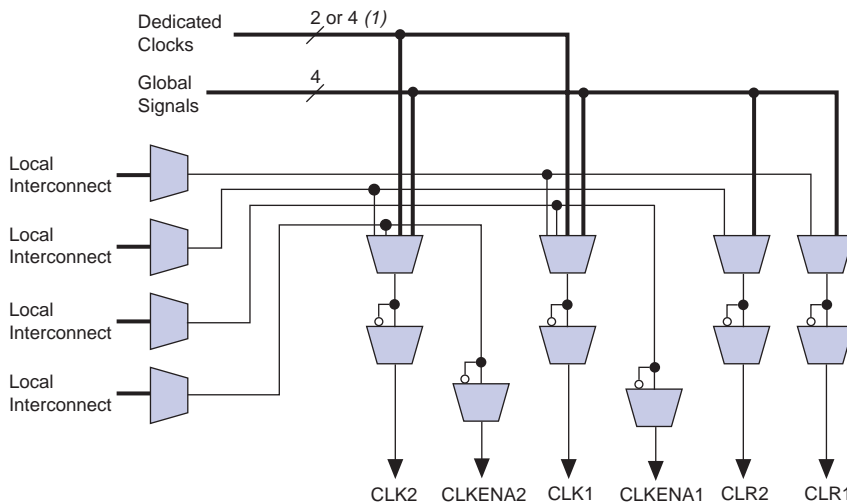
Note to Figure 15:
(1)   APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Figure 18. Deep Memory Block Implemented with Multiple ESBs
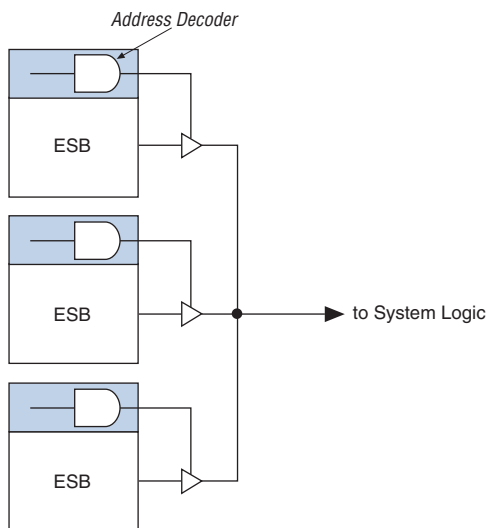
The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in Figure 19.

Figure 19. APEX 20K ESB Implementing Dual-Port RAM
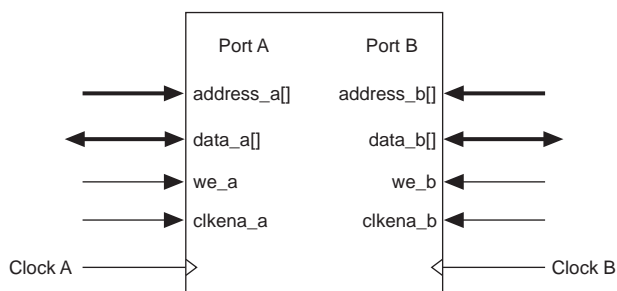
For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation
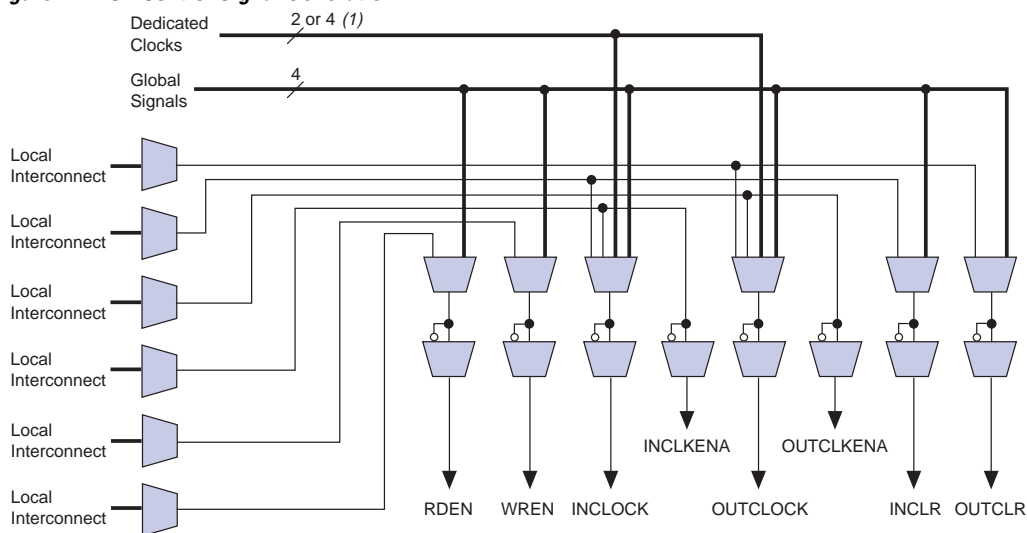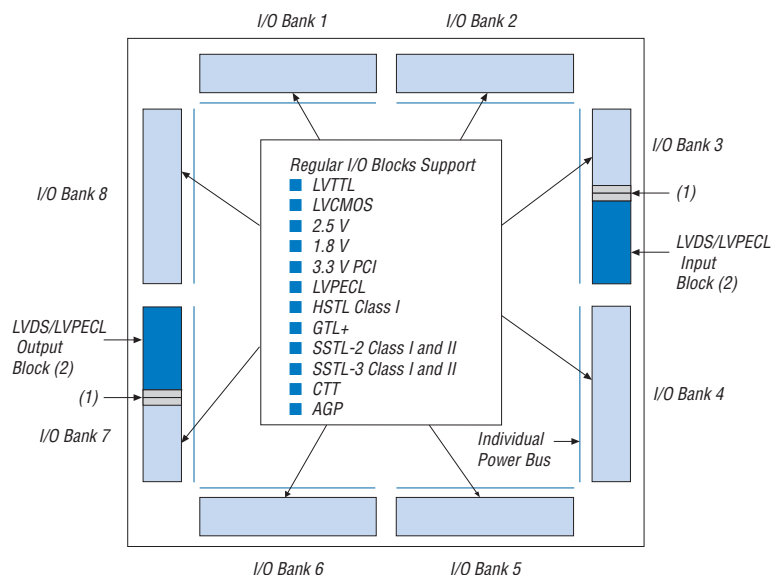

Note to Figure 24:

(1)   APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Figure 29. APEX 20KE I/O Banks

Notes to *Figure 29*:
(1)   For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
(2)   If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Figure 30. Specifications for the Incoming & Generated Clocks   Note (1)
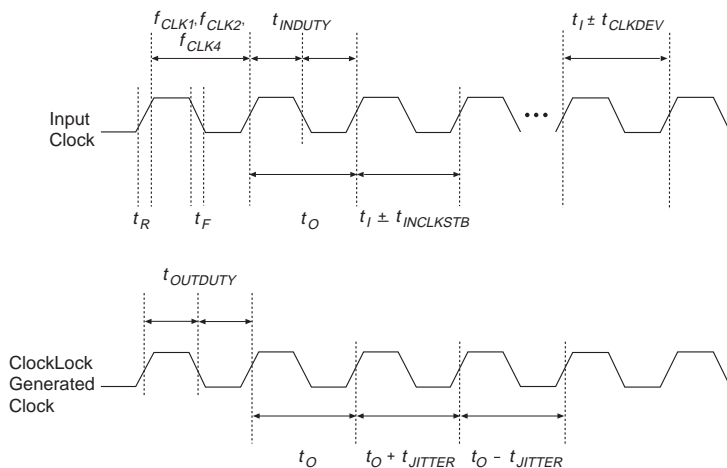
Note to Figure 30:
(1)   The tI parameter refers to the nominal input clock period; the tO parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

Symbol	Parameter	Min	Max	Unit
Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)				
f_{OUT}	Output frequency	25	180	MHz
f_{CLK1} *(1)*	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	180 *(1)*	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	90	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	48	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) *(2)*		25,000 *(3)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ClockBoost to acquire lock *(4)*		10	µs

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length	
Device	**Boundary-Scan Register Length**
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 *(1)*

Note to Table 20:
(1)   This device does not support JTAG boundary scan testing.

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

<table>
<caption>*Table 22. APEX 20K JTAG Timing Parameters & Values*</caption>
<tr><th>Symbol</th><th>Parameter</th><th>Min</th><th>Max</th><th>Unit</th></tr>
<tr><td>t_{JCP}</td><td>TCK clock period</td><td>100</td><td></td><td>ns</td></tr>
<tr><td>t_{JCH}</td><td>TCK clock high time</td><td>50</td><td></td><td>ns</td></tr>
<tr><td>t_{JCL}</td><td>TCK clock low time</td><td>50</td><td></td><td>ns</td></tr>
<tr><td>t_{JPSU}</td><td>JTAG port setup time</td><td>20</td><td></td><td>ns</td></tr>
<tr><td>t_{JPH}</td><td>JTAG port hold time</td><td>45</td><td></td><td>ns</td></tr>
<tr><td>t_{JPCO}</td><td>JTAG port clock to output</td><td></td><td>25</td><td>ns</td></tr>
<tr><td>t_{JPZX}</td><td>JTAG port high impedance to valid output</td><td></td><td>25</td><td>ns</td></tr>
<tr><td>t_{JPXZ}</td><td>JTAG port valid output to high impedance</td><td></td><td>25</td><td>ns</td></tr>
<tr><td>t_{JSSU}</td><td>Capture register setup time</td><td>20</td><td></td><td>ns</td></tr>
<tr><td>t_{JSH}</td><td>Capture register hold time</td><td>45</td><td></td><td>ns</td></tr>
<tr><td>t_{JSCO}</td><td>Update register clock to output</td><td></td><td>35</td><td>ns</td></tr>
<tr><td>t_{JSZX}</td><td>Update register high impedance to valid output</td><td></td><td>35</td><td>ns</td></tr>
<tr><td>t_{JSXZ}</td><td>Update register valid output to high impedance</td><td></td><td>35</td><td>ns</td></tr>
</table>

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

Table 26. APEX 20K 5.0-V Tolerant Device Capacitance   *Notes (2), (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 23 through 26:
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A= 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
(10) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
(11) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 27. APEX 20KE Device Absolute Maximum Ratings   *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f$_{MAX}$ Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t$_{SU}$	0.5		0.6		0.8		ns
t$_H$	0.7		0.8		1.0		ns
t$_{CO}$		0.3		0.4		0.5	ns
t$_{LUT}$		0.8		1.0		1.3	ns
t$_{ESBRC}$		1.7		2.1		2.4	ns
t$_{ESBWC}$		5.7		6.9		8.1	ns
t$_{ESBWESU}$	3.3		3.9		4.6		ns
t$_{ESBDATASU}$	2.2		2.7		3.1		ns
t$_{ESBDATAH}$	0.6		0.8		0.9		ns
t$_{ESBADDRSU}$	2.4		2.9		3.3		ns
t$_{ESBDATACO1}$		1.3		1.6		1.8	ns
t$_{ESBDATACO2}$		2.6		3.1		3.6	ns
t$_{ESBDD}$		2.5		3.3		3.6	ns
t$_{PD}$		2.5		3.0		3.6	ns
t$_{PTERMSU}$	2.3		2.6		3.2		ns
t$_{PTERMCO}$		1.5		1.8		2.1	ns
t$_{F1-4}$		0.5		0.6		0.7	ns
t$_{F5-20}$		1.6		1.7		1.8	ns
t$_{F20+}$		2.2		2.2		2.3	ns
t$_{CH}$	2.0		2.5		3.0		ns
t$_{CL}$	2.0		2.5		3.0		ns
t$_{CLRP}$	0.3		0.4		0.4		ns
t$_{PREP}$	0.5		0.5		0.5		ns
t$_{ESBCH}$	2.0		2.5		3.0		ns
t$_{ESBCL}$	2.0		2.5		3.0		ns
t$_{ESBWP}$	1.6		1.9		2.2		ns
t$_{ESBRP}$	1.0		1.3		1.4		ns

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.3		2.8		3.2		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.3		2.8		3.2		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.0		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.9		2.3		2.6		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	–	ns

Altera Corporation

Table 62. EP20K100E f_MAX ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_ESBARC		1.61		1.84		1.97	ns
t_ESBSRC		2.57		2.97		3.20	ns
t_ESBAWC		0.52		4.09		4.39	ns
t_ESBSWC		3.17		3.78		4.09	ns
t_ESBWASU	0.56		6.41		0.63		ns
t_ESBWAH	0.48		0.54		0.55		ns
t_ESBWDSU	0.71		0.80		0.81		ns
t_ESBWDH	.048		0.54		0.55		ns
t_ESBRASU	1.57		1.75		1.87		ns
t_ESBRAH	0.00		0.00		0.20		ns
t_ESBWESU	1.54		1.72		1.80		ns
t_ESBWEH	0.00		0.00		0.00		ns
t_ESBDATASU	-0.16		-0.20		-0.20		ns
t_ESBDATAH	0.13		0.13		0.13		ns
t_ESBWADDRSU	0.12		0.08		0.13		ns
t_ESBRADDRSU	0.17		0.15		0.19		ns
t_ESBDATACO1		1.20		1.39		1.52	ns
t_ESBDATACO2		2.54		2.99		3.22	ns
t_ESBDD		3.06		3.56		3.85	ns
t_PD		1.73		2.02		2.20	ns
t_PTERMSU	1.11		1.26		1.38		ns
t_PTERMCO		1.19		1.40		1.08	ns

Table 63. EP20K100E f_MAX Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_F1-4		0.24		0.27		0.29	ns
t_F5-20		1.04		1.26		1.52	ns
t_F20+		1.12		1.36		1.86	ns

Table 69. EP20K160E f$_{MAX}$ Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.25		0.26		0.28	ns
t$_{F5-20}$		1.00		1.18		1.35	ns
t$_{F20+}$		1.95		2.19		2.30	ns

Table 70. EP20K160E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{CH}$	1.34		1.43		1.55		ns
t$_{CL}$	1.34		1.43		1.55		ns
t$_{CLRP}$	0.18		0.19		0.21		ns
t$_{PREP}$	0.18		0.19		0.21		ns
t$_{ESBCH}$	1.34		1.43		1.55		ns
t$_{ESBCL}$	1.34		1.43		1.55		ns
t$_{ESBWP}$	1.15		1.45		1.73		ns
t$_{ESBRP}$	0.93		1.15		1.38		ns

Table 71. EP20K160E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSU}$	2.23		2.34		2.47		ns
t$_{INH}$	0.00		0.00		0.00		ns
t$_{OUTCO}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
t$_{INSUPLL}$	2.12		2.07		-		ns
t$_{INHPLL}$	0.00		0.00		-		ns
t$_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns

Table 98. EP20K1000E f_MAX ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
t_{ESBWASU}	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
t_{ESBWDSU}	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
t_{ESBRASU}	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
t_{ESBWESU}	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
t_{ESBDATASU}	0.25		0.27		0.29		ns
t_{ESBDATAH}	0.13		0.13		0.13		ns
t_{ESBWADDRSU}	0.11		0.04		0.11		ns
t_{ESBRADDRSU}	0.14		0.11		0.16		ns
t_{ESBDATACO1}		1.29		1.50		1.63	ns
t_{ESBDATACO2}		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
t_{PTERMSU}	1.08		1.19		1.32		ns
t_{PTERMCO}		1.31		1.53		1.66	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSUBIDIR}$	3.47		3.68		3.99		ns
t$_{INHBIDIR}$	0.00		0.00		0.00		ns
t$_{OUTCOBIDIR}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
t$_{XZBIDIR}$		6.91		7.62		8.38	ns
t$_{ZXBIDIR}$		6.91		7.62		8.38	ns
t$_{INSUBIDIRPLL}$	3.05		3.26				ns
t$_{INHBIDIRPLL}$	0.00		0.00				ns
t$_{OUTCOBIDIRPLL}$	0.50	2.67	0.50	2.99			ns
t$_{XZBIDIRPLL}$		3.41		3.80			ns
t$_{ZXBIDIRPLL}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		−0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		−0.24		−0.23		−0.19	ns
SSTL-3 Class I		−0.32		−0.21		−0.47	ns
SSTL-3 Class II		−0.08		0.03		−0.23	ns
SSTL-2 Class I		−0.17		−0.06		−0.32	ns
SSTL-2 Class II		−0.16		−0.05		−0.31	ns
LVDS		−0.12		−0.12		−0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns