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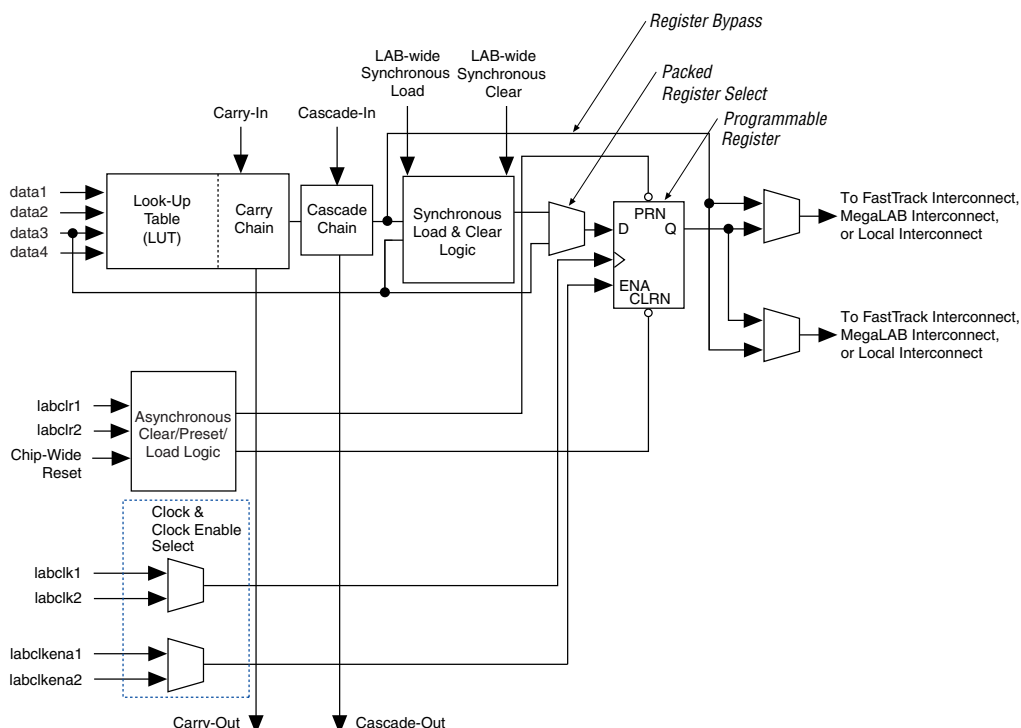
Details

Product Status	Obsolete
Number of LABs/CLBs	2432
Number of Logic Elements/Cells	24320
Total RAM Bits	311296
Number of I/O	488
Number of Gates	1537000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k600ebc652-3

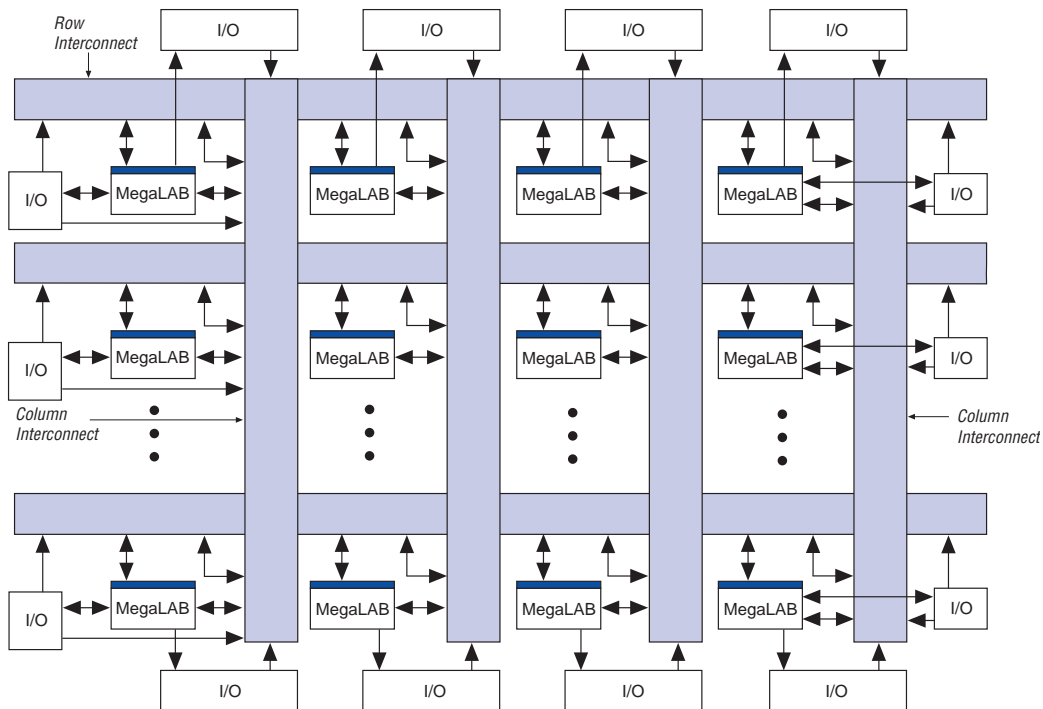
Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See [Figure 5](#).

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Figure 9. APEX 20K Interconnect Structure

A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Table 9. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin								✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ (1)				

Note to Table 9:

(1) This connection is supported in APEX 20KE devices only.

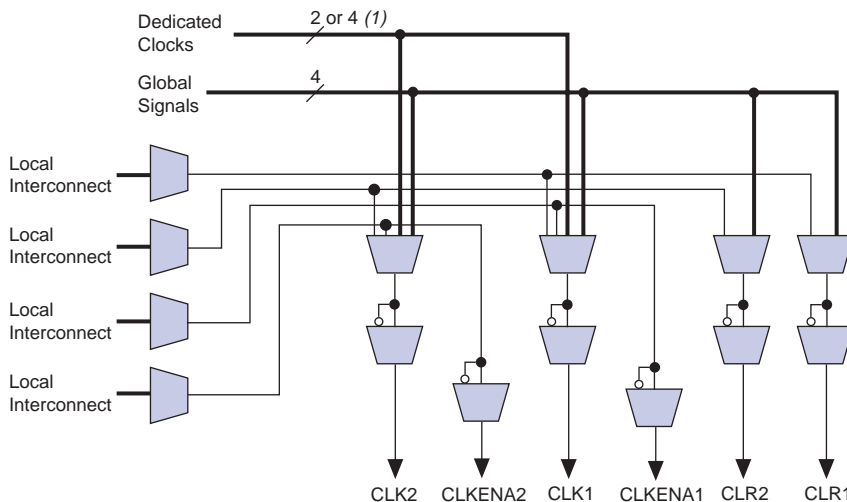
Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. [Figure 13](#) shows the ESB in product-term mode.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Note to Figure 15:

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

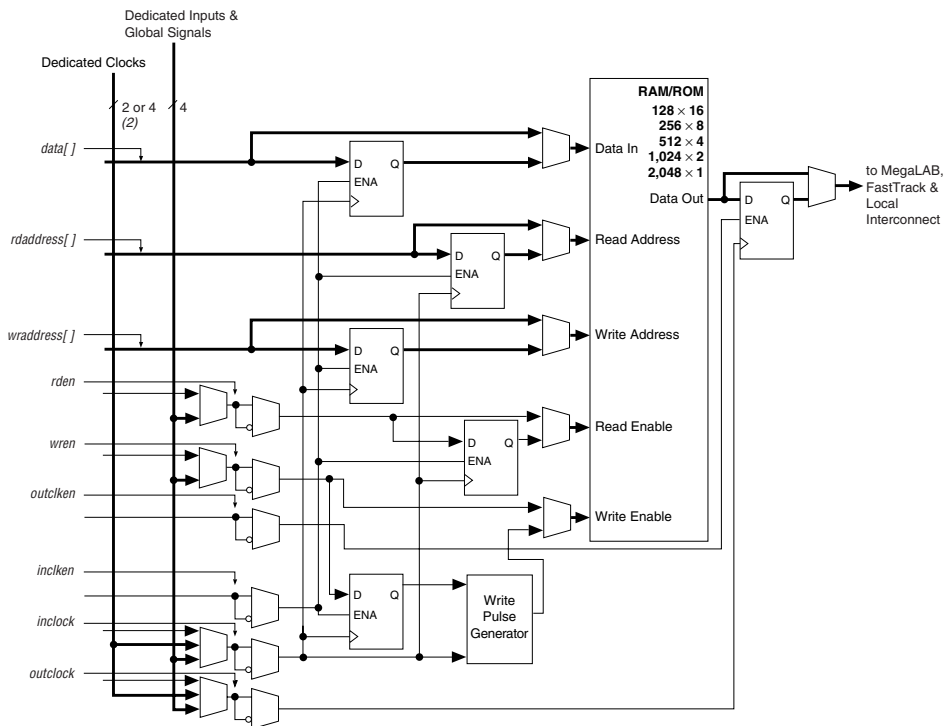
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode Note (1)



Notes to Figure 21:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

Table 11. APEX 20KE Programmable Delay Chains	
Programmable Delays	Quartus II Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. **Figure 26** shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. [Figure 30](#) shows the incoming and generated clock specifications.



For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock (5)		200	ps
t_{INCLKSTB}	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:

- (1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
- (2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
- (4) The jitter specification is measured under long-term observation.
- (5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
t_{OUTDUTY}	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) (1)		25,000 (2)	PPM
t_{R}	Input rise time		5	ns
t_{F}	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock (3)		10	μs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock (4)		200	ps
t_{INCLKSTB}	Input clock stability (measured between adjacent clocks)		50	ps

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) ⁽¹⁾			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) ⁽²⁾
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 21:

- (1) The most significant bit (MSB) is on the left.
 (2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

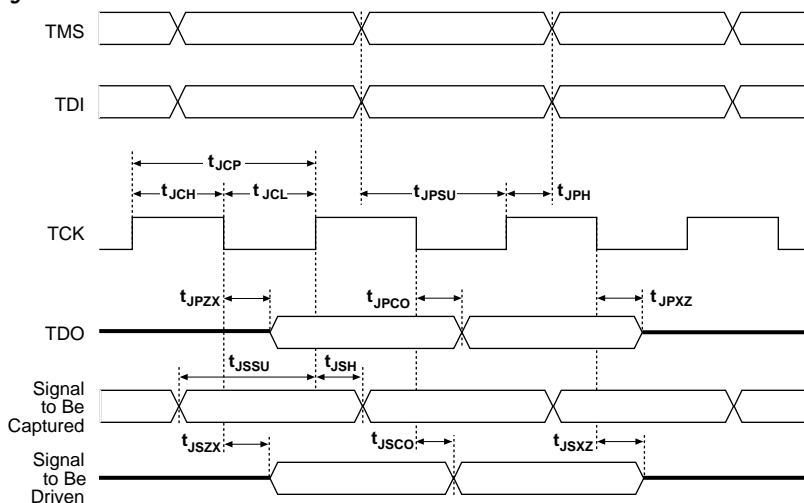
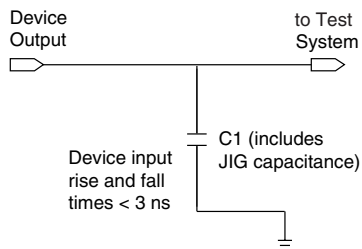
Figure 31. APEX 20K JTAG Waveforms

Figure 32. APEX 20K AC Test Conditions *Note (1)*


Note to Figure 32:

- (1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (3)	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I			–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

Table 26. APEX 20K 5.0-V Tolerant Device Capacitance *Notes (2), (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF

Notes to Tables 23 through 26:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) All APEX 20K devices are 5.0-V tolerant.
- (3) Minimum DC input is -0.5 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns .
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Maximum V_{CC} rise time is 100 ms , and V_{CC} must rise monotonically.
- (6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (7) Typical values are for $T_A = 25^\circ\text{C}$, $V_{CCINT} = 2.5\text{ V}$, and $V_{CCIO} = 2.5\text{ V}$ or 3.3 V .
- (8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
- (9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTTL and LVC MOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
- (10) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
- (11) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (12) This value is specified for normal device operation. The value may vary during power-up.
- (13) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO} .
- (14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 27. APEX 20KE Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (2)	-0.5	2.5	V
V_{CCIO}			-0.5	4.6	V
V_I			-0.5	4.6	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	$^\circ\text{C}$
T_{AMB}	Ambient temperature	Under bias	-65	135	$^\circ\text{C}$
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	$^\circ\text{C}$
		Ceramic PGA packages, under bias		150	$^\circ\text{C}$

Figure 39. ESB Synchronous Timing Waveforms

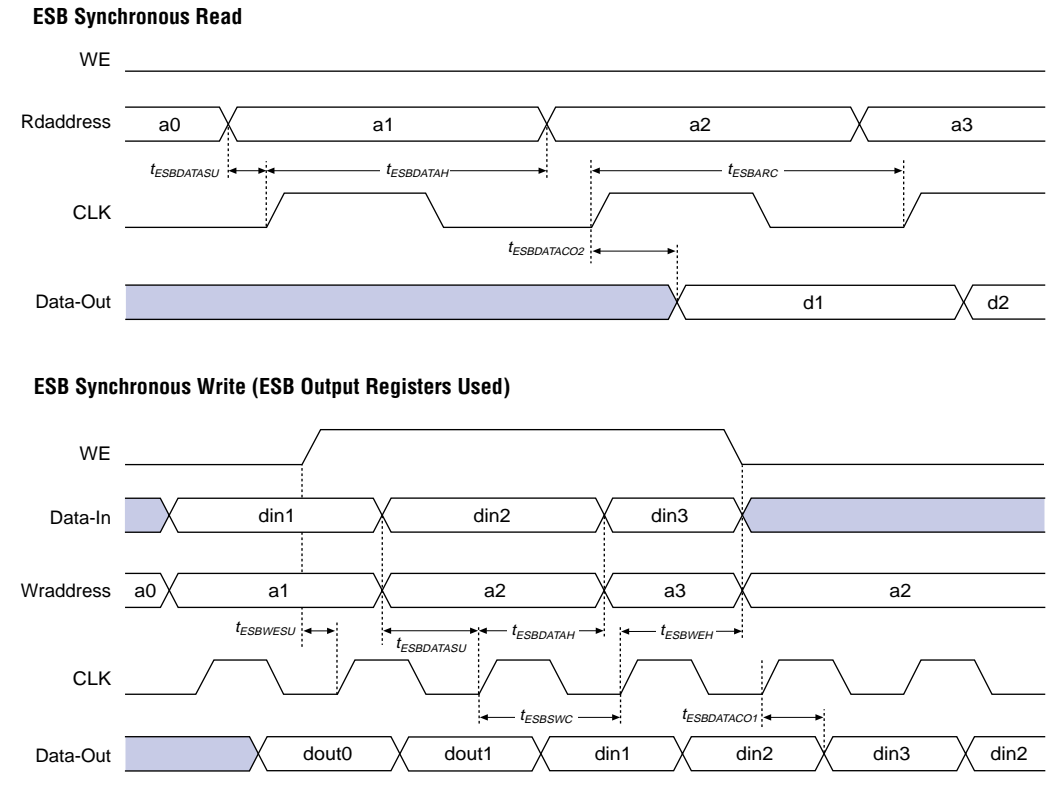


Figure 40 shows the timing model for bidirectional I/O pin timing.

Table 41. EP20K200 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_H	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.4		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 42. EP20K400 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.1		0.3		0.6		ns
t_H	0.5		0.8		0.9		ns
t_{CO}		0.1		0.4		0.6	ns
t_{LUT}		1.0		1.2		1.4	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
t_{F1-4}		0.4		0.5		0.6	ns
t_{F5-20}		2.6		2.8		2.9	ns
t_{F20+}		3.7		3.8		3.9	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.5		0.6		0.8		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.5		1.9		2.2		ns
t_{ESBRP}	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Tables 67 through 72 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

Table 67. EP20K160E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.24		0.26		ns
t_H	0.22		0.24		0.26		ns
t_{CO}		0.25		0.31		0.35	ns
t_{LUT}		0.69		0.88		1.12	ns

Table 68. EP20K160E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.65		2.02		2.11	ns
t_{ESBSRC}		2.21		2.70		3.11	ns
t_{ESBAWC}		3.04		3.79		4.42	ns
t_{ESBSWC}		2.81		3.56		4.10	ns
$t_{ESBWASU}$	0.54		0.66		0.73		ns
t_{ESBWAH}	0.36		0.45		0.47		ns
$t_{ESBWDSU}$	0.68		0.81		0.94		ns
t_{ESBWDH}	0.36		0.45		0.47		ns
$t_{ESBRASU}$	1.58		1.87		2.06		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.41		1.71		2.00		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.02		-0.03		0.09		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.14		0.17		0.35		ns
$t_{ESBRADDRSU}$	0.21		0.27		0.43		ns
$t_{ESBDATACO1}$		1.04		1.30		1.46	ns
$t_{ESBDATACO2}$		2.15		2.70		3.16	ns
t_{ESBDD}		2.69		3.35		3.97	ns
t_{PD}		1.55		1.93		2.29	ns
$t_{PTERMSU}$	1.01		1.23		1.52		ns
$t_{PTERMCO}$		1.06		1.32		1.04	ns

Table 74. EP20K200E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.68		2.06		2.24	ns
t_{ESBSRC}		2.27		2.77		3.18	ns
t_{ESBAWC}		3.10		3.86		4.50	ns
t_{ESBSWC}		2.90		3.67		4.21	ns
$t_{ESBWASU}$	0.55		0.67		0.74		ns
t_{ESBWAH}	0.36		0.46		0.48		ns
$t_{ESBWDSU}$	0.69		0.83		0.95		ns
t_{ESBWDH}	0.36		0.46		0.48		ns
$t_{ESBRASU}$	1.61		1.90		2.09		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.42		1.71		2.01		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.06		-0.07		0.05		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.13		0.31		ns
$t_{ESBRADDRSU}$	0.18		0.23		0.39		ns
$t_{ESBDATAO1}$		1.09		1.35		1.51	ns
$t_{ESBDATAO2}$		2.19		2.75		3.22	ns
t_{ESBDD}		2.75		3.41		4.03	ns
t_{PD}		1.58		1.97		2.33	ns
$t_{PTERMSU}$	1.00		1.22		1.51		ns
$t_{PTERMCO}$		1.10		1.37		1.09	ns

Table 75. EP20K200E t_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.27		0.29	ns
t_{F5-20}		1.02		1.20		1.41	ns
t_{F20+}		1.99		2.23		2.53	ns

Table 82. EP20K300E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.25		1.43		1.67		ns
t _{CL}	1.25		1.43		1.67		ns
t _{CLRP}	0.19		0.26		0.35		ns
t _{PREP}	0.19		0.26		0.35		ns
t _{ESBCH}	1.25		1.43		1.67		ns
t _{ESBCL}	1.25		1.43		1.67		ns
t _{ESBWP}	1.25		1.71		2.28		ns
t _{ESBRP}	1.01		1.38		1.84		ns

Table 83. EP20K300E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.31		2.44		2.57		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.29	2.00	5.82	2.00	6.24	ns
t _{INSUPLL}	1.76		1.85		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.65	0.50	2.95	-	-	ns

Table 84. EP20K300E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	2.77		2.85		3.11		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	5.29	2.00	5.82	2.00	6.24	ns
t _{XZBIDIR}		7.59		8.30		9.09	ns
t _{ZXBIDIR}		7.59		8.30		9.09	ns
t _{INSUBIDIRPLL}	2.50		2.76		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.65	0.50	2.95	-	-	ns
t _{XZBIDIRPLL}		5.00		5.43		-	ns
t _{ZXBIDIRPLL}		5.00		5.43		-	ns

Table 92. EP20K600E t_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		2.39		3.11	ns
t_{ESBSRC}		2.27		3.07		3.86	ns
t_{ESBAWC}		3.19		4.56		5.93	ns
t_{ESBSWC}		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATAO1}$		1.01		1.19		1.37	ns
$t_{ESBDATAO2}$		2.18		3.12		4.05	ns
t_{ESBDD}		3.19		4.56		5.93	ns
t_{PD}		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

Table 93. EP20K600E t_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.25		0.26	ns
t_{F5-20}		1.26		1.39		1.52	ns
t_{F20+}		3.51		3.88		4.26	ns

Table 94. EP20K600E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	2.00		2.50		2.75		ns
t _{CL}	2.00		2.50		2.75		ns
t _{CLRP}	0.18		0.26		0.34		ns
t _{PREP}	0.18		0.26		0.34		ns
t _{ESBCH}	2.00		2.50		2.75		ns
t _{ESBCL}	2.00		2.50		2.75		ns
t _{ESBWP}	1.17		1.68		2.18		ns
t _{ESBRP}	0.95		1.35		1.76		ns

Table 95. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.74		2.74		2.87		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.51	2.00	6.06	2.00	6.61	ns
t _{INSUPLL}	1.86		1.96		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.62	0.50	2.91	-	-	ns

Table 96. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	0.64		0.98		1.08		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	5.51	2.00	6.06	2.00	6.61	ns
t _{XZBIDIR}		6.10		6.74		7.10	ns
t _{ZXBIDIR}		6.10		6.74		7.10	ns
t _{INSUBIDIRPLL}	2.26		2.68		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.62	0.50	2.91	-	-	ns
t _{XZBIDIRPLL}		3.21		3.59		-	ns
t _{ZXBIDIRPLL}		3.21		3.59		-	ns