



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2432
Number of Logic Elements/Cells	24320
Total RAM Bits	311296
Number of I/O	508
Number of Gates	1537000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k600ef672c1xgz">https://www.e-xfl.com/product-detail/intel/ep20k600ef672c1xgz</a>

## General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an “E” suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). [Table 8](#) compares the features included in APEX 20K and APEX 20KE devices.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

### *Carry Chain*

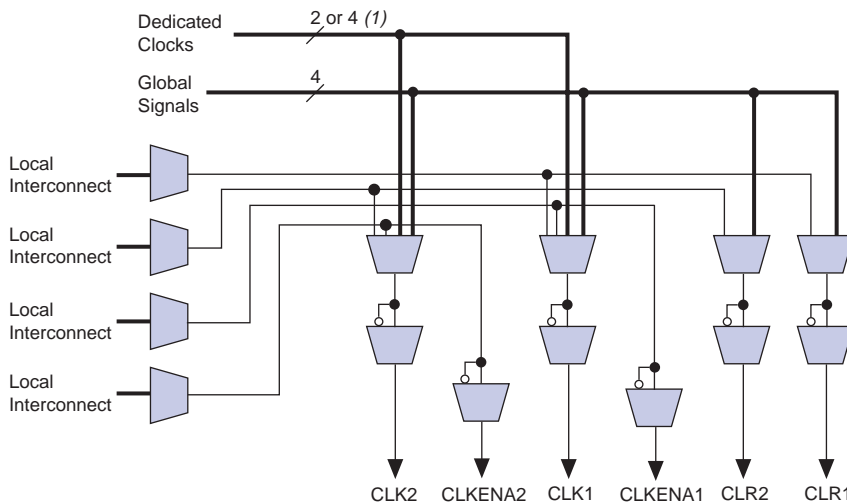
The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

**Figure 15. ESB Product-Term Mode Control Logic**



**Note to Figure 15:**

(1) APEX 20KE devices have four dedicated clocks.

### Parallel Expanders

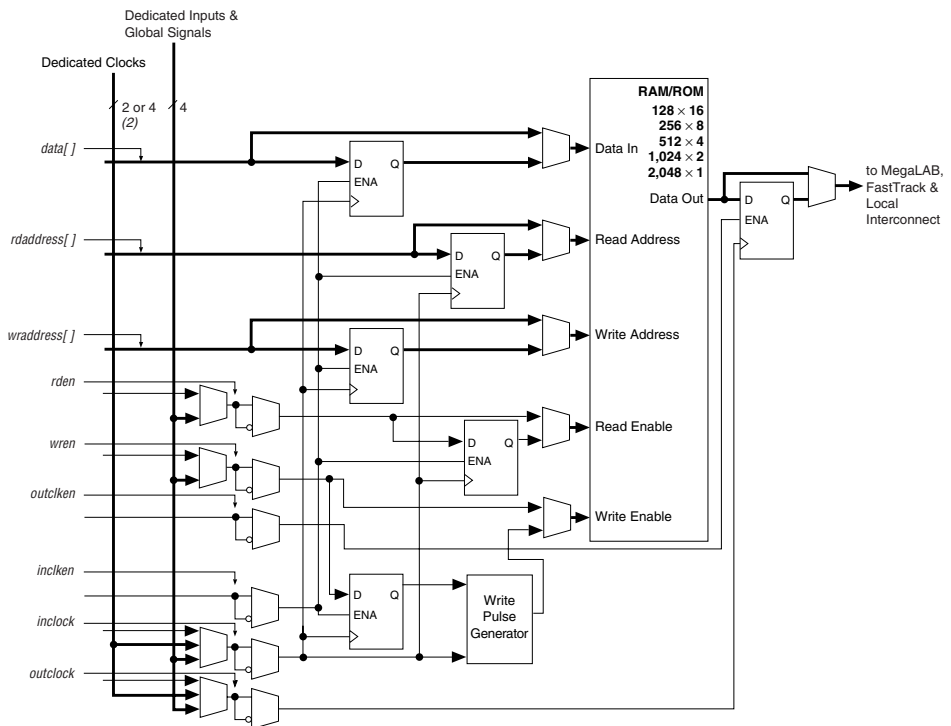
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

**Figure 21. ESB in Input/Output Clock Mode** Note (1)



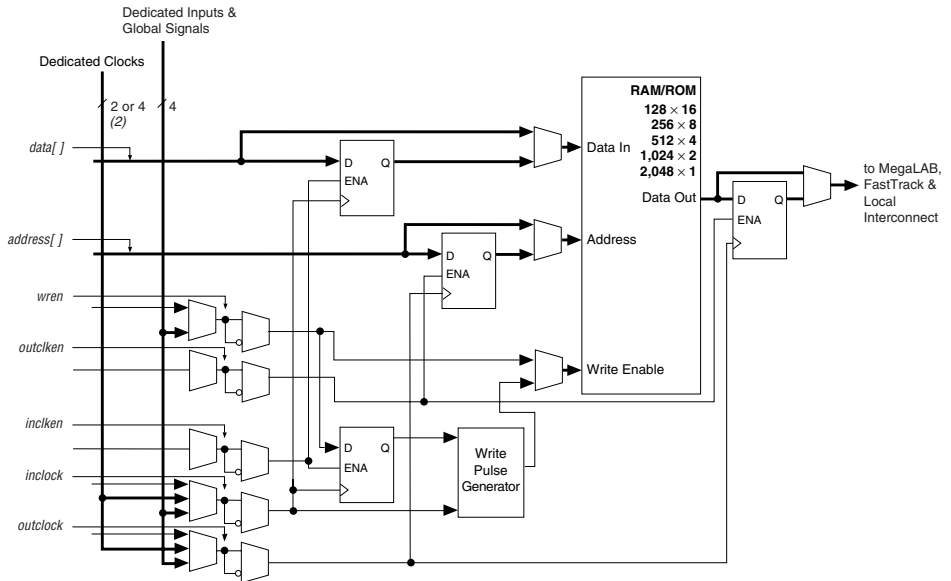
### Notes to Figure 21:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



Notes to Figure 22:

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

<b>Table 10. APEX 20K Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register $t_{CO}$ delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V VCCINT level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

<b>Table 13. APEX 20KE MultiVolt I/O Support</b> <i>Note (1)</i>								
V <sub>CCIO</sub> (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓	(2)			✓(3)	

**Notes to Table 13:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V<sub>CCIO</sub>, except for the 5.0-V input case.
- (2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.
- (3) When V<sub>CCIO</sub> = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.



For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

**Table 14. Multiplication Factor Combinations**

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

## APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

### *External PLL Feedback*

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

### *Clock Multiplication*

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by  $m/(n \times k)$  or  $m/(n \times v)$ , where  $m$  and  $k$  range from 2 to 160, and  $n$  and  $v$  range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

**Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions** *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
$V_I$	Input voltage	(3), (6)	−0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Junction temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)** *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (9)		5.75	V
$V_{IL}$	Low-level input voltage		−0.5		$0.8, 0.3 \times V_{CCIO}$ (9)	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (10)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (10)	1.7			V

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the  $f_{MAX}$  timing model for APEX 20K devices.

**Figure 36. APEX 20K  $t_{MAX}$  Timing Model**

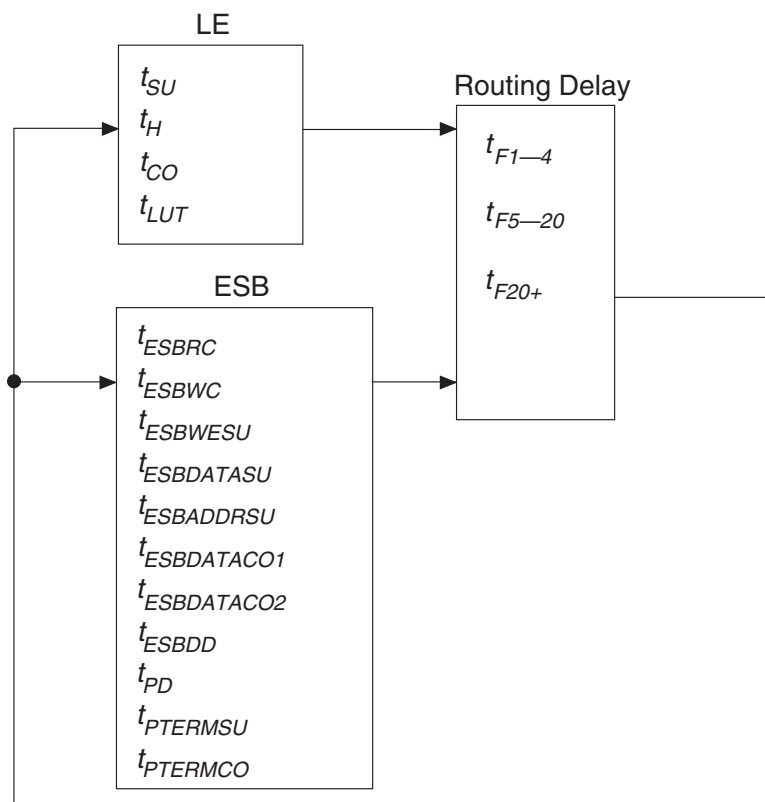


Figure 37 shows the  $f_{MAX}$  timing model for APEX 20KE devices. These parameters can be used to estimate  $f_{MAX}$  for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Figure 39. ESB Synchronous Timing Waveforms

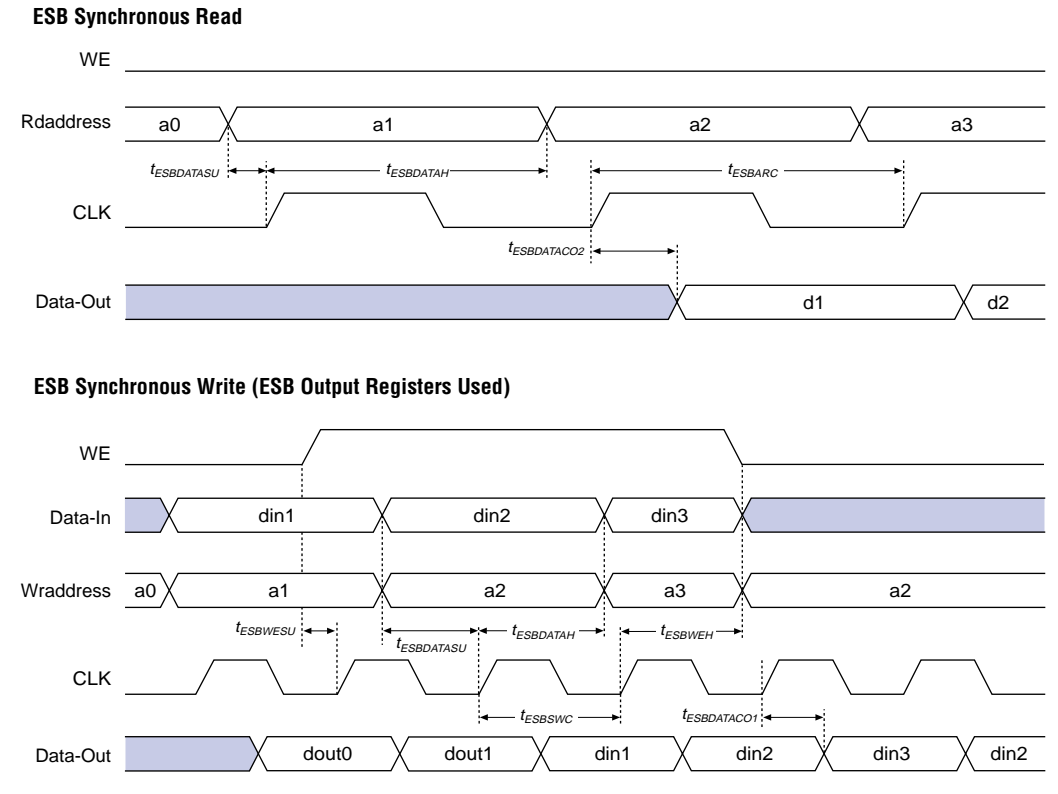


Figure 40 shows the timing model for bidirectional I/O pin timing.

**Table 31. APEX 20K  $t_{MAX}$  Timing Parameters (Part 2 of 2)**

Symbol	Parameter
$t_{ESB\text{DATA}CO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
$t_{F1-4}$	Fanout delay using local interconnect
$t_{F5-20}$	Fanout delay using MegaLab Interconnect
$t_{F20+}$	Fanout delay using FastTrack Interconnect
$t_{CH}$	Minimum clock high time from clock pin
$t_{CL}$	Minimum clock low time from clock pin
$t_{CLRP}$	LE clear pulse width
$t_{PREP}$	LE preset pulse width
$t_{ESBCH}$	Clock high time
$t_{ESBCL}$	Clock low time
$t_{ESBWP}$	Write pulse width
$t_{ESBRP}$	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

**Table 32. APEX 20K External Timing Parameters Note (1)**

Symbol	Clock Parameter
$t_{INSU}$	Setup time with global clock at IOE register
$t_{INH}$	Hold time with global clock at IOE register
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE register

**Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)**

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INH\text{BIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCO\text{BIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZ\text{BIDIR}}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF

**Table 46. EP20K200 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.9		2.3		2.6		ns
$t_{\text{INHBIDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{\text{XZBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{ZXBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{INSUBIDIR}} (2)$	1.1		1.2		—		ns
$t_{\text{INHBIDIR}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	2.7	0.5	3.1	—	—	ns
$t_{\text{XZBIDIR}} (2)$		4.3		5.0		—	ns
$t_{\text{ZXBIDIR}} (2)$		4.3		5.0		—	ns

**Table 47. EP20K400 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INH}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{INSU}} (2)$	0.4		1.0		—		ns
$t_{\text{INH}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCO}} (2)$	0.5	3.1	0.5	4.1	—	—	ns

**Table 48. EP20K400 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INHBIDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{XZBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{ZXBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{INSUBIDIR}} (2)$	0.5		1.0		—		ns
$t_{\text{INHBIDIR}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	3.1	0.5	4.1	—	—	ns
$t_{\text{XZBIDIR}} (2)$		6.2		7.6		—	ns
$t_{\text{ZXBIDIR}} (2)$		6.2		7.6		—	ns

**Table 52. EP20K30E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	0.55		0.78		1.15		ns
t <sub>CL</sub>	0.55		0.78		1.15		ns
t <sub>CLRP</sub>	0.22		0.31		0.46		ns
t <sub>PREP</sub>	0.22		0.31		0.46		ns
t <sub>ESBCH</sub>	0.55		0.78		1.15		ns
t <sub>ESBCL</sub>	0.55		0.78		1.15		ns
t <sub>ESBWP</sub>	1.43		2.01		2.97		ns
t <sub>ESBRP</sub>	1.15		1.62		2.39		ns

**Table 53. EP20K30E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.02		2.13		2.24		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>INSUPLL</sub>	2.11		2.23		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns

**Table 54. EP20K30E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	1.85		1.77		1.54		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.88	2.00	5.36	2.00	5.88	ns
t <sub>XZBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>ZXBIDIR</sub>		7.48		8.46		9.83	ns
t <sub>INSUBIDIRPLL</sub>	4.12		4.24		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.60	0.50	2.88	-	-	ns
t <sub>XZBIDIRPLL</sub>		5.21		5.99		-	ns
t <sub>ZXBIDIRPLL</sub>		5.21		5.99		-	ns

Tables 55 through 60 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

**Table 55. EP20K60E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.17		0.15		0.16		ns
$t_H$	0.32		0.33		0.39		ns
$t_{CO}$		0.29		0.40		0.60	ns
$t_{LUT}$		0.77		1.07		1.59	ns



**Table 57. EP20K60E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

**Table 94. EP20K600E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	2.00		2.50		2.75		ns
t <sub>CL</sub>	2.00		2.50		2.75		ns
t <sub>CLRP</sub>	0.18		0.26		0.34		ns
t <sub>PREP</sub>	0.18		0.26		0.34		ns
t <sub>ESBCH</sub>	2.00		2.50		2.75		ns
t <sub>ESBCL</sub>	2.00		2.50		2.75		ns
t <sub>ESBWP</sub>	1.17		1.68		2.18		ns
t <sub>ESBRP</sub>	0.95		1.35		1.76		ns

**Table 95. EP20K600E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.74		2.74		2.87		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	5.51	2.00	6.06	2.00	6.61	ns
t <sub>INSUPLL</sub>	1.86		1.96		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.62	0.50	2.91	-	-	ns

**Table 96. EP20K600E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	0.64		0.98		1.08		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	5.51	2.00	6.06	2.00	6.61	ns
t <sub>XZBIDIR</sub>		6.10		6.74		7.10	ns
t <sub>ZXBIDIR</sub>		6.10		6.74		7.10	ns
t <sub>INSUBIDIRPLL</sub>	2.26		2.68		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.62	0.50	2.91	-	-	ns
t <sub>XZBIDIRPLL</sub>		3.21		3.59		-	ns
t <sub>ZXBIDIRPLL</sub>		3.21		3.59		-	ns

Tables 97 through 102 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

**Table 97. EP20K1000E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.25		0.25		0.25		ns
$t_H$	0.25		0.25		0.25		ns
$t_{CO}$		0.28		0.32		0.33	ns
$t_{LUT}$		0.80		0.95		1.13	ns

**Table 102. EP20K1000E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.22		3.33		3.51		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{\text{XZBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{ZXBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.25		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.25	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		2.81		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		2.81		3.80			ns

Tables 103 through 108 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

**Table 103. EP20K1500E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.32		0.33	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$  added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).