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Intel - EP20K60EFC144-2XN Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2560
Number of Logic Elements/Cells	2560
Total RAM Bits	32768
Number of I/O	93
Number of Gates	162000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-BGA
Supplier Device Package	144-FBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k60efc144-2xn

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
 - Built-in low-skew clock tree
 - Up to eight global clock signals
 - ClockLock[®] feature reducing clock delay and skew
 - ClockBoost[®] feature providing clock multiplication and division
 - ClockShiftTM programmable clock phase and delay shifting
- Powerful I/O features
 - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) PCI Local Bus Specification, Revision 2.2 for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
 - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
 - Bidirectional I/O performance $(t_{CO} + t_{SU})$ up to 250 MHz
 - LVDS performance up to 840 Mbits per channel
 - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
 - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
 - Programmable clamp to V_{CCIO}
 - Individual tri-state output enable control for each pin
 - Programmable output slew-rate control to reduce switching noise
 - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stubseries terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
 - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
 - Four-level hierarchical FastTrack[®] Interconnect structure providing fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
 - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
 - FineLine BGA[®] packages maximize board space efficiency
- Advanced software support
 - Software design support and automatic place-and-route provided by the Altera[®] Quartus[®] II development system for

APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLABTM structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.







Figure 6. APEX 20K Carry Chain

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Table 9. AP	EX 20K	Routing S	Scheme								
Source	Destination										
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect		
Row I/O Pin					✓	~	~	~			
Column I/O Pin								~	✓ (1)		
LE					~	~	~	~			
ESB					 Image: A set of the set of the	~	~	~			
Local Interconnect	~	~	~	~							
MegaLAB Interconnect					~						
Row FastTrack Interconnect						~		~			
Column FastTrack Interconnect						~	~				
FastRow Interconnect					✓ (1)						

Note to Table 9:

(1) This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

Figure 13. Product-Term Logic in ESB



Note to Figure 13:

(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The productterm select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell. The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.



Figure 15. ESB Product-Term Mode Control Logic

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.





Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.







For more information on APEX 20KE devices and CAM, see *Application* Note 119 (Implementing High-Speed Search Applications with APEX CAM).

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.





(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.



Figure 25. APEX 20K Bidirectional I/O Registers Note (1)



Altera Corporation

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.



For more information on I/O standards supported by APEX 20KE devices, see *Application Note* 117 (*Using Selectable I/O Standards in Altera Devices*).

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output levels are some supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output levels are some supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output levels are some supply. The output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output levels are some supply. The output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

Table 13. /	Table 13. APEX 20KE MultiVolt I/O Support Note (1)									
V _{CCIO} (V)		Input Siç	jnals (V)		Output Signals (V)					
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0		
1.8	\checkmark	\checkmark	\checkmark		\checkmark					
2.5	\checkmark	\checkmark	>			\checkmark				
3.3	\checkmark	\checkmark	\checkmark	(2)			✓(3)			

Notes to Table 13:

 The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

(3) When $V_{CCIO} = 3.3 \text{ V}$, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices.

Table 2	4. APEX 20K 5.0-V Tolerant D	Device Recommended Operating Condition	ns Note (2	2)	
Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
VI	Input voltage	(3), (6)	-0.5	5.75	V
Vo	Output voltage		0	V _{CCIO}	V
ТJ	Junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Table 2	5. APEX 20K 5.0-V Tolerant De	vice DC Operating Con	ditions (Part 1 o	f 2)	Notes (2), (7), (a	8)
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IH}	High-level input voltage		1.7, 0.5 × V _{CCIO} (9)		5.75	V
V _{IL}	Low-level input voltage		-0.5		$0.8, 0.3 \times V_{CCIO}$	V
V _{OH}	3.3-V high-level TTL output voltage	I _{OH} = -8 mA DC, V _{CCIO} = 3.00 V <i>(10)</i>	2.4			V
	3.3-V high-level CMOS output voltage	I _{OH} = -0.1 mA DC, V _{CCIO} = 3.00 V <i>(10)</i>	V _{CCIO} - 0.2			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5 \text{ mA DC},$ $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (10)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I _{OH} = -0.1 mA DC, V _{CCIO} = 2.30 V <i>(10)</i>	2.1			V
		I _{OH} = -1 mA DC, V _{CCIO} = 2.30 V (10)	2.0			V
		$I_{OH} = -2 \text{ mA DC},$ $V_{CCIO} = 2.30 \text{ V} (10)$	1.7			V

Table 2	Table 26. APEX 20K 5.0-V Tolerant Device Capacitance Notes (2), (14)								
Symbol	Parameter	Conditions	Min	Max	Unit				
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		8	pF				
CINCLK	Input capacitance on dedicated clock pin	V _{IN} = 0 V, f = 1.0 MHz		12	pF				
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		8	pF				

Notes to Tables 23 through 26:

- (1) See the Operating Requirements for Altera Devices Data Sheet.
- All APEX 20K devices are 5.0-V tolerant. (2)
- (3) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
- Numbers in parentheses are for industrial-temperature-range devices. (4)
- Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically. (5)
- All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are (6) powered.
- (7)Typical values are for $T_A = 25^{\circ}$ C, $V_{CCINT} = 2.5$ V, and $V_{CCIO} = 2.5$ or 3.3 V.
- These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on (8)page 62.
- (9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
- (10) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
- (11) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (12) This value is specified for normal device operation. The value may vary during power-up.
- (13) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO} .
- (14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 2	Table 27. APEX 20KE Device Absolute Maximum Ratings Note (1)								
Symbol	Parameter	Conditions	Min	Max	Unit				
V _{CCINT}	Supply voltage	With respect to ground (2)	-0.5	2.5	V				
V _{CCIO}			-0.5	4.6	V				
VI	DC input voltage		-0.5	4.6	V				
I _{OUT}	DC output current, per pin		-25	25	mA				
T _{STG}	Storage temperature	No bias	-65	150	°C				
T _{AMB}	Ambient temperature	Under bias	-65	135	°C				
Τ _J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C				
		Ceramic PGA packages, under bias		150	°C				

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For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

Table 30.	Table 30. APEX 20KE Device Capacitance Note (15)							
Symbol	Parameter	Conditions	Min	Max	Unit			
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		8	pF			
CINCLK	Input capacitance on dedicated clock pin	V _{IN} = 0 V, f = 1.0 MHz		12	pF			
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		8	pF			

Notes to Tables 27 through 30:

- (1) See the Operating Requirements for Altera Devices Data Sheet.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
- (5) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

Vin	Max. Duty Cycle
4.0V	100% (DC)
4.1	90%

- 4.2 50%
- 4.3 30%
- 4.4 17%
- 4.5 10%
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (7) Typical values are for $T_A = 25^\circ$ C, $V_{CCINT} = 1.8$ V, and $V_{CCIO} = 1.8$ V, 2.5 V or 3.3 V.
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to Application Note 117 (Using Selectable I/O Standards in Altera Devices) for the V_{IH}, V_{IL}, V_{OH}, V_{OL}, and I_I parameters when VCCIO = 1.8 V.
- (10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $\rm V_{CCIO}$ and $\rm V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.



Figure 35 shows the output drive characteristics of APEX 20KE devices.

Note to Figure 35:(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Table 94. EP20K600E Minimum Pulse Width Timing Parameters									
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed	-3 Speed Grade			
	Min	Max	Min	Max	Min	Max			
t _{CH}	2.00		2.50		2.75		ns		
t _{CL}	2.00		2.50		2.75		ns		
t _{CLRP}	0.18		0.26		0.34		ns		
t _{PREP}	0.18		0.26		0.34		ns		
t _{ESBCH}	2.00		2.50		2.75		ns		
t _{ESBCL}	2.00		2.50		2.75		ns		
t _{ESBWP}	1.17		1.68		2.18		ns		
t _{ESBRP}	0.95		1.35		1.76		ns		

Table 95. EP20K600E External Timing Parameters									
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit		
	Min	Max	Min	Max	Min	Max			
t _{INSU}	2.74		2.74		2.87		ns		
t _{INH}	0.00		0.00		0.00		ns		
tоитсо	2.00	5.51	2.00	6.06	2.00	6.61	ns		
tINSUPLL	1.86		1.96		-		ns		
t _{INHPLL}	0.00		0.00		-		ns		
toutcopll	0.50	2.62	0.50	2.91	-	-	ns		

Table 96. EP20K600E External Bidirectional Timing Parameters									
Symbol	-1 Spee	d Grade	-2 Speed Grade		-3 Speed Grade		Unit		
	Min	Max	Min	Мах	Min	Max			
t _{insubidir}	0.64		0.98		1.08		ns		
t _{inhbidir}	0.00		0.00		0.00		ns		
t _{outcobidir}	2.00	5.51	2.00	6.06	2.00	6.61	ns		
t _{XZBIDIR}		6.10		6.74		7.10	ns		
t _{ZXBIDIR}		6.10		6.74		7.10	ns		
t _{insubidirpll}	2.26		2.68		-		ns		
t _{inhbidirpll}	0.00		0.00		-		ns		
toutcobidirpll	0.50	2.62	0.50	2.91	-	-	ns		
t _{XZBIDIRPLL}		3.21		3.59		-	ns		
t _{ZXBIDIRPLL}		3.21		3.59		-	ns		

Table 104. EP20K1500E f _{MAX} ESB Timing Microparameters										
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit			
	Min	Max	Min	Max	Min	Max	1			
t _{ESBARC}		1.78		2.02		1.95	ns			
t _{ESBSRC}		2.52		2.91		3.14	ns			
t _{ESBAWC}		3.52		4.11		4.40	ns			
t _{ESBSWC}		3.23		3.84		4.16	ns			
t _{ESBWASU}	0.62		0.67		0.61		ns			
t _{ESBWAH}	0.41		0.55		0.55		ns			
t _{ESBWDSU}	0.77		0.79		0.81		ns			
t _{ESBWDH}	0.41		0.55		0.55		ns			
t _{ESBRASU}	1.74		1.92		1.85		ns			
t _{ESBRAH}	0.00		0.01		0.23		ns			
t _{ESBWESU}	2.07		2.28		2.41		ns			
t _{ESBWEH}	0.00		0.00		0.00		ns			
t _{ESBDATASU}	0.25		0.27		0.29		ns			
t _{ESBDATAH}	0.13		0.13		0.13		ns			
t _{ESBWADDRSU}	0.11		0.04		0.11		ns			
t _{ESBRADDRSU}	0.14		0.11		0.16		ns			
t _{ESBDATACO1}		1.29		1.50		1.63	ns			
t _{ESBDATACO2}		2.55		2.99		3.22	ns			
t _{ESBDD}		3.12		3.57		3.85	ns			
t _{PD}		1.84		2.13		2.32	ns			
t _{PTERMSU}	1.08		1.19		1.32		ns			
t _{PTERMCO}		1.31		1.53		1.66	ns			

Table 105. EP20K1500E f _{MAX} Routing Delays												
Symbol	-1 Spe	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade						
	Min	Max	Min	Max	Min	Max						
t _{F1-4}		0.28		0.28		0.28	ns					
t _{F5-20}		1.36		1.50		1.62	ns					
t _{F20+}		4.43		4.48		5.07	ns					