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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	2560
Number of Logic Elements/Cells	2560
Total RAM Bits	32768
Number of I/O	196
Number of Gates	162000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k60efc324-1">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k60efc324-1</a>

**Table 2. Additional APEX 20K Device Features** *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

*Note to Tables 1 and 2:*

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see [Table 3](#))
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - ESB offering programmable power-saving mode

**Table 3. APEX 20K Supply Voltages**

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage ( $V_{CCINT}$ )	2.5 V	1.8 V
MultiVolt I/O interface voltage levels ( $V_{CCIO}$ )	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

*Note to Table 3:*

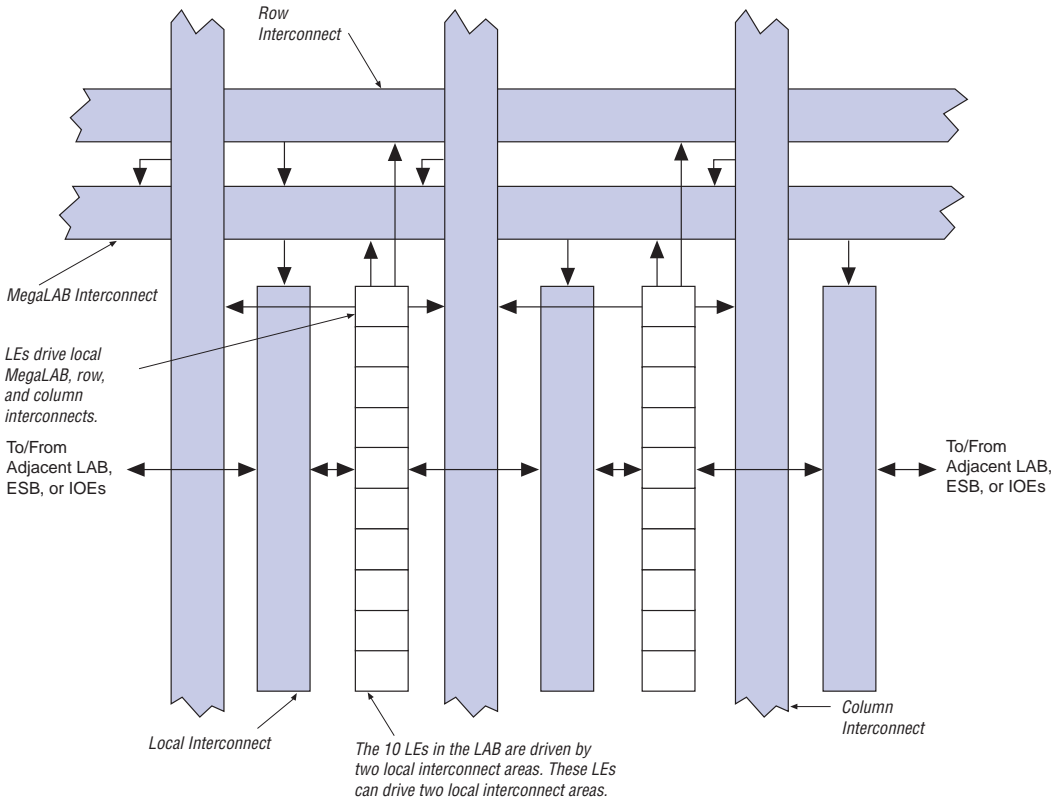
(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure



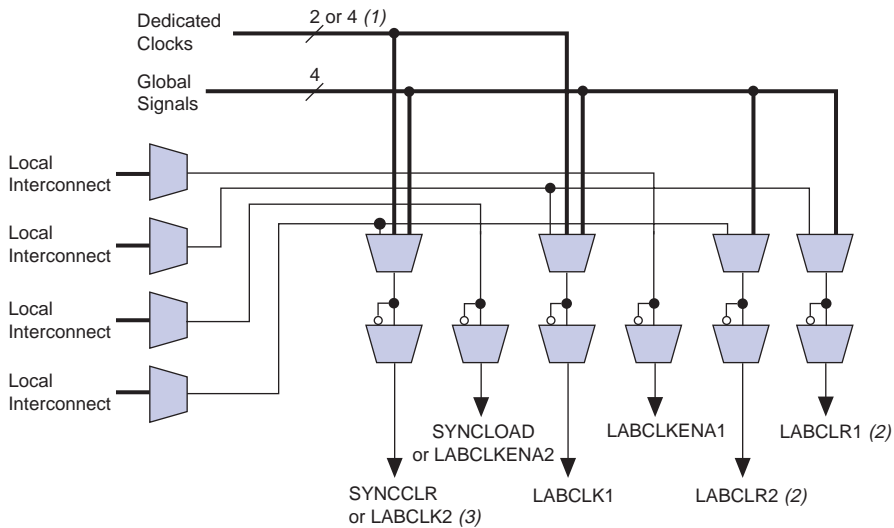
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. **Figure 4** shows the LAB control signal generation circuit.

**Figure 4. LAB Control Signal Generation**



**Notes to Figure 4:**

- (1) APEX 20KE devices have four dedicated clocks.
- (2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
- (3) The SYNCCLR signal can be generated by the local interconnect or global signals.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

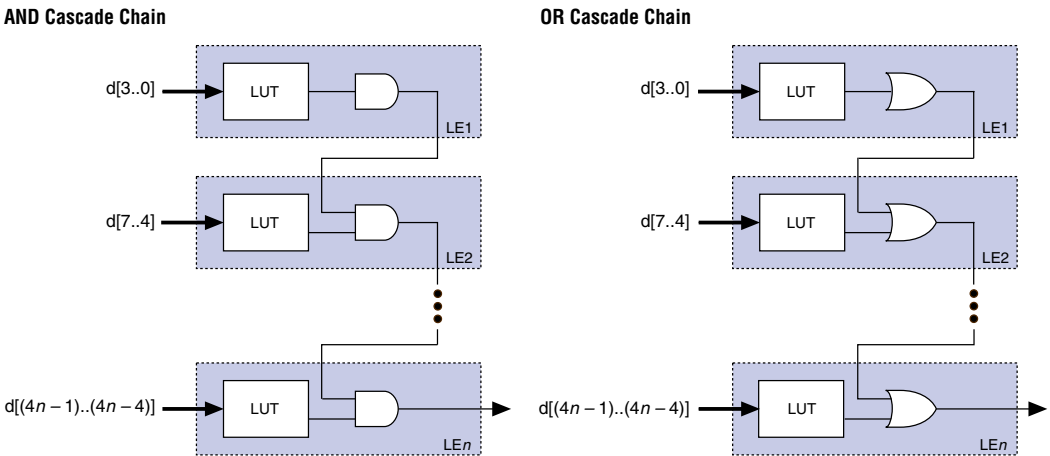
Figure 6 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

### Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain



### *LE Operating Modes*

The APEX 20K LE can operate in one of the following three modes:

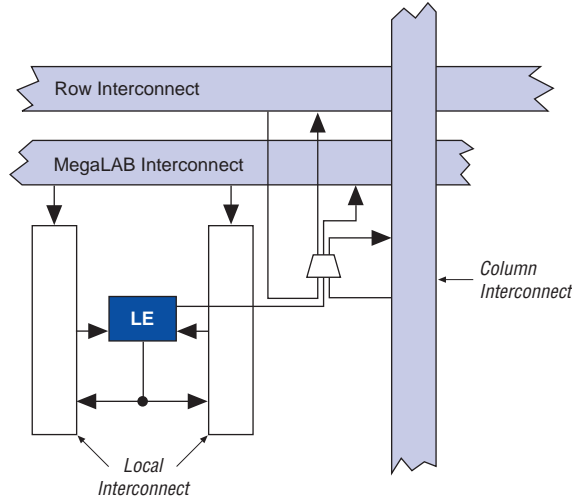
- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

**Figure 11. Driving the FastTrack Interconnect**



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABs in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.



ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable ( $WE$ ) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the  $WE$  signal. In contrast, the ESB's synchronous RAM generates its own  $WE$  signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

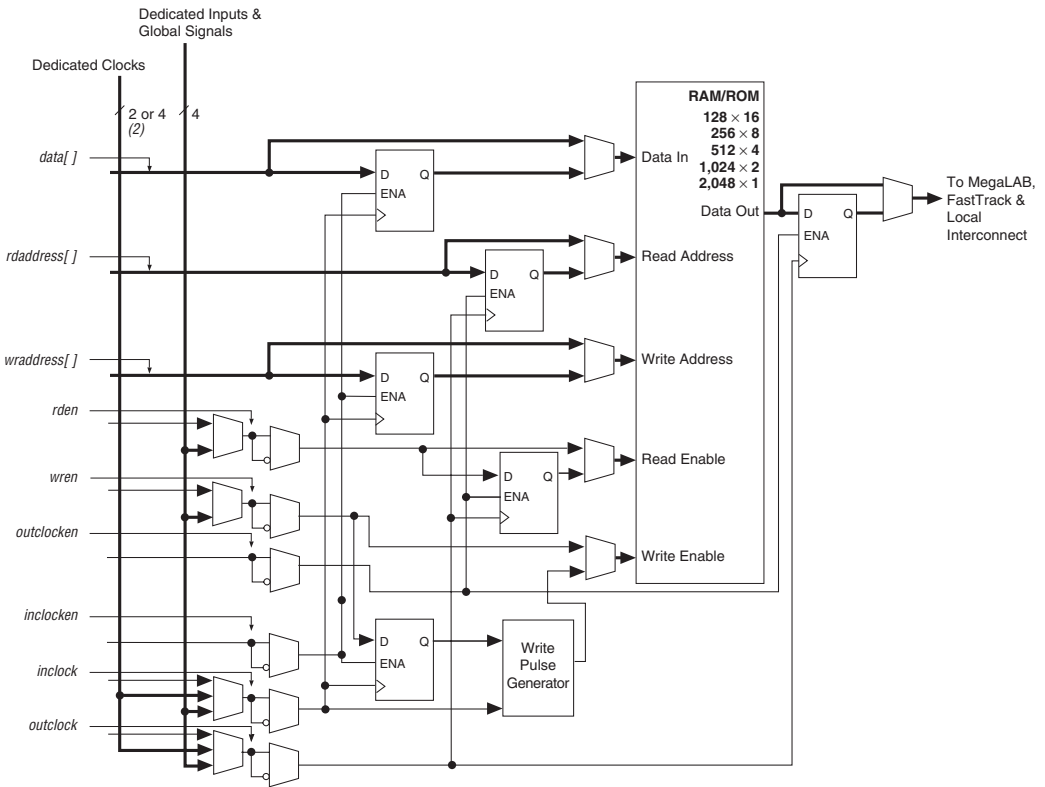
When implementing memory, each ESB can be configured in any of the following sizes:  $128 \times 16$ ,  $256 \times 8$ ,  $512 \times 4$ ,  $1,024 \times 2$ , or  $2,048 \times 1$ . By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two  $128 \times 16$  RAM blocks can be combined to form a  $128 \times 32$  RAM block, and two  $512 \times 4$  RAM blocks can be combined to form a  $512 \times 8$  RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).

## Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

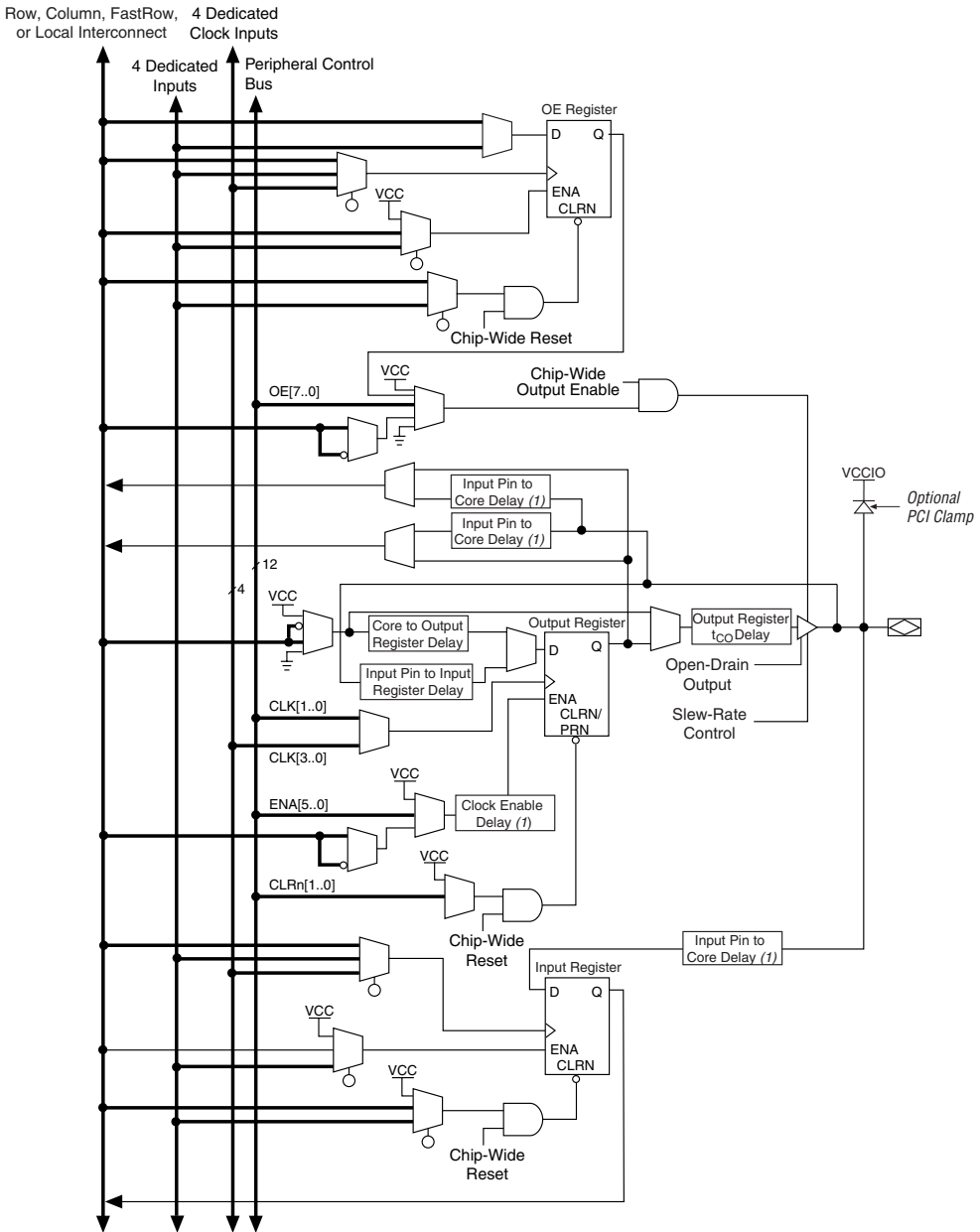
Figure 20. ESB in Read/Write Clock Mode Note (1)



**Notes to Figure 20:**

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

Figure 26. APEX 20KE Bidirectional I/O Registers Notes (1), (2)

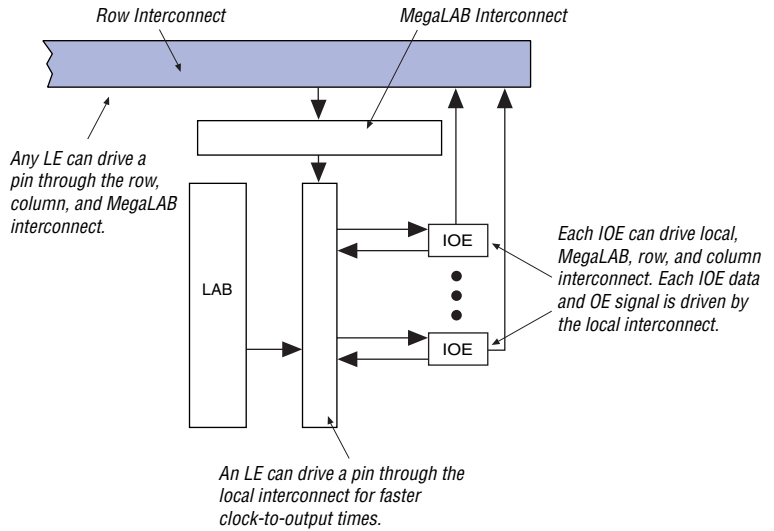


Notes to Figure 26:

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. **Figure 27** shows how a row IOE connects to the interconnect.

**Figure 27. Row IOE Connection to the Interconnect**



**Table 29. APEX 20KE Device DC Operating Conditions** *Notes (7), (8), (9)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>IH</sub>	High-level LVTTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V <sub>CCIO</sub> (10)		4.1	V	
V <sub>IL</sub>	Low-level LVTTTL, CMOS, or 3.3-V PCI input voltage		-0.5		0.8, 0.3 × V <sub>CCIO</sub> (10)	V	
V <sub>OH</sub>	3.3-V high-level LVTTTL output voltage	I <sub>OH</sub> = -12 mA DC, V <sub>CCIO</sub> = 3.00 V (11)	2.4			V	
	3.3-V high-level LVCMOS output voltage	I <sub>OH</sub> = -0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (11)	V <sub>CCIO</sub> - 0.2			V	
	3.3-V high-level PCI output voltage	I <sub>OH</sub> = -0.5 mA DC, V <sub>CCIO</sub> = 3.00 to 3.60 V (11)	0.9 × V <sub>CCIO</sub>			V	
	2.5-V high-level output voltage	I <sub>OH</sub> = -0.1 mA DC, V <sub>CCIO</sub> = 2.30 V (11)	2.1			V	
		I <sub>OH</sub> = -1 mA DC, V <sub>CCIO</sub> = 2.30 V (11)	2.0			V	
		I <sub>OH</sub> = -2 mA DC, V <sub>CCIO</sub> = 2.30 V (11)	1.7			V	
V <sub>OL</sub>	3.3-V low-level LVTTTL output voltage	I <sub>OL</sub> = 12 mA DC, V <sub>CCIO</sub> = 3.00 V (12)			0.4	V	
	3.3-V low-level LVCMOS output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 3.00 V (12)			0.2	V	
	3.3-V low-level PCI output voltage	I <sub>OL</sub> = 1.5 mA DC, V <sub>CCIO</sub> = 3.00 to 3.60 V (12)			0.1 × V <sub>CCIO</sub>	V	
	2.5-V low-level output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 2.30 V (12)				0.2	V
		I <sub>OL</sub> = 1 mA DC, V <sub>CCIO</sub> = 2.30 V (12)				0.4	V
		I <sub>OL</sub> = 2 mA DC, V <sub>CCIO</sub> = 2.30 V (12)				0.7	V
I <sub>I</sub>	Input pin leakage current	V <sub>I</sub> = 4.1 to -0.5 V (13)	-10		10	μA	
I <sub>OZ</sub>	Tri-stated I/O pin leakage current	V <sub>O</sub> = 4.1 to -0.5 V (13)	-10		10	μA	
I <sub>CC0</sub>	V <sub>CC</sub> supply current (standby) (All ESBs in power-down mode)	V <sub>I</sub> = ground, no load, no toggling inputs, -1 speed grade		10		mA	
		V <sub>I</sub> = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA	
R <sub>CONF</sub>	Value of I/O pin pull-up resistor before and during configuration	V <sub>CCIO</sub> = 3.0 V (14)	20		50	kΩ	
		V <sub>CCIO</sub> = 2.375 V (14)	30		80	kΩ	
		V <sub>CCIO</sub> = 1.71 V (14)	60		150	kΩ	

**Table 36. APEX 20KE Routing Timing Microparameters** *Note (1)*

Symbol	Parameter
$t_{F1-4}$	Fanout delay using Local Interconnect
$t_{F5-20}$	Fanout delay estimate using MegaLab Interconnect
$t_{F20+}$	Fanout delay estimate using FastTrack Interconnect

*Note to Table 36:*

- (1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

**Table 37. APEX 20KE Functional Timing Microparameters**

Symbol	Parameter
TCH	Minimum clock high time from clock pin
TCL	Minimum clock low time from clock pin
TCLRP	LE clear Pulse Width
TPREP	LE preset pulse width
TESBCH	Clock high time for ESB
TESBCL	Clock low time for ESB
TESBWP	Write pulse width
TESBRP	Read pulse width

Tables 38 and 39 describe the APEX 20KE external timing parameters.

**Table 38. APEX 20KE External Timing Parameters** *Note (1)*

Symbol	Clock Parameter	Conditions
$t_{INSU}$	Setup time with global clock at IOE input register	
$t_{INH}$	Hold time with global clock at IOE input register	
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
$t_{INHPLL}$	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF

**Table 42. EP20K400  $f_{MAX}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.1		0.3		0.6		ns
$t_H$	0.5		0.8		0.9		ns
$t_{CO}$		0.1		0.4		0.6	ns
$t_{LUT}$		1.0		1.2		1.4	ns
$t_{ESBRC}$		1.7		2.1		2.4	ns
$t_{ESBWC}$		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
$t_{ESBDD}$		2.5		3.3		3.6	ns
$t_{PD}$		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
$t_{F1-4}$		0.4		0.5		0.6	ns
$t_{F5-20}$		2.6		2.8		2.9	ns
$t_{F20+}$		3.7		3.8		3.9	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns
$t_{CLRP}$	0.5		0.6		0.8		ns
$t_{PREP}$	0.5		0.5		0.5		ns
$t_{ESBCH}$	2.0		2.5		3.0		ns
$t_{ESBCL}$	2.0		2.5		3.0		ns
$t_{ESBWP}$	1.5		1.9		2.2		ns
$t_{ESBRP}$	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 46. EP20K200 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.9		2.3		2.6		ns
$t_{\text{INHDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{\text{XZBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{ZXBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{INSUBIDIR}} (2)$	1.1		1.2		–		ns
$t_{\text{INHDIR}} (2)$	0.0		0.0		–		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	2.7	0.5	3.1	–	–	ns
$t_{\text{XZBIDIR}} (2)$		4.3		5.0		–	ns
$t_{\text{ZXBIDIR}} (2)$		4.3		5.0		–	ns

**Table 47. EP20K400 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INH}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{INSU}} (2)$	0.4		1.0		–		ns
$t_{\text{INH}} (2)$	0.0		0.0		–		ns
$t_{\text{OUTCO}} (2)$	0.5	3.1	0.5	4.1	–	–	ns

**Table 48. EP20K400 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INHDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{XZBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{ZXBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{INSUBIDIR}} (2)$	0.5		1.0		–		ns
$t_{\text{INHDIR}} (2)$	0.0		0.0		–		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	3.1	0.5	4.1	–	–	ns
$t_{\text{XZBIDIR}} (2)$		6.2		7.6		–	ns
$t_{\text{ZXBIDIR}} (2)$		6.2		7.6		–	ns



Tables 55 through 60 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

**Table 55. EP20K60E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.17		0.15		0.16		ns
$t_H$	0.32		0.33		0.39		ns
$t_{CO}$		0.29		0.40		0.60	ns
$t_{LUT}$		0.77		1.07		1.59	ns

**Table 74. EP20K200E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.68		2.06		2.24	ns
$t_{ESBSRC}$		2.27		2.77		3.18	ns
$t_{ESBAWC}$		3.10		3.86		4.50	ns
$t_{ESBSWC}$		2.90		3.67		4.21	ns
$t_{ESBWASU}$	0.55		0.67		0.74		ns
$t_{ESBWAH}$	0.36		0.46		0.48		ns
$t_{ESBWDSU}$	0.69		0.83		0.95		ns
$t_{ESBWDH}$	0.36		0.46		0.48		ns
$t_{ESBRASU}$	1.61		1.90		2.09		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.42		1.71		2.01		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.06		-0.07		0.05		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.13		0.31		ns
$t_{ESBRADDRSU}$	0.18		0.23		0.39		ns
$t_{ESBDATACO1}$		1.09		1.35		1.51	ns
$t_{ESBDATACO2}$		2.19		2.75		3.22	ns
$t_{ESBDD}$		2.75		3.41		4.03	ns
$t_{PD}$		1.58		1.97		2.33	ns
$t_{PTERMSU}$	1.00		1.22		1.51		ns
$t_{PTERMCO}$		1.10		1.37		1.09	ns

**Table 75. EP20K200E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.27		0.29	ns
$t_{F5-20}$		1.02		1.20		1.41	ns
$t_{F20+}$		1.99		2.23		2.53	ns

**Table 78. EP20K200E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.81		3.19		3.54		ns
$t_{\text{INHBDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{\text{XZBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{ZXBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{INSUBIDIRPLL}}$	3.30		3.64		-		ns
$t_{\text{INHBDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.40		6.05		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.40		6.05		-	ns

Tables 79 through 84 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

**Table 79. EP20K300E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.16		0.17		0.18		ns
$t_{\text{H}}$	0.31		0.33		0.38		ns
$t_{\text{CO}}$		0.28		0.38		0.51	ns
$t_{\text{LUT}}$		0.79		1.07		1.43	ns

**Table 102. EP20K1000E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.22		3.33		3.51		ns
$t_{\text{INHIBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{\text{XZBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{ZXBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.25		3.26				ns
$t_{\text{INHIBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.25	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		2.81		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		2.81		3.80			ns

Tables 103 through 108 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

**Table 103. EP20K1500E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.32		0.33	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

### **Configuration Schemes**

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see [Table 111](#)), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

<b>Table 111. Data Sources for Configuration</b>	
<b>Configuration Scheme</b>	<b>Data Source</b>
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File



For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

### **Device Pin-Outs**

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information