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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	2560
Number of Logic Elements/Cells	2560
Total RAM Bits	32768
Number of I/O	196
Number of Gates	162000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k60efc324-2">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=ep20k60efc324-2</a>

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP<sup>SM</sup>) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS)

**Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count** *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

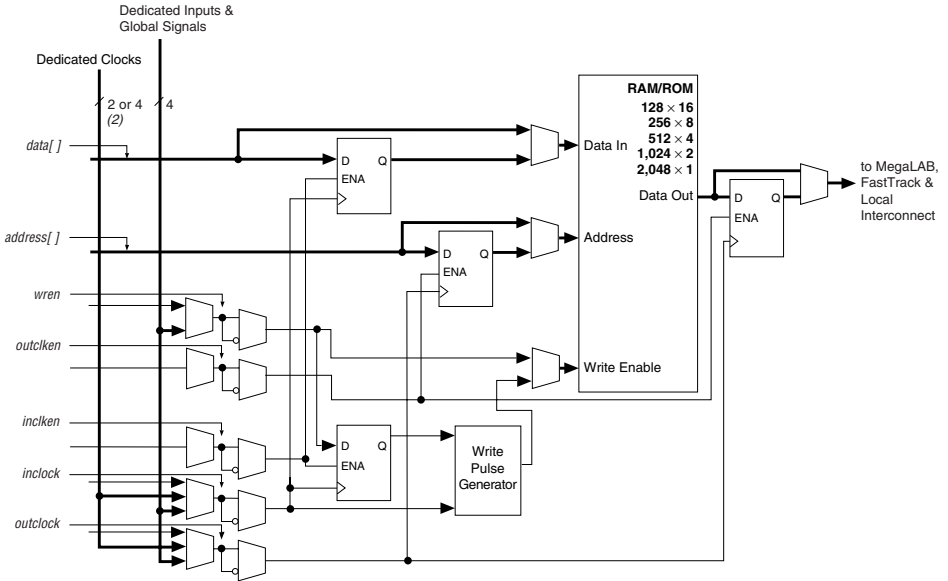
APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

Figure 22. ESB in Single-Port Mode *Note (1)*



Notes to Figure 22:

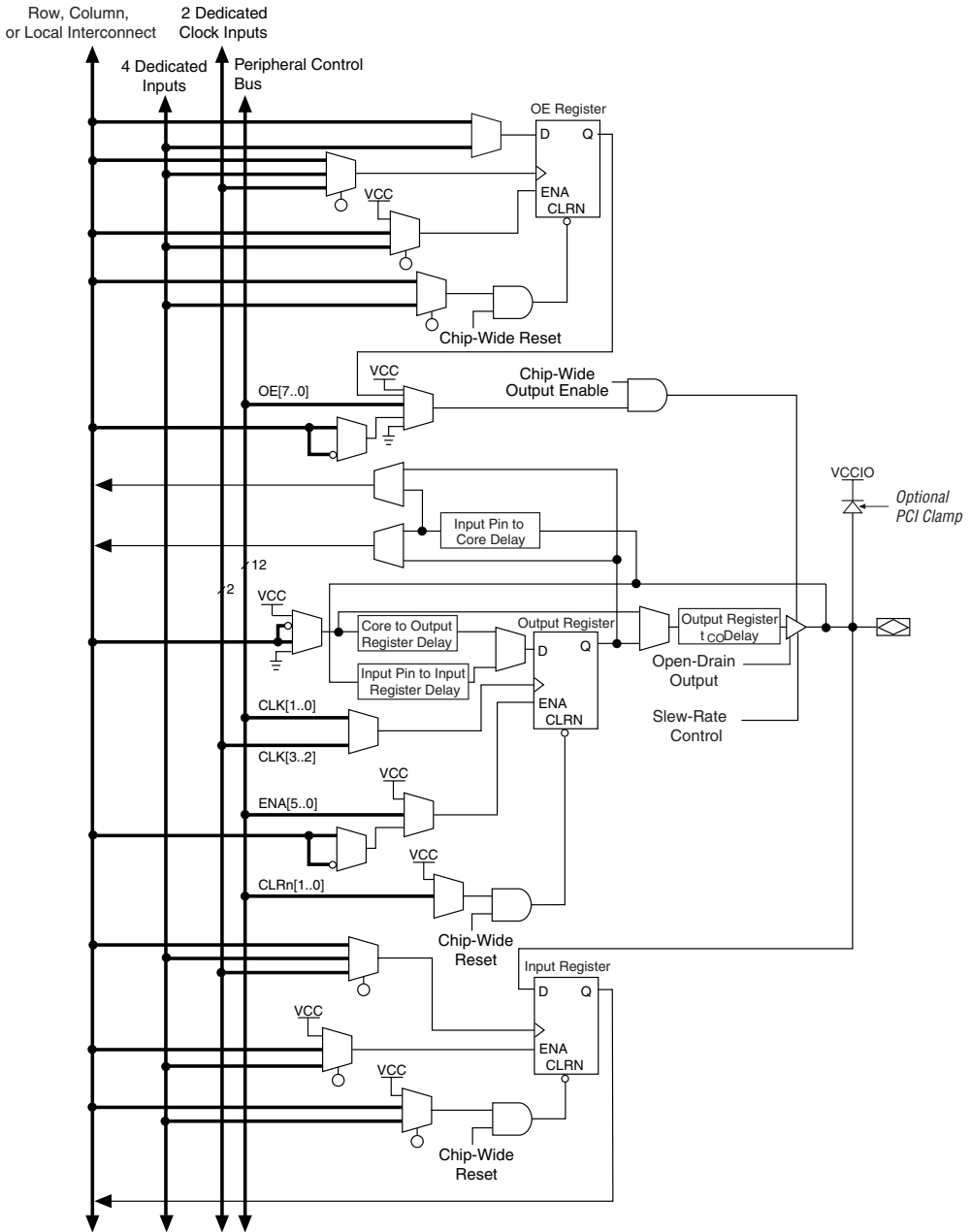
- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

### Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Figure 25. APEX 20K Bidirectional I/O Registers Note (1)



Note to Figure 25:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

<i><b>Table 11. APEX 20KE Programmable Delay Chains</b></i>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register $t_{CO}$ Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

**Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2) Note (1)**

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f <sub>VCO</sub> (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
f <sub>CLOCK0</sub>	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f <sub>CLOCK1</sub>	clock1 PLL output frequency for internal use		20	335	20	200	MHz
f <sub>CLOCK0_EXT</sub>	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
f <sub>CLOCK1_EXT</sub>	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

Symbol	Parameter	Min	Max	Unit
t <sub>JCP</sub>	TCK clock period	100		ns
t <sub>JCH</sub>	TCK clock high time	50		ns
t <sub>JCL</sub>	TCK clock low time	50		ns
t <sub>JPSU</sub>	JTAG port setup time	20		ns
t <sub>JPH</sub>	JTAG port hold time	45		ns
t <sub>JPCO</sub>	JTAG port clock to output		25	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output		25	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance		25	ns
t <sub>JSSU</sub>	Capture register setup time	20		ns
t <sub>JSH</sub>	Capture register hold time	45		ns
t <sub>JSCO</sub>	Update register clock to output		35	ns
t <sub>JSZX</sub>	Update register high impedance to valid output		35	ns
t <sub>JSXZ</sub>	Update register valid output to high impedance		35	ns



For more information, see the following documents:

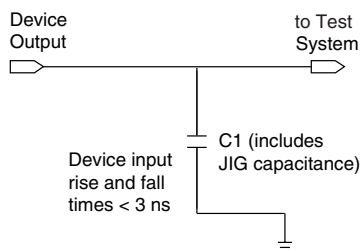
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.



**Figure 32. APEX 20K AC Test Conditions** *Note (1)*



**Note to Figure 32:**

- (1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

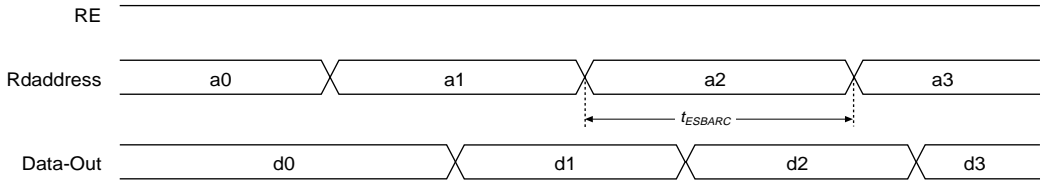
**Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings** *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage	With respect to ground (3)	-0.5	3.6	V
$V_{CCIO}$			-0.5	4.6	V
$V_I$			DC input voltage	-2.0	5.75
$I_{OUT}$	DC output current, per pin		-25	25	mA
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	-65	135	°C
$T_J$	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

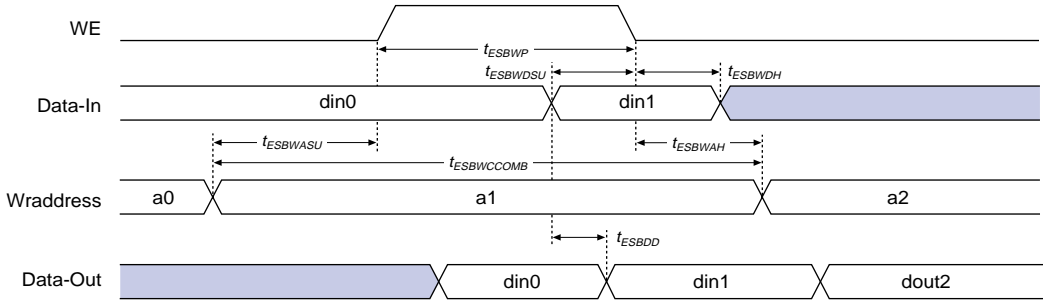
Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms

**ESB Asynchronous Read**



**ESB Asynchronous Write**



**Table 31. APEX 20K  $t_{MAX}$  Timing Parameters (Part 2 of 2)**

Symbol	Parameter
$t_{ESB\text{DATA}CO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
$t_{F1-4}$	Fanout delay using local interconnect
$t_{F5-20}$	Fanout delay using MegaLab Interconnect
$t_{F20+}$	Fanout delay using FastTrack Interconnect
$t_{CH}$	Minimum clock high time from clock pin
$t_{CL}$	Minimum clock low time from clock pin
$t_{CLRP}$	LE clear pulse width
$t_{PREP}$	LE preset pulse width
$t_{ESBCH}$	Clock high time
$t_{ESBCL}$	Clock low time
$t_{ESBWP}$	Write pulse width
$t_{ESBRP}$	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

**Table 32. APEX 20K External Timing Parameters Note (1)**

Symbol	Clock Parameter
$t_{INSU}$	Setup time with global clock at IOE register
$t_{INH}$	Hold time with global clock at IOE register
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE register

**Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)**

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INH\text{BIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCO\text{BIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZ\text{BIDIR}}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{ZX\text{BIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF

**Table 39. APEX 20KE External Bidirectional Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{\text{INHIDIR}}$	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
$t_{\text{XZBIDIR}}$	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
$t_{\text{ZXBIDIR}}$	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{\text{INSUBIDIRPLL}}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{\text{INHIDIRPLL}}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{\text{OUTCOBIDIRPLL}}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{\text{XZBIDIRPLL}}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{\text{ZXBIDIRPLL}}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

**Note to Tables 38 and 39:**

(1) These timing parameters are sample-tested only.

**Table 62. EP20K100E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.61		1.84		1.97	ns
$t_{ESBSRC}$		2.57		2.97		3.20	ns
$t_{ESBAWC}$		0.52		4.09		4.39	ns
$t_{ESBSWC}$		3.17		3.78		4.09	ns
$t_{ESBWASU}$	0.56		6.41		0.63		ns
$t_{ESBWAH}$	0.48		0.54		0.55		ns
$t_{ESBWDSU}$	0.71		0.80		0.81		ns
$t_{ESBWDH}$	.048		0.54		0.55		ns
$t_{ESBRASU}$	1.57		1.75		1.87		ns
$t_{ESBRAH}$	0.00		0.00		0.20		ns
$t_{ESBWESU}$	1.54		1.72		1.80		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.16		-0.20		-0.20		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.12		0.08		0.13		ns
$t_{ESBRADDRSU}$	0.17		0.15		0.19		ns
$t_{ESBDATACO1}$		1.20		1.39		1.52	ns
$t_{ESBDATACO2}$		2.54		2.99		3.22	ns
$t_{ESBDD}$		3.06		3.56		3.85	ns
$t_{PD}$		1.73		2.02		2.20	ns
$t_{PTERMSU}$	1.11		1.26		1.38		ns
$t_{PTERMCO}$		1.19		1.40		1.08	ns

**Table 63. EP20K100E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.27		0.29	ns
$t_{F5-20}$		1.04		1.26		1.52	ns
$t_{F20+}$		1.12		1.36		1.86	ns

**Table 64. EP20K100E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	2.00		2.00		2.00		ns
t <sub>CL</sub>	2.00		2.00		2.00		ns
t <sub>CLRP</sub>	0.20		0.20		0.20		ns
t <sub>PREP</sub>	0.20		0.20		0.20		ns
t <sub>ESBCH</sub>	2.00		2.00		2.00		ns
t <sub>ESBCL</sub>	2.00		2.00		2.00		ns
t <sub>ESBWP</sub>	1.29		1.53		1.66		ns
t <sub>ESBRP</sub>	1.11		1.29		1.41		ns

**Table 65. EP20K100E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.23		2.32		2.43		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.86	2.00	5.35	2.00	5.84	ns
t <sub>INSUPLL</sub>	1.58		1.66		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.96	0.50	3.29	-	-	ns

**Table 66. EP20K100E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	2.74		2.96		3.19		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.86	2.00	5.35	2.00	5.84	ns
t <sub>XZBIDIR</sub>		5.00		5.48		5.89	ns
t <sub>ZXBIDIR</sub>		5.00		5.48		5.89	ns
t <sub>INSUBIDIRPLL</sub>	4.64		5.03		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.96	0.50	3.29	-	-	ns
t <sub>XZBIDIRPLL</sub>		3.10		3.42		-	ns
t <sub>ZXBIDIRPLL</sub>		3.10		3.42		-	ns

**Table 68. EP20K160E  $f_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.65		2.02		2.11	ns
$t_{ESBSRC}$		2.21		2.70		3.11	ns
$t_{ESBAWC}$		3.04		3.79		4.42	ns
$t_{ESBSWC}$		2.81		3.56		4.10	ns
$t_{ESBWASU}$	0.54		0.66		0.73		ns
$t_{ESBWAH}$	0.36		0.45		0.47		ns
$t_{ESBWDSU}$	0.68		0.81		0.94		ns
$t_{ESBWDH}$	0.36		0.45		0.47		ns
$t_{ESBRASU}$	1.58		1.87		2.06		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.41		1.71		2.00		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.02		-0.03		0.09		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.14		0.17		0.35		ns
$t_{ESBRADDRSU}$	0.21		0.27		0.43		ns
$t_{ESBDATACO1}$		1.04		1.30		1.46	ns
$t_{ESBDATACO2}$		2.15		2.70		3.16	ns
$t_{ESBDD}$		2.69		3.35		3.97	ns
$t_{PD}$		1.55		1.93		2.29	ns
$t_{PTERMSU}$	1.01		1.23		1.52		ns
$t_{PTERMCO}$		1.06		1.32		1.04	ns

**Table 76. EP20K200E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.36		2.44		2.65		ns
t <sub>CL</sub>	1.36		2.44		2.65		ns
t <sub>CLRP</sub>	0.18		0.19		0.21		ns
t <sub>PREP</sub>	0.18		0.19		0.21		ns
t <sub>ESBCH</sub>	1.36		2.44		2.65		ns
t <sub>ESBCL</sub>	1.36		2.44		2.65		ns
t <sub>ESBWP</sub>	1.18		1.48		1.76		ns
t <sub>ESBRP</sub>	0.95		1.17		1.41		ns

**Table 77. EP20K200E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.24		2.35		2.47		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	5.12	2.00	5.62	2.00	6.11	ns
t <sub>INSUPLL</sub>	2.13		2.07		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	3.01	0.50	3.36	-	-	ns



**Table 78. EP20K200E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.81		3.19		3.54		ns
$t_{\text{INHBDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{\text{XZBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{ZXBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{INSUBIDIRPLL}}$	3.30		3.64		-		ns
$t_{\text{INHBDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.40		6.05		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.40		6.05		-	ns

Tables 79 through 84 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

**Table 79. EP20K300E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.16		0.17		0.18		ns
$t_{\text{H}}$	0.31		0.33		0.38		ns
$t_{\text{CO}}$		0.28		0.38		0.51	ns
$t_{\text{LUT}}$		0.79		1.07		1.43	ns

**Table 82. EP20K300E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.25		1.43		1.67		ns
t <sub>CL</sub>	1.25		1.43		1.67		ns
t <sub>CLRP</sub>	0.19		0.26		0.35		ns
t <sub>PREP</sub>	0.19		0.26		0.35		ns
t <sub>ESBCH</sub>	1.25		1.43		1.67		ns
t <sub>ESBCL</sub>	1.25		1.43		1.67		ns
t <sub>ESBWP</sub>	1.25		1.71		2.28		ns
t <sub>ESBRP</sub>	1.01		1.38		1.84		ns

**Table 83. EP20K300E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.31		2.44		2.57		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	5.29	2.00	5.82	2.00	6.24	ns
t <sub>INSUPLL</sub>	1.76		1.85		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.65	0.50	2.95	-	-	ns

**Table 84. EP20K300E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	2.77		2.85		3.11		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	5.29	2.00	5.82	2.00	6.24	ns
t <sub>XZBIDIR</sub>		7.59		8.30		9.09	ns
t <sub>ZXBIDIR</sub>		7.59		8.30		9.09	ns
t <sub>INSUBIDIRPLL</sub>	2.50		2.76		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.65	0.50	2.95	-	-	ns
t <sub>XZBIDIRPLL</sub>		5.00		5.43		-	ns
t <sub>ZXBIDIRPLL</sub>		5.00		5.43		-	ns

**Table 87. EP20K400E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.25		0.26	ns
$t_{F5-20}$		1.01		1.12		1.25	ns
$t_{F20+}$		3.71		3.92		4.17	ns

**Table 88. EP20K400E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.36		2.22		2.35		ns
$t_{CL}$	1.36		2.26		2.35		ns
$t_{CLR P}$	0.18		0.18		0.19		ns
$t_{PREP}$	0.18		0.18		0.19		ns
$t_{ESBCH}$	1.36		2.26		2.35		ns
$t_{ESBCL}$	1.36		2.26		2.35		ns
$t_{ESBWP}$	1.17		1.38		1.56		ns
$t_{ESBRP}$	0.94		1.09		1.25		ns

**Table 89. EP20K400E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.51		2.64		2.77		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

## Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see [Table 111](#)), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

**Table 111. Data Sources for Configuration**

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File



For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*.

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$  added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).