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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	2560
Number of Logic Elements/Cells	2560
Total RAM Bits	32768
Number of I/O	148
Number of Gates	162000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k60eqc208-1x

Table 8. Comparison of APEX 20K & APEX 20KE Features

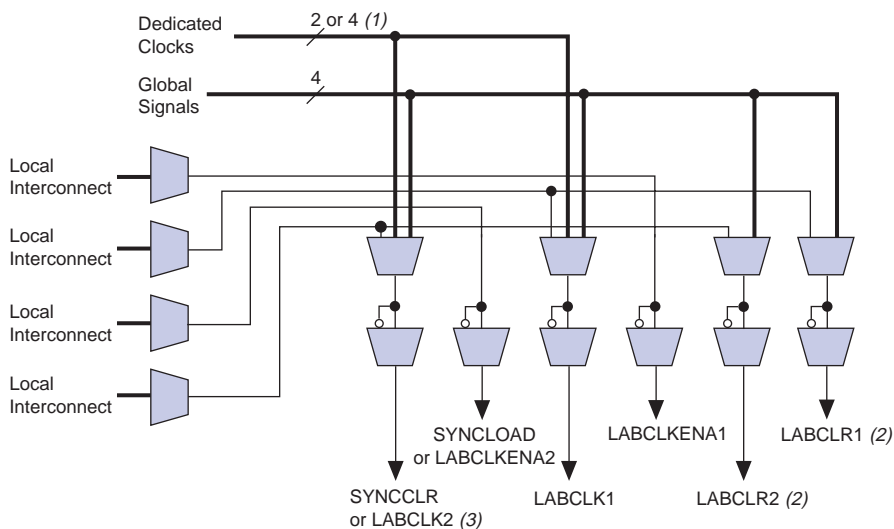| Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
SignalTap logic analysis	Full support	Full support
32/64-Bit, 33-MHz PCI	Full compliance in -1, -2 speed grades	Full compliance in -1, -2 speed grades
32/64-Bit, 66-MHz PCI	-	Full compliance in -1 speed grade
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device Certain devices are 5.0-V tolerant	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction 2× and 4× clock multiplication	Clock delay reduction $m/(n \times v)$ or $m/(n \times k)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVTTL True-LVDS and LVPECL data pins (in EP20K300E and larger devices) LVDS and LVPECL signaling (in all BGA and FineLine BGA devices) LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation

Notes to Figure 4:
(1) APEX 20KE devices have four dedicated clocks.
(2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
(3) The SYNCCLR signal can be generated by the local interconnect or global signals.

LE Operating Modes

The APEX 20K LE can operate in one of the following three modes:

■ Normal mode
■ Arithmetic mode
■ Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

*Figure 11. Driving the FastTrack Interconnect*
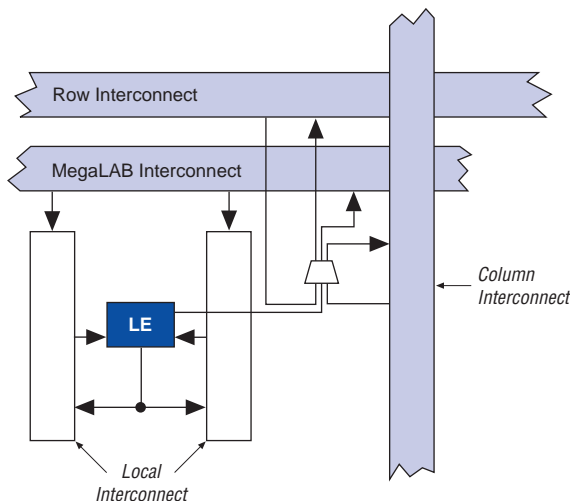
APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABS in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode   *Note (1)*
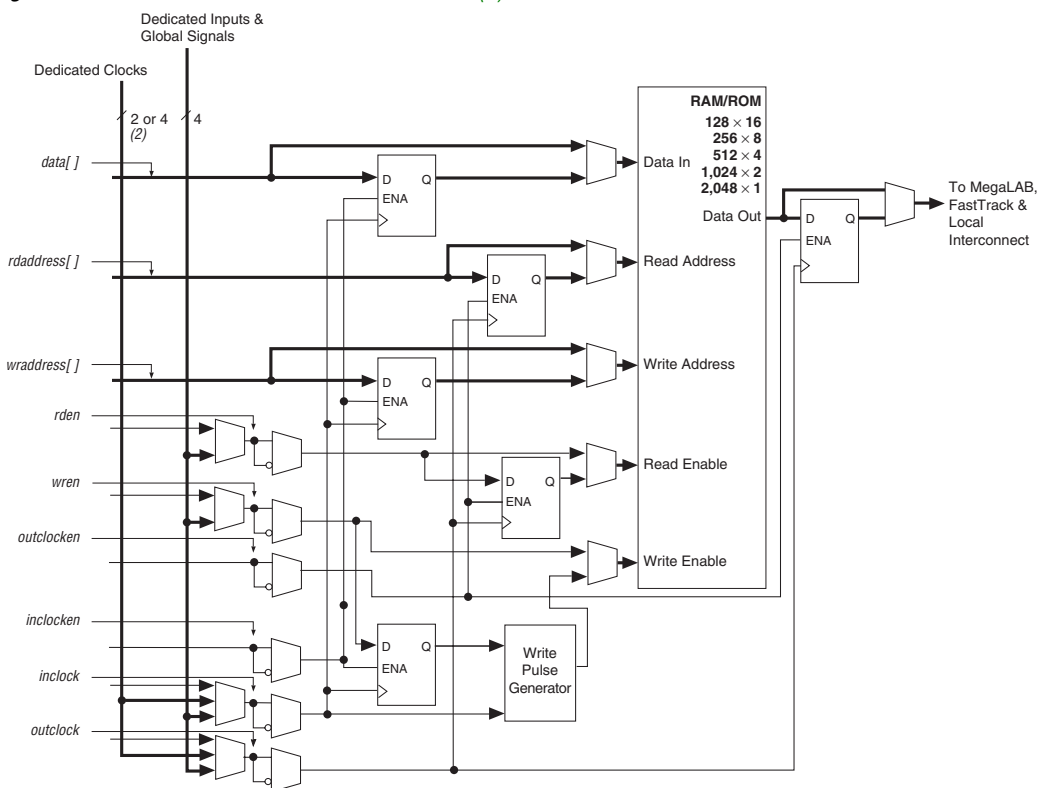
Notes to Figure 20:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

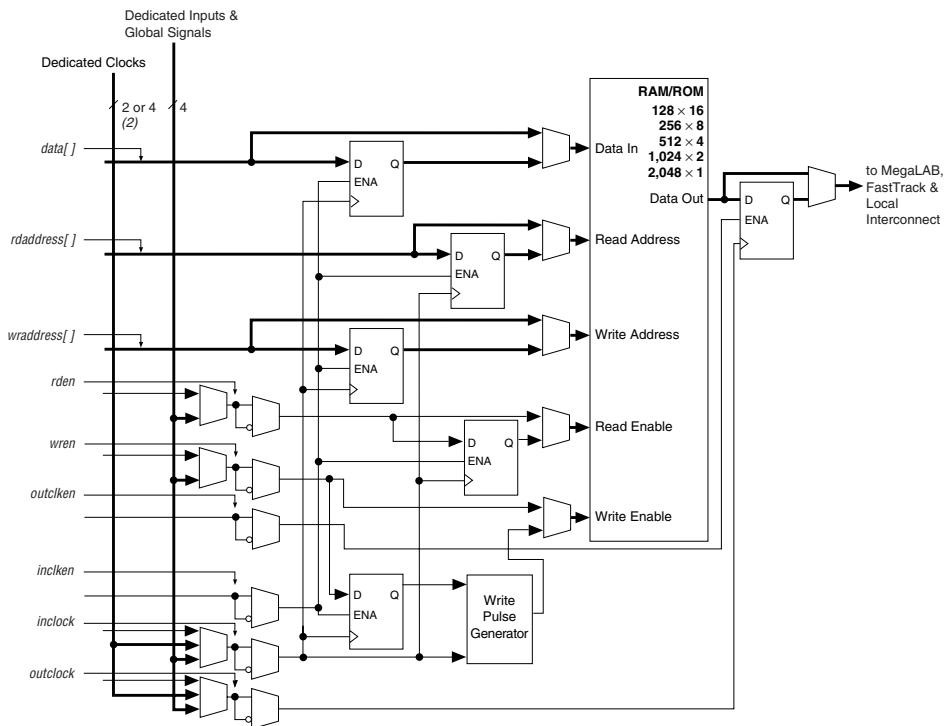*Figure 21. ESB in Input/Output Clock Mode*   *Note (1)*

Notes to Figure 21:
(1)   All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2)   APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation
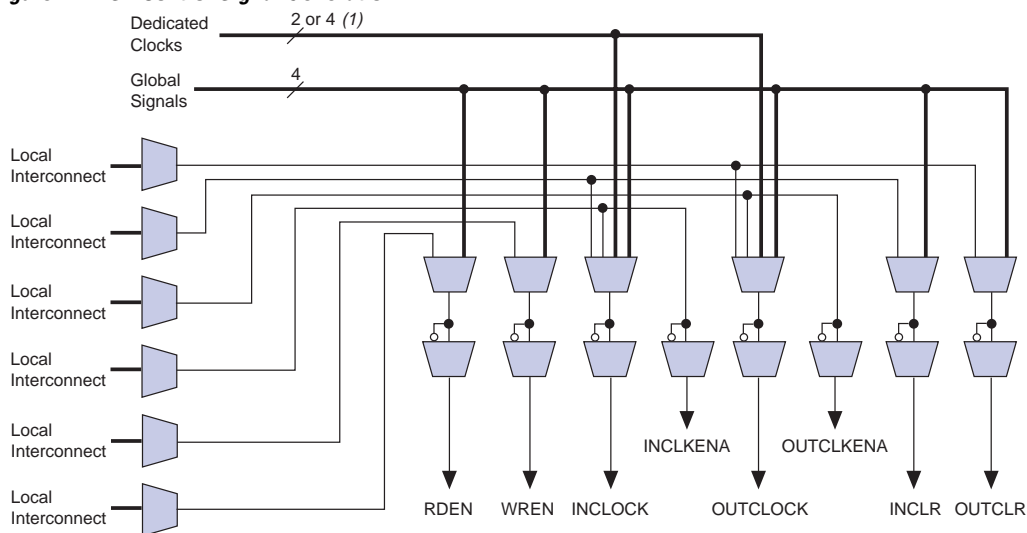
Note to Figure 24:
(1)   APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Table 18. APEX 20KE Clock Input & Output Parameters   (Part 2 of 2)   *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f_{IN}	Input clock frequency	3.3-V LVTTL	1.5	290	1.5	257	MHz
		2.5-V LVTTL	1.5	281	1.5	250	MHz
		1.8-V LVTTL	1.5	272	1.5	243	MHz
		GTL+	1.5	303	1.5	261	MHz
		SSTL-2 Class I	1.5	291	1.5	253	MHz
		SSTL-2 Class II	1.5	291	1.5	253	MHz
		SSTL-3 Class I	1.5	300	1.5	260	MHz
		SSTL-3 Class II	1.5	300	1.5	260	MHz
		LVDS	1.5	420	1.5	350	MHz

Notes to Tables 17 and 18:
(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the CLKLK_ENA pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ð f_{VCO} ð 840 MHz for LVDS mode.

SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length	
Device	**Boundary-Scan Register Length**
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 *(1)*

Note to Table 20:

(1)   This device does not support JTAG boundary scan testing.

Figure 32. APEX 20K AC Test Conditions   *Note (1)*
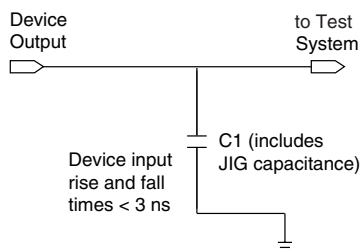
Note to Figure 32:
(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings   *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	−0.5	3.6	V
V_{CCIO}			−0.5	4.6	V
V_I	DC input voltage		−2.0	5.75	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices   *Note (1)*
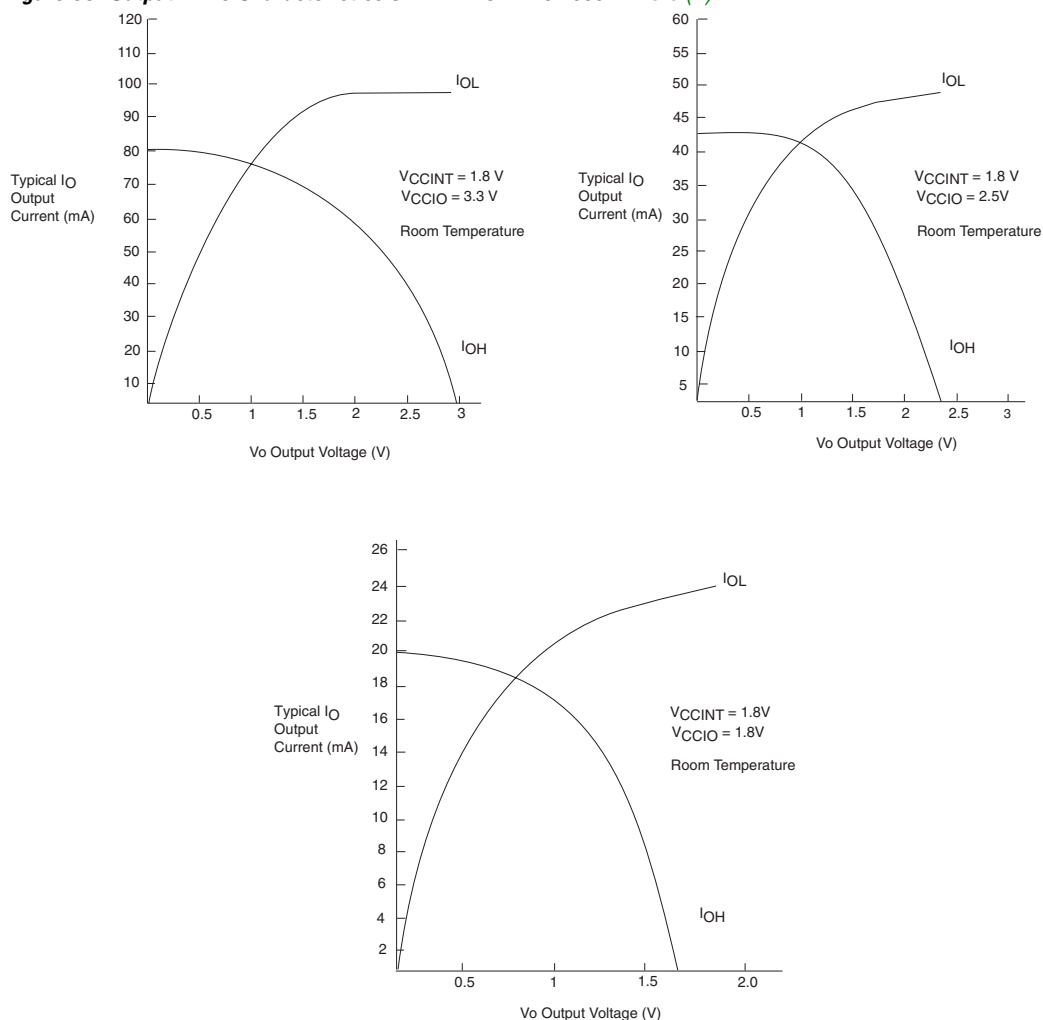
Note to Figure 35:
(1)   These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.6		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 42. EP20K400 f_MAX Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t$_{SU}$	0.1		0.3		0.6		ns
t$_H$	0.5		0.8		0.9		ns
t$_{CO}$		0.1		0.4		0.6	ns
t$_{LUT}$		1.0		1.2		1.4	ns
t$_{ESBRC}$		1.7		2.1		2.4	ns
t$_{ESBWC}$		5.7		6.9		8.1	ns
t$_{ESBWESU}$	3.3		3.9		4.6		ns
t$_{ESBDATASU}$	2.2		2.7		3.1		ns
t$_{ESBDATAH}$	0.6		0.8		0.9		ns
t$_{ESBADDRSU}$	2.4		2.9		3.3		ns
t$_{ESBDATACO1}$		1.3		1.6		1.8	ns
t$_{ESBDATACO2}$		2.5		3.1		3.6	ns
t$_{ESBDD}$		2.5		3.3		3.6	ns
t$_{PD}$		2.5		3.1		3.6	ns
t$_{PTERMSU}$	1.7		2.1		2.4		ns
t$_{PTERMCO}$		1.0		1.2		1.4	ns
t$_{F1-4}$		0.4		0.5		0.6	ns
t$_{F5-20}$		2.6		2.8		2.9	ns
t$_{F20+}$		3.7		3.8		3.9	ns
t$_{CH}$	2.0		2.5		3.0		ns
t$_{CL}$	2.0		2.5		3.0		ns
t$_{CLRP}$	0.5		0.6		0.8		ns
t$_{PREP}$	0.5		0.5		0.5		ns
t$_{ESBCH}$	2.0		2.5		3.0		ns
t$_{ESBCL}$	2.0		2.5		3.0		ns
t$_{ESBWP}$	1.5		1.9		2.2		ns
t$_{ESBRP}$	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 50. EP20K30E f$_{MAX}$ ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{ESBARC}$		2.03		2.86		4.24	ns
t$_{ESBSRC}$		2.58		3.49		5.02	ns
t$_{ESBAWC}$		3.88		5.45		8.08	ns
t$_{ESBSWC}$		4.08		5.35		7.48	ns
t$_{ESBWASU}$	1.77		2.49		3.68		ns
t$_{ESBWAH}$	0.00		0.00		0.00		ns
t$_{ESBWDSU}$	1.95		2.74		4.05		ns
t$_{ESBWDH}$	0.00		0.00		0.00		ns
t$_{ESBRASU}$	1.96		2.75		4.07		ns
t$_{ESBRAH}$	0.00		0.00		0.00		ns
t$_{ESBWESU}$	1.80		2.73		4.28		ns
t$_{ESBWEH}$	0.00		0.00		0.00		ns
t$_{ESBDATASU}$	0.07		0.48		1.17		ns
t$_{ESBDATAH}$	0.13		0.13		0.13		ns
t$_{ESBWADDRSU}$	0.30		0.80		1.64		ns
t$_{ESBRADDRSU}$	0.37		0.90		1.78		ns
t$_{ESBDATACO1}$		1.11		1.32		1.67	ns
t$_{ESBDATACO2}$		2.65		3.73		5.53	ns
t$_{ESBDD}$		3.88		5.45		8.08	ns
t$_{PD}$		1.91		2.69		3.98	ns
t$_{PTERMSU}$	1.04		1.71		2.82		ns
t$_{PTERMCO}$		1.13		1.34		1.69	ns

Table 51. EP20K30E f$_{MAX}$ Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.24		0.27		0.31	ns
t$_{F5-20}$		1.03		1.14		1.30	ns
t$_{F20+}$		1.42		1.54		1.77	ns

Table 62. EP20K100E f$_{MAX}$ ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{ESBARC}$		1.61		1.84		1.97	ns
t$_{ESBSRC}$		2.57		2.97		3.20	ns
t$_{ESBAWC}$		0.52		4.09		4.39	ns
t$_{ESBSWC}$		3.17		3.78		4.09	ns
t$_{ESBWASU}$	0.56		6.41		0.63		ns
t$_{ESBWAH}$	0.48		0.54		0.55		ns
t$_{ESBWDSU}$	0.71		0.80		0.81		ns
t$_{ESBWDH}$	.048		0.54		0.55		ns
t$_{ESBRASU}$	1.57		1.75		1.87		ns
t$_{ESBRAH}$	0.00		0.00		0.20		ns
t$_{ESBWESU}$	1.54		1.72		1.80		ns
t$_{ESBWEH}$	0.00		0.00		0.00		ns
t$_{ESBDATASU}$	-0.16		-0.20		-0.20		ns
t$_{ESBDATAH}$	0.13		0.13		0.13		ns
t$_{ESBWADDRSU}$	0.12		0.08		0.13		ns
t$_{ESBRADDRSU}$	0.17		0.15		0.19		ns
t$_{ESBDATACO1}$		1.20		1.39		1.52	ns
t$_{ESBDATACO2}$		2.54		2.99		3.22	ns
t$_{ESBDD}$		3.06		3.56		3.85	ns
t$_{PD}$		1.73		2.02		2.20	ns
t$_{PTERMSU}$	1.11		1.26		1.38		ns
t$_{PTERMCO}$		1.19		1.40		1.08	ns

Table 63. EP20K100E f$_{MAX}$ Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.24		0.27		0.29	ns
t$_{F5-20}$		1.04		1.26		1.52	ns
t$_{F20+}$		1.12		1.36		1.86	ns

Table 69. EP20K160E f$_{MAX}$ Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.25		0.26		0.28	ns
t$_{F5-20}$		1.00		1.18		1.35	ns
t$_{F20+}$		1.95		2.19		2.30	ns

Table 70. EP20K160E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{CH}$	1.34		1.43		1.55		ns
t$_{CL}$	1.34		1.43		1.55		ns
t$_{CLRP}$	0.18		0.19		0.21		ns
t$_{PREP}$	0.18		0.19		0.21		ns
t$_{ESBCH}$	1.34		1.43		1.55		ns
t$_{ESBCL}$	1.34		1.43		1.55		ns
t$_{ESBWP}$	1.15		1.45		1.73		ns
t$_{ESBRP}$	0.93		1.15		1.38		ns

Table 71. EP20K160E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSU}$	2.23		2.34		2.47		ns
t$_{INH}$	0.00		0.00		0.00		ns
t$_{OUTCO}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
t$_{INSUPLL}$	2.12		2.07		-		ns
t$_{INHPLL}$	0.00		0.00		-		ns
t$_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns

Table 72. EP20K160E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.86		3.24		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{XZBIDIR}$		7.43		8.23		8.58	ns
$t_{ZXBIDIR}$		7.43		8.23		8.58	ns
$t_{INSUBIDIRPLL}$	4.93		5.48		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{XZBIDIRPLL}$		5.36		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.36		5.99		-	ns

Tables 73 through 78 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

Table 73. EP20K200E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.24		0.26		ns
t_{H}	0.23		0.24		0.26		ns
t_{CO}		0.26		0.31		0.36	ns
t_{LUT}		0.70		0.90		1.14	ns

Table 74. EP20K200E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.68		2.06		2.24	ns
t_{ESBSRC}		2.27		2.77		3.18	ns
t_{ESBAWC}		3.10		3.86		4.50	ns
t_{ESBSWC}		2.90		3.67		4.21	ns
t_{ESBWASU}	0.55		0.67		0.74		ns
t_{ESBWAH}	0.36		0.46		0.48		ns
t_{ESBWDSU}	0.69		0.83		0.95		ns
t_{ESBWDH}	0.36		0.46		0.48		ns
t_{ESBRASU}	1.61		1.90		2.09		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
t_{ESBWESU}	1.42		1.71		2.01		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
t_{ESBDATASU}	-0.06		-0.07		0.05		ns
t_{ESBDATAH}	0.13		0.13		0.13		ns
t_{ESBWADDRSU}	0.11		0.13		0.31		ns
t_{ESBRADDRSU}	0.18		0.23		0.39		ns
t_{ESBDATACO1}		1.09		1.35		1.51	ns
t_{ESBDATACO2}		2.19		2.75		3.22	ns
t_{ESBDD}		2.75		3.41		4.03	ns
t_{PD}		1.58		1.97		2.33	ns
t_{PTERMSU}	1.00		1.22		1.51		ns
t_{PTERMCO}		1.10		1.37		1.09	ns

Table 75. EP20K200E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.27		0.29	ns
t_{F5-20}		1.02		1.20		1.41	ns
t_{F20+}		1.99		2.23		2.53	ns

Table 86. EP20K400E f_MAX ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_ESBARC		1.67		1.91		1.99	ns
t_ESBSRC		2.30		2.66		2.93	ns
t_ESBAWC		3.09		3.58		3.99	ns
t_ESBSWC		3.01		3.65		4.05	ns
t_ESBWASU	0.54		0.63		0.65		ns
t_ESBWAH	0.36		0.43		0.42		ns
t_ESBWDSU	0.69		0.77		0.84		ns
t_ESBWDH	0.36		0.43		0.42		ns
t_ESBRASU	1.61		1.77		1.86		ns
t_ESBRAH	0.00		0.00		0.01		ns
t_ESBWESU	1.35		1.47		1.61		ns
t_ESBWEH	0.00		0.00		0.00		ns
t_ESBDATASU	-0.18		-0.30		-0.27		ns
t_ESBDATAH	0.13		0.13		0.13		ns
t_ESBWADDRSU	-0.02		-0.11		-0.03		ns
t_ESBRADDRSU	0.06		-0.01		-0.05		ns
t_ESBDATACO1		1.16		1.40		1.54	ns
t_ESBDATACO2		2.18		2.55		2.85	ns
t_ESBDD		2.73		3.17		3.58	ns
t_PD		1.57		1.83		2.07	ns
t_PTERMSU	0.92		0.99		1.18		ns
t_PTERMCO		1.18		1.43		1.17	ns

Table 99. EP20K1000E f$_{MAX}$ Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{F1-4}$		0.27		0.27		0.27	ns
t$_{F5-20}$		1.45		1.63		1.75	ns
t$_{F20+}$		4.15		4.33		4.97	ns

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{CH}$	1.25		1.43		1.67		ns
t$_{CL}$	1.25		1.43		1.67		ns
t$_{CLRP}$	0.20		0.20		0.20		ns
t$_{PREP}$	0.20		0.20		0.20		ns
t$_{ESBCH}$	1.25		1.43		1.67		ns
t$_{ESBCL}$	1.25		1.43		1.67		ns
t$_{ESBWP}$	1.28		1.51		1.65		ns
t$_{ESBRP}$	1.11		1.29		1.41		ns

Table 101. EP20K1000E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t$_{INSU}$	2.70		2.84		2.97		ns
t$_{INH}$	0.00		0.00		0.00		ns
t$_{OUTCO}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
t$_{INSUPLL}$	1.64		2.09		-		ns
t$_{INHPLL}$	0.00		0.00		-		ns
t$_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns