Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2560
Number of Logic Elements/Cells	2560
Total RAM Bits	32768
Number of I/O	92
Number of Gates	162000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k60etc144-1

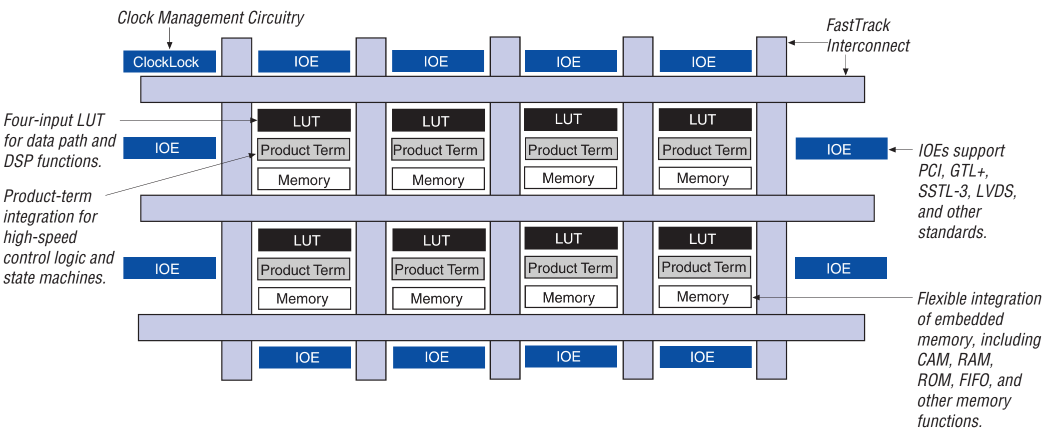
Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram

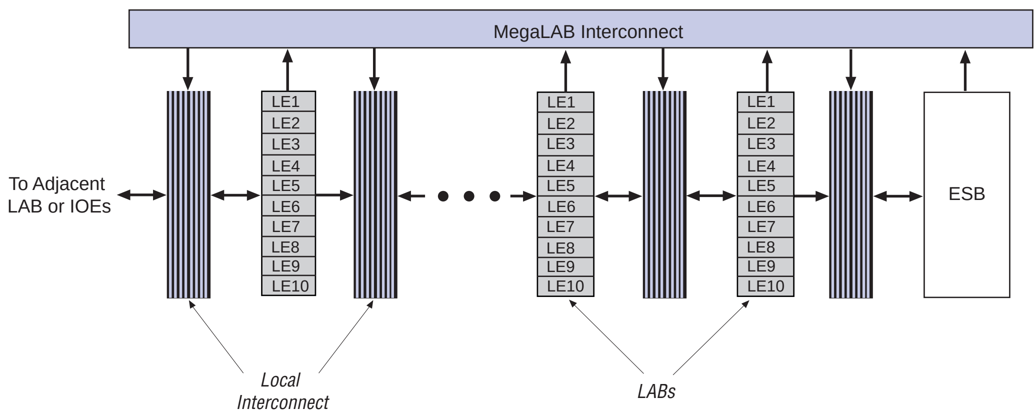


APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

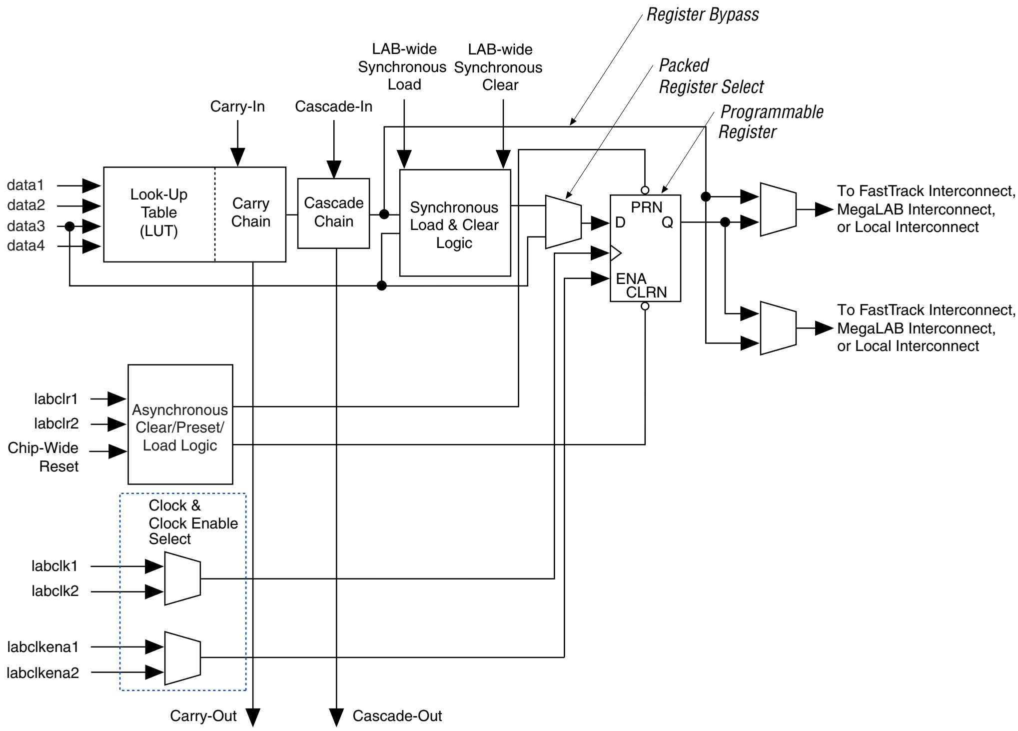
Figure 2. MegaLAB Structure



Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

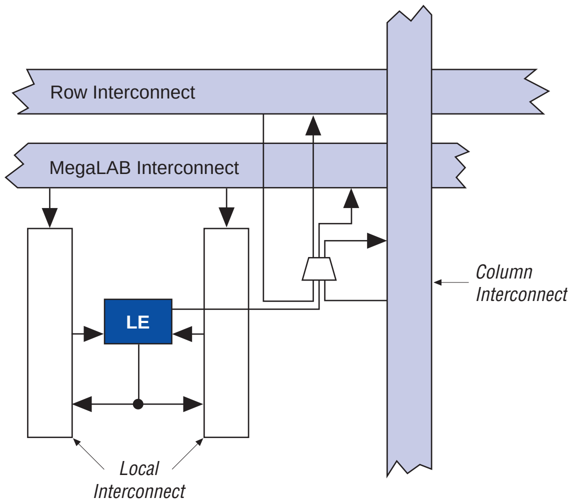
Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

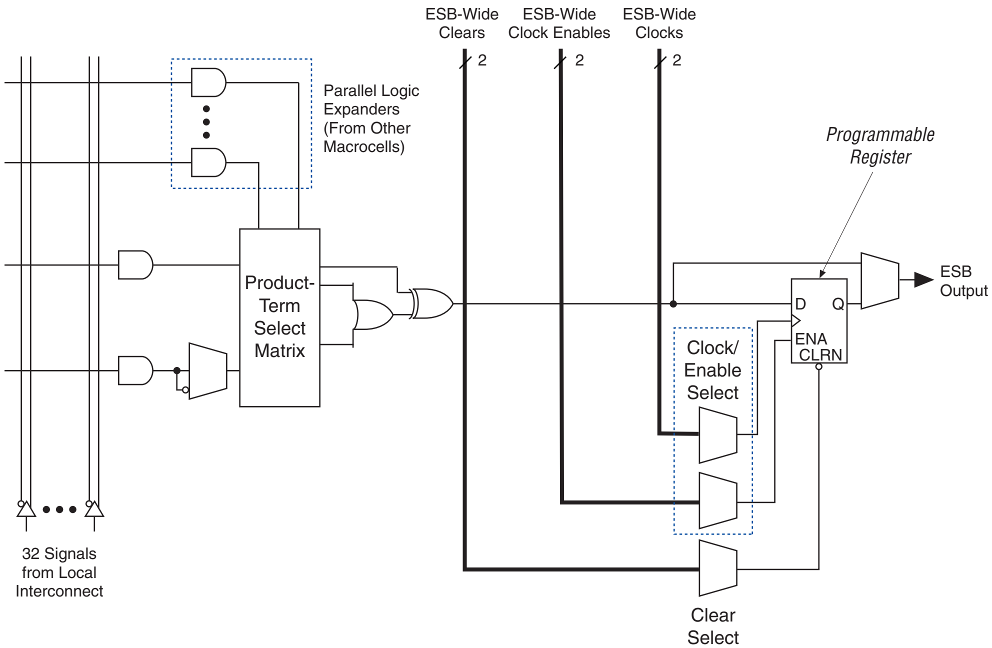
Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABS in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Figure 14. APEX 20K Macrocell



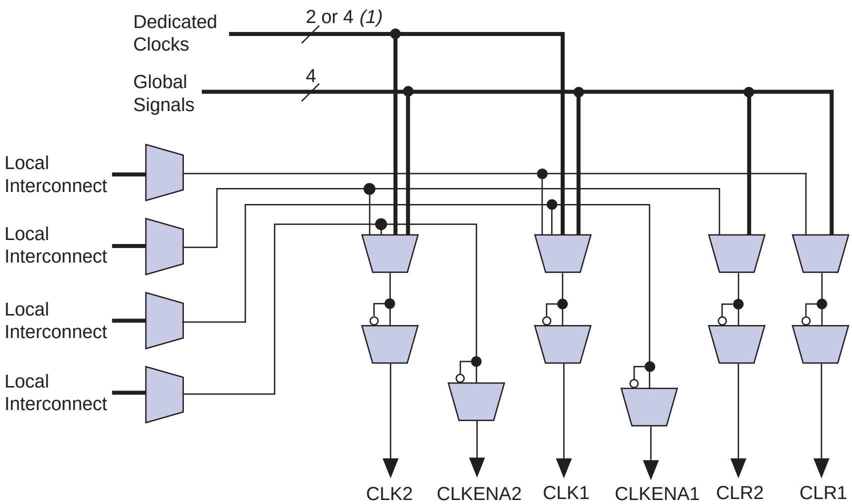
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Note to Figure 15:

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

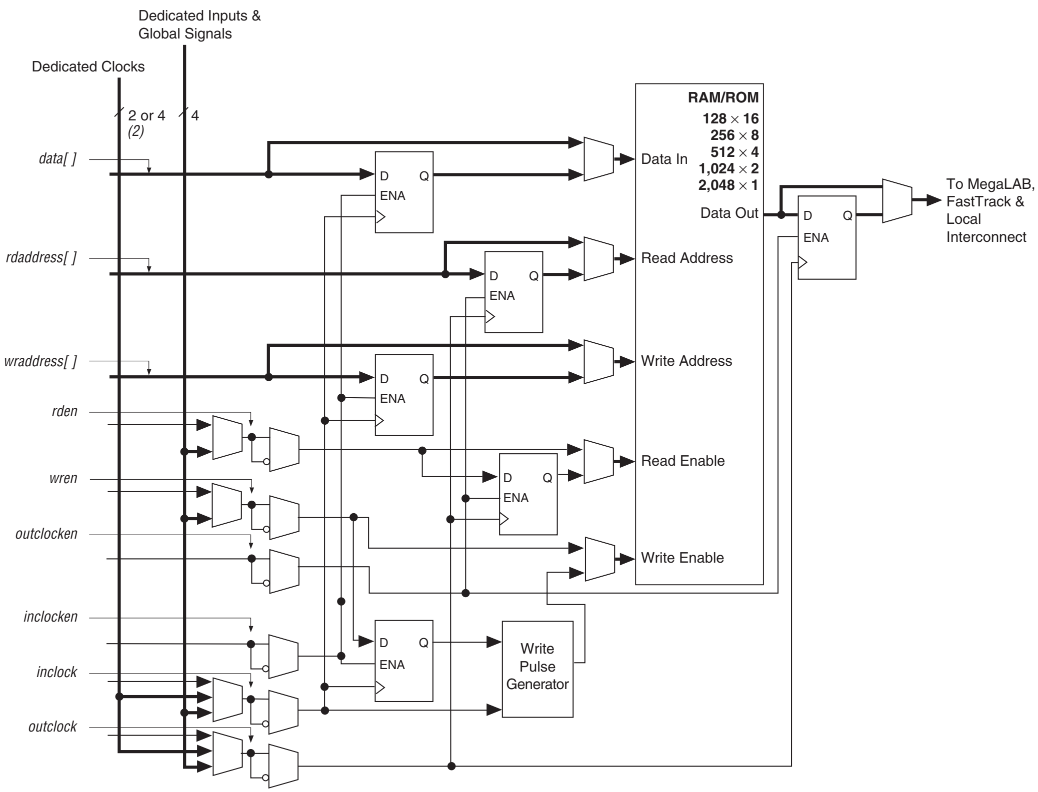
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Notes to Figure 20:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

Table 11. APEX 20KE Programmable Delay Chains

Programmable Delays	Quartus II Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Notes to Table 16:

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus II software, designers must specify the input frequency. The Quartus II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

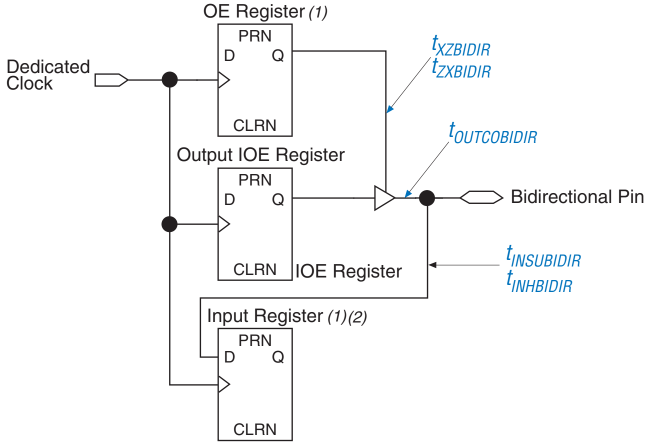
Table 17. APEX 20KE ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	peak-to-peak
$t_{OUTJITTER}$	Jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	RMS
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
t_{LOCK} (2), (3)	Time required for ClockLock or ClockBoost to acquire lock				40	µs

Table 29. APEX 20KE Device DC Operating Conditions *Notes (7), (8), (9)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V_{CCIO} *(10)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(10)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V *(11)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(11)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(11)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(11)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(11)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(11)*	1.7			V
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(12)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(12)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(12)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(12)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(12)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(12)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V *(13)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V *(13)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(14)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(14)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(14)*	60		150	kΩ

Figure 40. Synchronous Bidirectional Pin External Timing



Notes to Figure 40:

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the f_{MAX} timing parameters shown in Figure 36 on page 68.

Table 31. APEX 20K f_{MAX} Timing Parameters (Part 1 of 2)

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in
t_{ESBRC}	ESB Asynchronous read cycle time
t_{ESBWC}	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBADDRSU}$	ESB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers

Table 39. APEX 20KE External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{XZBIDIRPLL}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{ZXBIDIRPLL}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

Note to Tables 38 and 39:

(1) These timing parameters are sample-tested only.

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.6		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 42. EP20K400 f_{MAX} Timing Parameters							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.1		0.3		0.6		ns
t_{H}	0.5		0.8		0.9		ns
t_{CO}		0.1		0.4		0.6	ns
t_{LUT}		1.0		1.2		1.4	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
t_{F1-4}		0.4		0.5		0.6	ns
t_{F5-20}		2.6		2.8		2.9	ns
t_{F20+}		3.7		3.8		3.9	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.5		0.6		0.8		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.5		1.9		2.2		ns
t_{ESBRP}	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Notes to Tables 43 through 48:
(1) This parameter is measured without using ClockLock or ClockBoost circuits.
(2) This parameter is measured using ClockLock or ClockBoost circuits.

Tables 49 through 54 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K30E APEX 20KE devices.

Table 49. EP20K30E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.01		0.02		0.02		ns
t_H	0.11		0.16		0.23		ns
t_{CO}		0.32		0.45		0.67	ns
t_{LUT}		0.85		1.20		1.77	ns

Tables 55 through 60 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

Table 55. EP20K60E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.17		0.15		0.16		ns
t_{H}	0.32		0.33		0.39		ns
t_{CO}		0.29		0.40		0.60	ns
t_{LUT}		0.77		1.07		1.59	ns

Table 74. EP20K200E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.68		2.06		2.24	ns
t_{ESBSRC}		2.27		2.77		3.18	ns
t_{ESBAWC}		3.10		3.86		4.50	ns
t_{ESBSWC}		2.90		3.67		4.21	ns
$t_{ESBWASU}$	0.55		0.67		0.74		ns
t_{ESBWAH}	0.36		0.46		0.48		ns
$t_{ESBWDSU}$	0.69		0.83		0.95		ns
t_{ESBWDH}	0.36		0.46		0.48		ns
$t_{ESBRASU}$	1.61		1.90		2.09		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.42		1.71		2.01		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.06		-0.07		0.05		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.13		0.31		ns
$t_{ESBRADDRSU}$	0.18		0.23		0.39		ns
$t_{ESBDATACO1}$		1.09		1.35		1.51	ns
$t_{ESBDATACO2}$		2.19		2.75		3.22	ns
t_{ESBDD}		2.75		3.41		4.03	ns
t_{PD}		1.58		1.97		2.33	ns
$t_{PTERMSU}$	1.00		1.22		1.51		ns
$t_{PTERMCO}$		1.10		1.37		1.09	ns

Table 75. EP20K200E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.27		0.29	ns
t_{F5-20}		1.02		1.20		1.41	ns
t_{F20+}		1.99		2.23		2.53	ns

Table 86. EP20K400E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		1.91		1.99	ns
t_{ESBSRC}		2.30		2.66		2.93	ns
t_{ESBAWC}		3.09		3.58		3.99	ns
t_{ESBSWC}		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
t_{ESBWAH}	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
t_{ESBWDH}	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
t_{ESBDD}		2.73		3.17		3.58	ns
t_{PD}		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

Table 110. Selectable I/O Standard Output Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		–0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		–0.48		–0.48		–0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.