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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2560 |
| Number of Logic Elements/Cells | 2560 |
| Total RAM Bits | 32768 |
| Number of I/O | 92 |
| Number of Gates | 162000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k60etc144-3n |

## General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices.

### *LE Operating Modes*

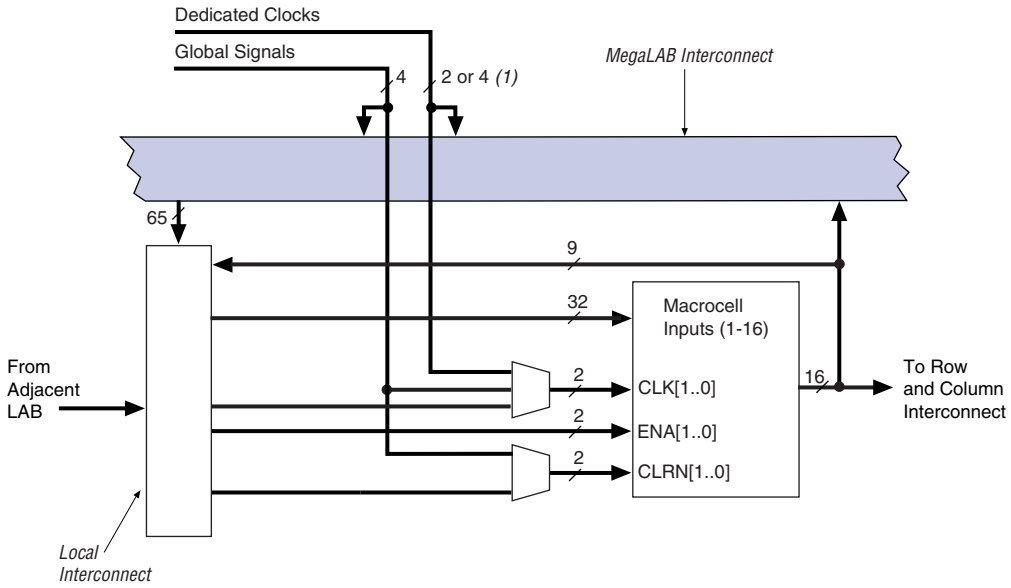
The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

*Figure 13. Product-Term Logic in ESB*



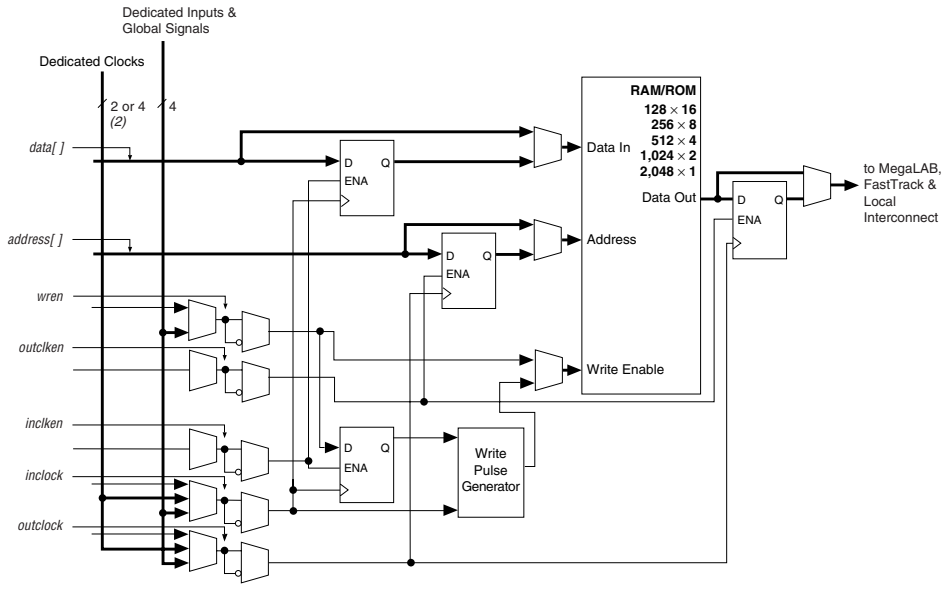

*Note to Figure 13:*
(1) APEX 20KE devices have four dedicated clocks.

## Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

*Figure 22. ESB in Single-Port Mode* *Note (1)*




*Notes to Figure 22:*

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

*Table 13. APEX 20KE MultiVolt I/O Support* *Note (1)*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | *(2)* | | | ✓ *(3)* | |

*Notes to Table 13:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

*Table 14. Multiplication Factor Combinations*

| Clock 1 | Clock 2 |
|---|---|
| ×1 | ×1 |
| ×1, ×2 | ×2 |
| ×1, ×2, ×4 | ×4 |

## APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

### *External PLL Feedback*

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

### *Clock Multiplication*

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where $m$ and $k$ range from 2 to 160, and $n$ and $v$ range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

*Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SKEW}$ | Skew delay between related ClockLock/ClockBoost-generated clocks | | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ClockBoost-generated clock *(5)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

*Notes to Table 15:*

(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, $t_{JITTER}$ is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

*Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | 25 | 170 | MHz |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 170 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 80 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 34 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)* | | 25,000 *(2)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ ClockBoost to acquire lock *(3)* | | 10 | µs |
| $t_{SKEW}$ | Skew delay between related ClockLock/ ClockBoost-generated clock | 500 | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ ClockBoost-generated clock *(4)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

*Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | I/O Standard | -1X Speed Grade | | -2X Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{VCO}$ *(4)* | Voltage controlled oscillator operating range | | 200 | 500 | 200 | 500 | MHz |
| $f_{CLOCK0}$ | `Clock0` PLL output frequency for internal use | | 1.5 | 335 | 1.5 | 200 | MHz |
| $f_{CLOCK1}$ | `Clock1` PLL output frequency for internal use | | 20 | 335 | 20 | 200 | MHz |
| $f_{CLOCK0\_EXT}$ | Output clock frequency for external `clock0` output | 3.3-V LVTTL | 1.5 | 245 | 1.5 | 226 | MHz |
| | | 2.5-V LVTTL | 1.5 | 234 | 1.5 | 221 | MHz |
| | | 1.8-V LVTTL | 1.5 | 223 | 1.5 | 216 | MHz |
| | | GTL+ | 1.5 | 205 | 1.5 | 193 | MHz |
| | | SSTL-2 Class I | 1.5 | 158 | 1.5 | 157 | MHz |
| | | SSTL-2 Class II | 1.5 | 142 | 1.5 | 142 | MHz |
| | | SSTL-3 Class I | 1.5 | 166 | 1.5 | 162 | MHz |
| | | SSTL-3 Class II | 1.5 | 149 | 1.5 | 146 | MHz |
| | | LVDS | 1.5 | 420 | 1.5 | 350 | MHz |
| $f_{CLOCK1\_EXT}$ | Output clock frequency for external `clock1` output | 3.3-V LVTTL | 20 | 245 | 20 | 226 | MHz |
| | | 2.5-V LVTTL | 20 | 234 | 20 | 221 | MHz |
| | | 1.8-V LVTTL | 20 | 223 | 20 | 216 | MHz |
| | | GTL+ | 20 | 205 | 20 | 193 | MHz |
| | | SSTL-2 Class I | 20 | 158 | 20 | 157 | MHz |
| | | SSTL-2 Class II | 20 | 142 | 20 | 142 | MHz |
| | | SSTL-3 Class I | 20 | 166 | 20 | 162 | MHz |
| | | SSTL-3 Class II | 20 | 149 | 20 | 146 | MHz |
| | | LVDS | 20 | 420 | 20 | 350 | MHz |

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

*Table 22. APEX 20K JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

*Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions* *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4), (5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3), (6)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)* *Notes (2), (7), (8)*

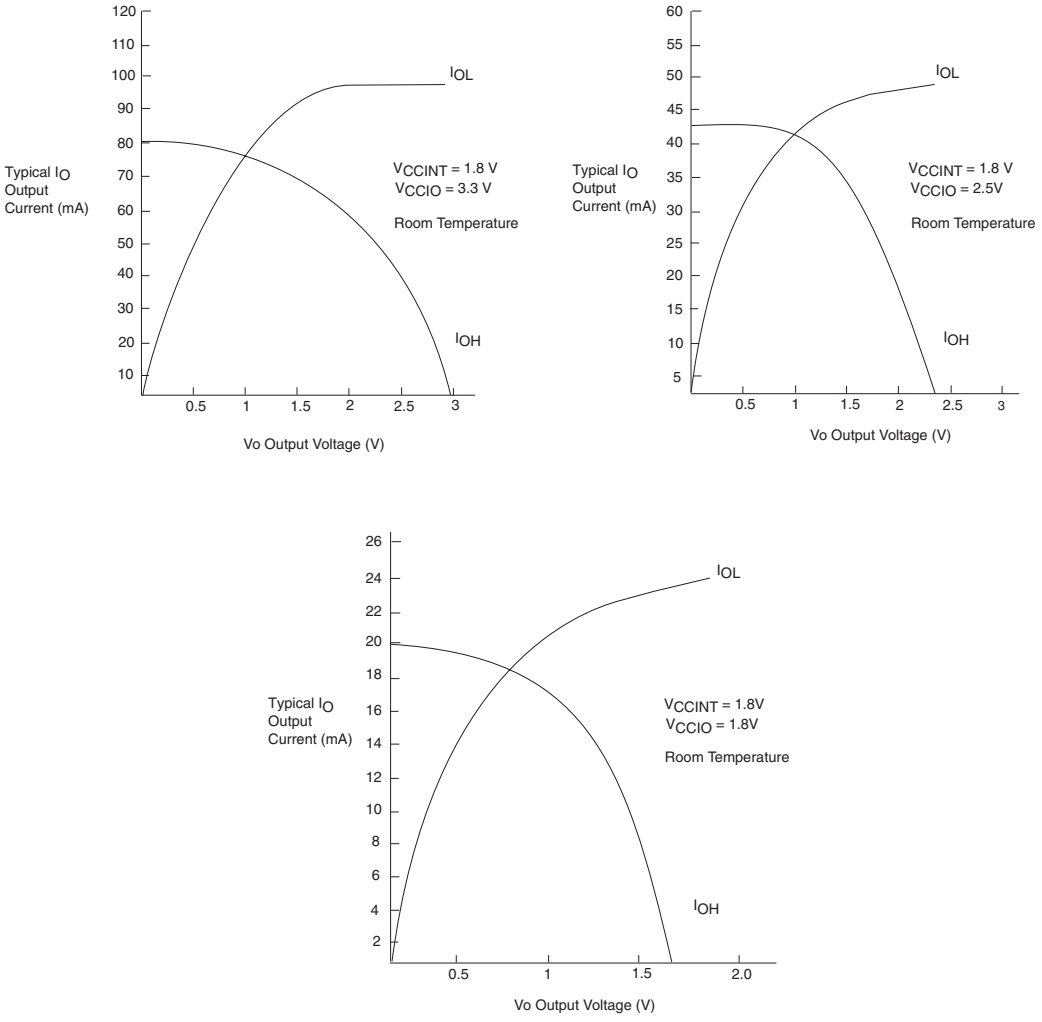
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(9)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 1.7 | | | V |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(11)* | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade *(12)* | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades *(12)* | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | W |
| | | $V_{CCIO}$ = 2.375 V *(13)* | 30 | | 80 | W |

Figure 35 shows the output drive characteristics of APEX 20KE devices.

***Figure 35. Output Drive Characteristics of APEX 20KE Devices*** *Note (1)*




*Note to Figure 35:*
(1) These are transient (AC) currents.

## Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

*Figure 37. APEX 20KE $f_{MAX}$ Timing Model*

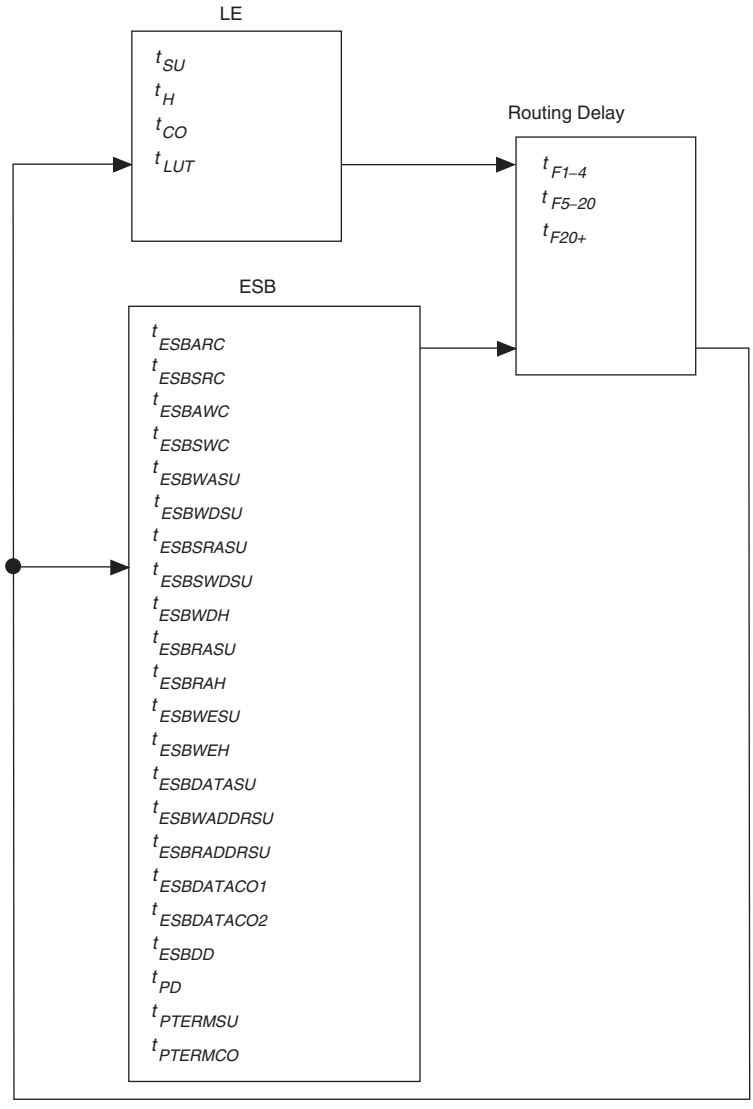
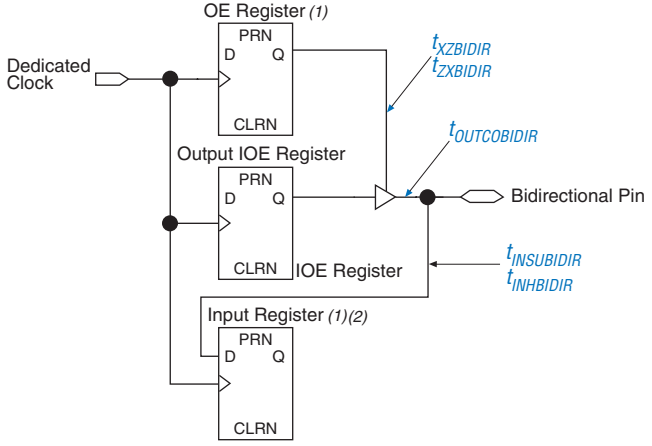


*Figure 40. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 40:*

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the $f_{MAX}$ timing parameters shown in Figure 36 on page 68.

*Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 1 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{ESBRC}$ | ESB Asynchronous read cycle time |
| $t_{ESBWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |

| Table 39. APEX 20KE External Bidirectional Timing Parameters Note (1) | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous Output Enable Register to output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous Output Enable Register output buffer enable delay | C1 = 10 pF |
| $t_{INSUBIDIRPLL}$ | Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{INHBIDIRPLL}$ | Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIRPLL}$ | Clock-to-output delay for bidirectional pins with PLL clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIRPLL}$ | Synchronous Output Enable Register to output buffer disable delay with PLL | C1 = 10 pF |
| $t_{ZXBIDIRPLL}$ | Synchronous Output Enable Register output buffer enable delay with PLL | C1 = 10 pF |

*Note to Tables 38 and 39:*
(1) These timing parameters are sample-tested only.

*Table 72. EP20K160E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.86 | | 3.24 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{XZBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{ZXBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{INSUBIDIRPLL}$ | 4.93 | | 5.48 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |

Tables 73 through 78 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

*Table 73. EP20K200E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.26 | | 0.31 | | 0.36 | ns |
| $t_{LUT}$ | | 0.70 | | 0.90 | | 1.14 | ns |

Tables 85 through 90 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

*Table 85. EP20K400E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{H}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{CO}$ | | 0.25 | | 0.29 | | 0.32 | ns |
| $t_{LUT}$ | | 0.70 | | 0.83 | | 1.01 | ns |

*Table 87. EP20K400E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.01 | | 1.12 | | 1.25 | ns |
| $t_{F20+}$ | | 3.71 | | 3.92 | | 4.17 | ns |

*Table 88. EP20K400E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.36 | | 2.22 | | 2.35 | | ns |
| $t_{CL}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.18 | | 0.19 | | ns |
| $t_{PREP}$ | 0.18 | | 0.18 | | 0.19 | | ns |
| $t_{ESBCH}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{ESBCL}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{ESBWP}$ | 1.17 | | 1.38 | | 1.56 | | ns |
| $t_{ESBRP}$ | 0.94 | | 1.09 | | 1.25 | | ns |

*Table 89. EP20K400E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.51 | | 2.64 | | 2.77 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.25 | 2.00 | 5.79 | 2.00 | 6.32 | ns |
| $t_{INSUPLL}$ | 3.221 | | 3.38 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.45 | - | - | ns |

*Table 99. EP20K1000E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.27 | | 0.27 | | 0.27 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.63 | | 1.75 | ns |
| $t_{F20+}$ | | 4.15 | | 4.33 | | 4.97 | ns |

*Table 100. EP20K1000E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 101. EP20K1000E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.70 | | 2.84 | | 2.97 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{INSUPLL}$ | 1.64 | | 2.09 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | - | - | ns |