**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | HCS12 |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | PWM, WDT |
| Number of I/O | 59 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 5.25V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-QFP |
| Supplier Device Package | 80-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12a64cfue |

# List of Tables

## Table 0-2 Document References

| User Guide | Version | Document Order Number |
|---|---|---|
| HCS12 CPU Reference Manual | V02 | S12CPUV2/D |
| HCS12 Module Mapping Control (MMC) Block Guide | V04 | S12MMCV4/D |
| HCS12 Multiplexed External Bus Interface (MEBI) Block Guide | V03 | S12MEBIV3/D |
| HCS12 Interrupt (INT) Block Guide | V01 | S12INTV1/D |
| HCS12 Background Debug (BDM) Block Guide | V04 | S12BDMV4/D |
| HCS12 Breakpoint (BKP) Block Guide | V01 | S12BKPV1/D |
| Clock and Reset Generator (CRG) Block User Guide | V04 | S12CRGV4/D |
| Oscillator (OSC) Block User Guide | V02 | S12OSCV2/D |
| Enhanced Capture Timer 16 Bit 8 Channel (ECT_16B8C) Block User Guide | V01 | S12ECT16B8CV1/D |
| Analog to Digital Converter 10 Bit 8 Channel (ATD_10B8C) Block User Guide | V02 | S12ATD10B8CV2/D |
| Inter IC Bus (IIC) Block User Guide | V02 | S12IICV2/D |
| Asynchronous Serial Interface (SCI) Block User Guide | V02 | S12SCIV2/D |
| Serial Peripheral Interface (SPI) Block User Guide | V02 | S12SPIV2/D |
| Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide | V01 | S12PWM8B8CV1/D |
| 64K Byte Flash (FTS64K) Block User Guide | V01 | S12FTS64KV1/D |
| 1K Byte EEPROM (EETS1K) Block User Guide | V01 | S12EETS1KV1/D |
| Byte Level Data Link Controller -J1850 (BDLC) Block User Guide | V01 | S12BDLCV1/D |
| Freescale Scalable CAN (MSCAN) Block User Guide | V02 | S12MSCANV2/D |
| Voltage Regulator (VREG) Block User Guide | V01 | S12VREGV1/D |
| Port Integration Module (PIM_9DJ64) Block User Guide | V01 | S12PIM9DJ64V1/D |

## 1.5.1 Detailed Register Map

### $0000 - $000F MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0000 | PORTA | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $0001 | PORTB | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $0002 | DDRA | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $0003 | DDRB | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $0004 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0005 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0006 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0007 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0008 | PORTE | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | Bit 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $0009 | DDRE | Read: | Bit 7 | 6 | 5 | 4 | 3 | Bit 2 | 0 | 0 |
| | | Write: | | | | | | | | |
| $000A | PEAR | Read: | NOACCE | 0 | PIPOE | NECLK | LSTRE | RDWE | 0 | 0 |
| | | Write: | | | | | | | | |
| $000B | MODE | Read: | MODC | MODB | MODA | 0 | IVIS | 0 | EMK | EME |
| | | Write: | | | | | | | | |
| $000C | PUCR | Read: | PUPKE | 0 | 0 | PUPEE | 0 | 0 | PUPBE | PUPAE |
| | | Write: | | | | | | | | |
| $000D | RDRIV | Read: | RDPK | 0 | 0 | RDPE | 0 | 0 | RDPB | RDPA |
| | | Write: | | | | | | | | |
| $000E | EBICTL | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ESTR |
| | | Write: | | | | | | | | |
| $000F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

### $0010 - $0014 MMC map 1 of 4 (HCS12 Module Mapping Control)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0010 | INITRM | Read: | RAM15 | RAM14 | RAM13 | RAM12 | RAM11 | 0 | 0 | RAMHAL |
| | | Write: | | | | | | | | |
| $0011 | INITRG | Read: | 0 | REG14 | REG13 | REG12 | REG11 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $007C | TC2H (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| $007D | TC2H (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $007E | TC3H (hi) | Read: | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit 8 |
| | | Write: | | | | | | | | |
| $007F | TC3H (lo) | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |

## $0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0080 | ATD0CTL0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0081 | ATD0CTL1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0082 | ATD0CTL2 | Read: | ADPU | AFFC | AWAI | ETRIGLE | ETRIGP | ETRIG | ASCIE | ASCIF |
| | | Write: | | | | | | | | |
| $0083 | ATD0CTL3 | Read: | 0 | S8C | S4C | S2C | S1C | FIFO | FRZ1 | FRZ0 |
| | | Write: | | | | | | | | |
| $0084 | ATD0CTL4 | Read: | SRES8 | SMP1 | SMP0 | PRS4 | PRS3 | PRS2 | PRS1 | PRS0 |
| | | Write: | | | | | | | | |
| $0085 | ATD0CTL5 | Read: | DJM | DSGN | SCAN | MULT | 0 | CC | CB | CA |
| | | Write: | | | | | | | | |
| $0086 | ATD0STAT0 | Read: | SCF | 0 | ETORF | FIFOR | 0 | CC2 | CC1 | CC0 |
| | | Write: | | | | | | | | |
| $0087 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0088 | ATD0TEST0 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0089 | ATD0TEST1 | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC |
| | | Write: | | | | | | | | |
| $008A | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $008B | ATD0STAT1 | Read: | CCF7 | CCF6 | CCF5 | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 |
| | | Write: | | | | | | | | |
| $008C | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $008D | ATD0DIEN | Read: | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | | Write: | | | | | | | | |
| $008E | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $008F | PORTAD0 | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | BIT 0 |
| | | Write: | | | | | | | | |
| $0090 | ATD0DR0H | Read: | Bit15 | 14 | 13 | 12 | 11 | 10 | 9 | Bit8 |
| | | Write: | | | | | | | | |
| $0091 | ATD0DR0L | Read: | Bit7 | Bit6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $00D5 | SCI1SR2 | Read: | 0 | 0 | 0 | 0 | 0 | BRK13 | TXDIR | RAF |
| | | Write: | | | | | | | | |
| $00D6 | SCI1DRH | Read: | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00D7 | SCI1DRL | Read: | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| | | Write: | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

## $00D8 - $00DF SPI0 (Serial Peripheral Interface)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $00D8 | SPI0CR1 | Read: | SPIE | SPE | SPTIE | MSTR | CPOL | CPHA | SSOE | LSBFE |
| | | Write: | | | | | | | | |
| $00D9 | SPI0CR2 | Read: | 0 | 0 | 0 | MODFEN | BIDIROE | 0 | SPISWAI | SPC0 |
| | | Write: | | | | | | | | |
| $00DA | SPI0BR | Read: | 0 | SPPR2 | SPPR1 | SPPR0 | 0 | SPR2 | SPR1 | SPR0 |
| | | Write: | | | | | | | | |
| $00DB | SPI0SR | Read: | SPIF | 0 | SPTEF | MODF | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00DC | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00DD | SPI0DR | Read: | Bit7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit0 |
| | | Write: | | | | | | | | |
| $00DE | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00DF | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $00E0 - $00E7 IIC (Inter IC Bus)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $00E0 | IBAD | Read: | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | 0 |
| | | Write: | | | | | | | | |
| $00E1 | IBFD | Read: | IBC7 | IBC6 | IBC5 | IBC4 | IBC3 | IBC2 | IBC1 | IBC0 |
| | | Write: | | | | | | | | |
| $00E2 | IBCR | Read: | IBEN | IBIE | MS/$\overline{SL}$ | TX/$\overline{RX}$ | TXAK | 0 | 0 | IBSWAI |
| | | Write: | | | | | | RSTA | | |
| $00E3 | IBSR | Read: | TCF | IAAS | IBB | IBAL | 0 | SRW | IBIF | RXAK |
| | | Write: | | | | | | | | |
| $00E4 | IBDR | Read: | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D 0 |
| | | Write: | | | | | | | | |
| $00E5 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00E6 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $00E7 | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |

## $0240 - $027F PIM (Port Integration Module)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $024A | DDRS | Read: | DDRS7 | DDRS7 | DDRS5 | DDRS4 | DDRS3 | DDRS2 | DDRS1 | DDRS0 |
| | | Write: | | | | | | | | |
| $024B | RDRS | Read: | RDRS7 | RDRS6 | RDRS5 | RDRS4 | RDRS3 | RDRS2 | RDRS1 | RDRS0 |
| | | Write: | | | | | | | | |
| $024C | PERS | Read: | PERS7 | PERS6 | PERS5 | PERS4 | PERS3 | PERS2 | PERS1 | PERS0 |
| | | Write: | | | | | | | | |
| $024D | PPSS | Read: | PPSS7 | PPSS6 | PPSS5 | PPSS4 | PPSS3 | PPSS2 | PPSS1 | PPSS0 |
| | | Write: | | | | | | | | |
| $024E | WOMS | Read: | WOMS7 | WOMS6 | WOMS5 | WOMS4 | WOMS3 | WOMS2 | WOMS1 | WOMS0 |
| | | Write: | | | | | | | | |
| $024F | Reserved | Read: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Write: | | | | | | | | |
| $0250 | PTM | Read: | PTM7 | PTM6 | PTM5 | PTM4 | PTM3 | PTM2 | PTM1 | PTM0 |
| | | Write: | | | | | | | | |
| $0251 | PTIM | Read: | PTIM7 | PTIM6 | PTIM5 | PTIM4 | PTIM3 | PTIM2 | PTIM1 | PTIM0 |
| | | Write: | | | | | | | | |
| $0252 | DDRM | Read: | DDRM7 | DDRM7 | DDRM5 | DDRM4 | DDRM3 | DDRM2 | DDRM1 | DDRM0 |
| | | Write: | | | | | | | | |
| $0253 | RDRM | Read: | RDRM7 | RDRM6 | RDRM5 | RDRM4 | RDRM3 | RDRM2 | RDRM1 | RDRM0 |
| | | Write: | | | | | | | | |
| $0254 | PERM | Read: | PERM7 | PERM6 | PERM5 | PERM4 | PERM3 | PERM2 | PERM1 | PERM0 |
| | | Write: | | | | | | | | |
| $0255 | PPSM | Read: | PPSM7 | PPSM6 | PPSM5 | PPSM4 | PPSM3 | PPSM2 | PPSM1 | PPSM0 |
| | | Write: | | | | | | | | |
| $0256 | WOMM | Read: | WOMM7 | WOMM6 | WOMM5 | WOMM4 | WOMM3 | WOMM2 | WOMM1 | WOMM0 |
| | | Write: | | | | | | | | |
| $0257 | MODRR | Read: | 0 | 0 | 0 | MODRR4 | 0 | 0 | MODRR1 | MODRR0 |
| | | Write: | | | | | | | | |
| $0258 | PTP | Read: | PTP7 | PTP6 | PTP5 | PTP4 | PTP3 | PTP2 | PTP1 | PTP0 |
| | | Write: | | | | | | | | |
| $0259 | PTIP | Read: | PTIP7 | PTIP6 | PTIP5 | PTIP4 | PTIP3 | PTIP2 | PTIP1 | PTIP0 |
| | | Write: | | | | | | | | |
| $025A | DDRP | Read: | DDRP7 | DDRP7 | DDRP5 | DDRP4 | DDRP3 | DDRP2 | DDRP1 | DDRP0 |
| | | Write: | | | | | | | | |
| $025B | RDRP | Read: | RDRP7 | RDRP6 | RDRP5 | RDRP4 | RDRP3 | RDRP2 | RDRP1 | RDRP0 |
| | | Write: | | | | | | | | |
| $025C | PERP | Read: | PERP7 | PERP6 | PERP5 | PERP4 | PERP3 | PERP2 | PERP1 | PERP0 |
| | | Write: | | | | | | | | |
| $025D | PPSP | Read: | PPSP7 | PPSP6 | PPSP5 | PPSP4 | PPSP3 | PPSP2 | PPSP1 | PPSS0 |
| | | Write: | | | | | | | | |
| $025E | PIEP | Read: | PIEP7 | PIEP6 | PIEP5 | PIEP4 | PIEP3 | PIEP2 | PIEP1 | PIEP0 |
| | | Write: | | | | | | | | |
| $025F | PIFP | Read: | PIFP7 | PIFP6 | PIFP5 | PIFP4 | PIFP3 | PIFP2 | PIFP1 | PIFP0 |
| | | Write: | | | | | | | | |
| $0260 | PTH | Read: | PTH7 | PTH6 | PTH5 | PTH4 | PTH3 | PTH2 | PTH1 | PTH0 |
| | | Write: | | | | | | | | |
| $0261 | PTIH | Read: | PTIH7 | PTIH6 | PTIH5 | PTIH4 | PTIH3 | PTIH2 | PTIH1 | PTIH0 |
| | | Write: | | | | | | | | |
| $0262 | DDRH | Read: | DDRH7 | DDRH7 | DDRH5 | DDRH4 | DDRH3 | DDRH2 | DDRH1 | DDRH0 |
| | | Write: | | | | | | | | |

### 2.3.14 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

### 2.3.15 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

### 2.3.16 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

### 2.3.17 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

### 2.3.18 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

### 2.3.19 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

### 2.3.20 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

### 2.3.21 PH7 / KWH7 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

| Mnemonic | Pin Number 112-pin QFP | Nominal Voltage | Description |
|---|---|---|---|
| VDDPLL | 43 | 2.5V | Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator. |
| VSSPLL | 45 | 0V | |
| VREGEN | 97 | 5.0V | Internal Voltage Regulator enable/disable |

### 2.4.1 VDDX, VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDX and VSSX are the supplies for Ports J, K, M, P, T and S.

### 2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDR and VSSR are the supplies for Ports A, B, E and H.

### 2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

***NOTE:*** *No load allowed except for bypass capacitors.*

### 2.4.4 VDDA, VSSA — Power Supply Pins for ATD0/ATD1 and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the two analog to digital converters. It also provides the reference for the internal voltage regulator. This allows the supply voltage to ATD0/ATD1 and the reference voltage to be bypassed independently.

#### 4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

### 4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode or via a sequence of BDM commands. Unsecuring is also possible via the Backdoor Key Access. Refer to Flash Block Guide for details.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

## 4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

### 4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

### 4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

### 4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and data bus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

### 4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

Consult the FTS64K Block User Guide for information about the flash module.

The "S12 LRAE" is a generic Load RAM and Execute (LRAE) program which will be programmed into the flash memory of this device during manufacture. This LRAE program will provide greater programming flexibility to the end users by allowing the device to be programmed directly using CAN or SCI after it is assembled on the PCB. Use of the LRAE program is at the discretion of the end user and, if not required, it must simply be erased prior to flash programming. For more details of the S12 LRAE and its implementation, please see the S12 LREA Application Note (AN2546/D).

It is planned that most HC9S12 devices manufactured after Q1 of 2004 will be shipped with the S12 LRAE programmed in the Flash . Exact details of the changeover (ie blank to programmed) for each product will be communicated in advance via GPCN and will be traceable by the customer via datecode marking on the device.

Please contact Freescale SPS Sales if you have any additional questions.

# Section 17 EEPROM 1K Block Description

Consult the EETS1K Block User Guide for information about the EEPROM module.

# Section 18 RAM Block Description

This module supports single-cycle misaligned word accesses.

# Section 19 MSCAN Block Description

Consult the MSCAN Block User Guide for information about the Freescale Scalable CAN Module.

# Section 20 Port Integration Module (PIM) Block Description

Consult the PIM_9DJ64 Block User Guide for information about the Port Integration Module.

# Section 21 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

# Section 22 Printed Circuit Board Layout Proposals

## Figure 22-1 Recommended PCB Layout 112LQFP Colpitts Oscillator

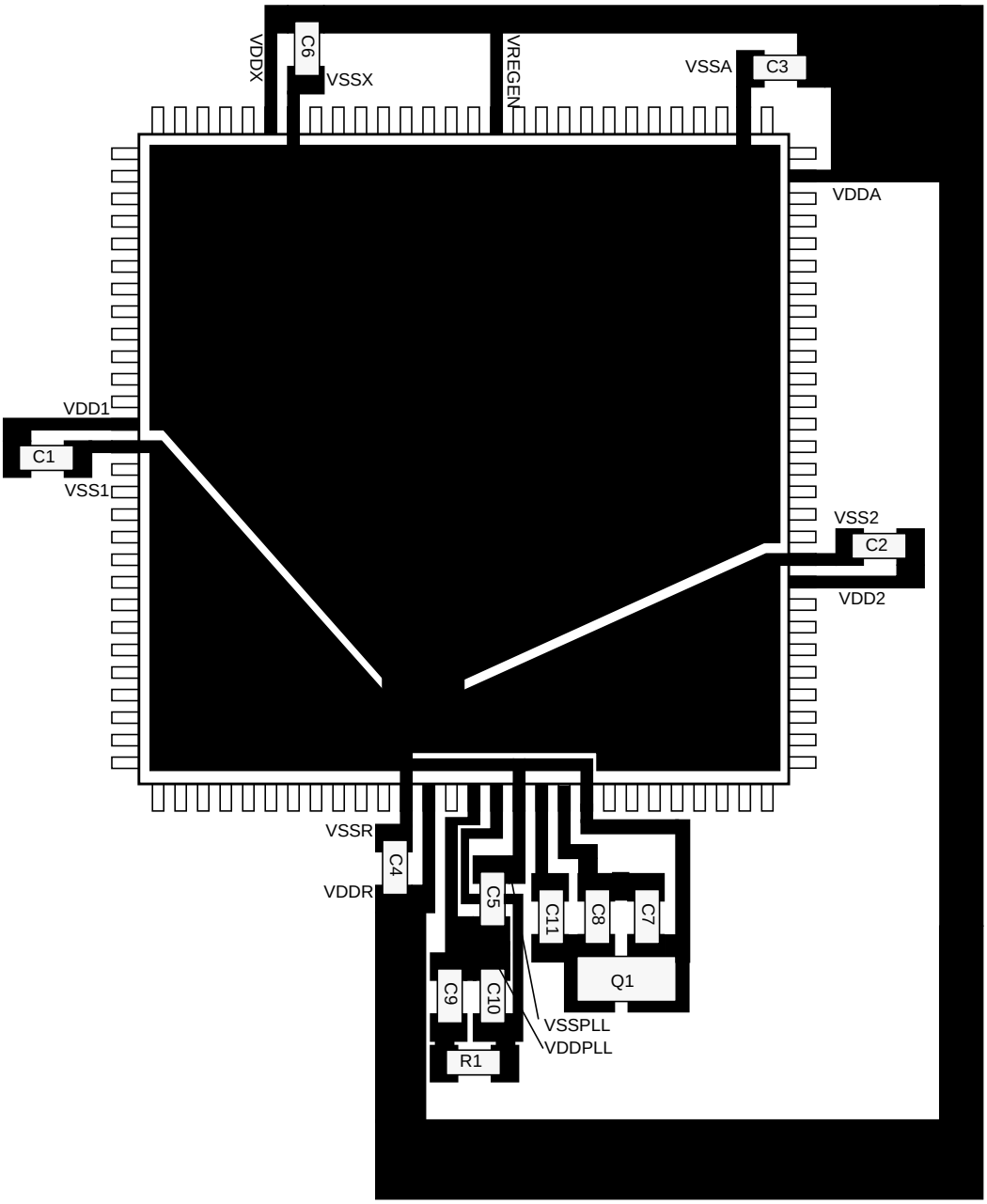
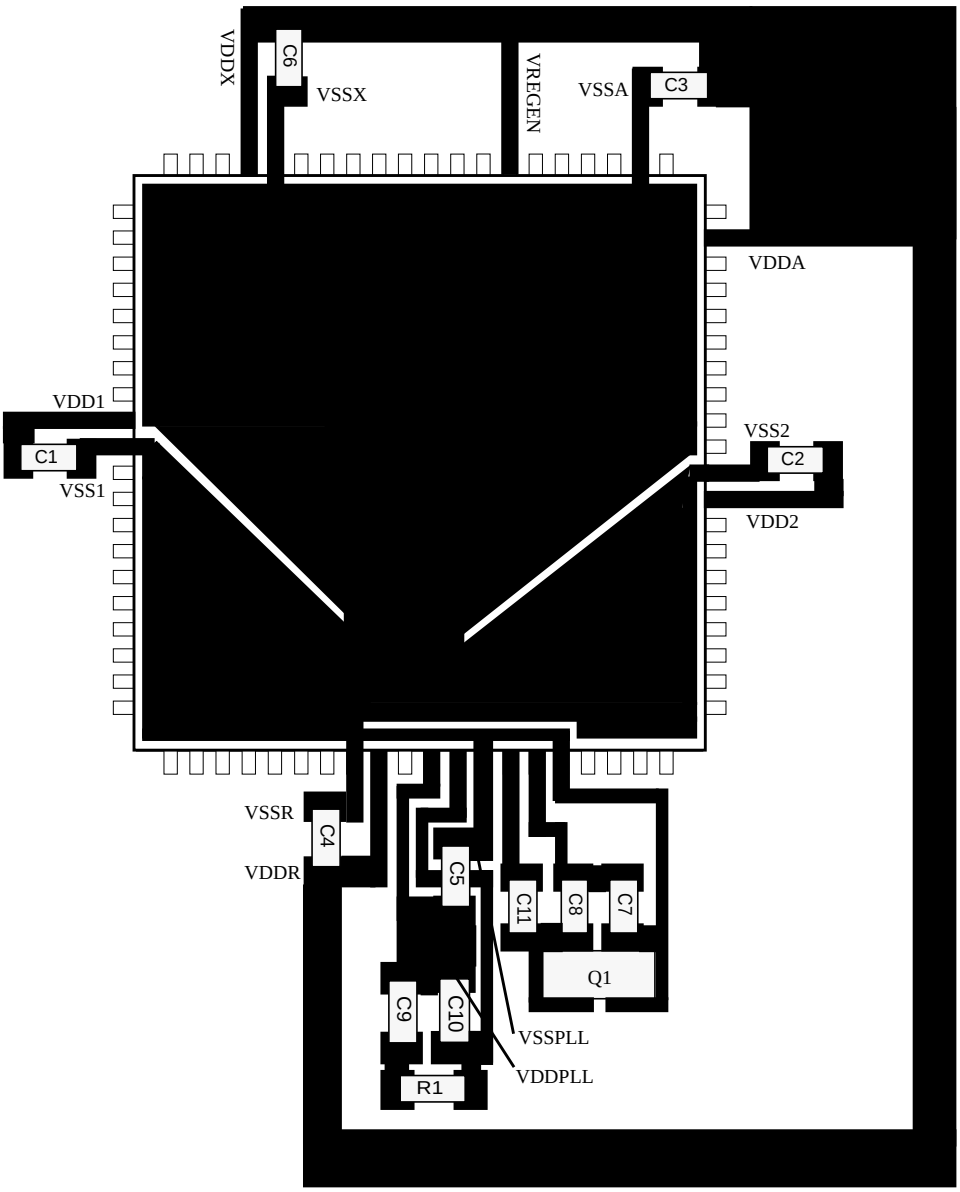


**Figure 22-2 Recommended PCB Layout for 80QFP Colpitts Oscillator**



$T_A$ = Ambient Temperature, [°C]

$P_D$ = Total Chip Power Dissipation, [W]

$\Theta_{JA}$ = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

$P_{INT}$ = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

$P_{IO}$ is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For $R_{DSON}$ is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

$I_{DDR}$ is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

$P_{IO}$ is the sum of all output currents on I/O ports associated with VDDX and VDDR.

# A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

## A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

**Table A-8 ATD Operating Characteristics**

| Conditions are shown in **Table A-4** unless otherwise noted | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | D | Reference Potential<br>Low<br>High | <br>$V_{RL}$<br>$V_{RH}$ | <br>$V_{SSA}$<br>$V_{DDA}/2$ | | <br>$V_{DDA}/2$<br>$V_{DDA}$ | <br>V<br>V |
| 2 | C | Differential Reference Voltage[1] | $V_{RH}$-$V_{RL}$ | 4.50 | 5.00 | 5.25 | V |
| 3 | D | ATD Clock Frequency | $f_{ATDCLK}$ | 0.5 | | 2.0 | MHz |
| 4 | D | ATD 10-Bit Conversion Period<br>Clock Cycles[2]<br>Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$ | <br>$N_{CONV10}$<br>$T_{CONV10}$ | <br>14<br>7 | | <br>28<br>14 | <br>Cycles<br>µs |
| 5 | D | ATD 8-Bit Conversion Period<br>Clock Cycles[2]<br>Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$ | <br>$N_{CONV8}$<br>$T_{CONV8}$ | <br>12<br>6 | | <br>26<br>13 | <br>Cycles<br>µs |
| 6 | D | Recovery Time ($V_{DDA}$=5.0 Volts) | $t_{REC}$ | | | 20 | µs |
| 7 | P | Reference Supply current 2 ATD blocks on | $I_{REF}$ | | | 0.750 | mA |
| 8 | P | Reference Supply current 1 ATD block on | $I_{REF}$ | | | 0.375 | mA |

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

## A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

### A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance $R_S$

## Table A-20 Expanded Bus Timing Characteristics

| Conditions are shown in **Table A-4** unless otherwise noted, $C_{LOAD}$ = 50pF | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 32 | D | NOACC hold time | $t_{NOH}$ | 2 | | | ns |
| 33 | D | IPIPO[1:0] delay time | $t_{P0D}$ | 2 | | 7 | ns |
| 34 | D | IPIPO[1:0] valid time to E rise ($PW_{EL}$–$t_{P0D}$) | $t_{P0V}$ | 11 | | | ns |
| 35 | D | IPIPO[1:0] delay time[1] ($PW_{EH}$-$t_{P1V}$) | $t_{P1D}$ | 2 | | 25 | ns |
| 36 | D | IPIPO[1:0] valid time to E fall | $t_{P1V}$ | 11 | | | ns |

NOTES:

1. Affected by clock stretch: add N x $t_{cyc}$ where N=0,1,2 or 3, depending on the number of clock stretches.

# User Guide End Sheet