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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12a64cpve

- **Ports**
  - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **Table 0-1**).
  - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **Table 0-1**).
  - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DJ64 Block User Guide), if using a derivative without CAN0 (see **Table 0-1**).
- **Pins not available in 80 pin QFP package**
  - **Port H**
    In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).
  - **Port J[1:0]**
    Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+$026C.
  - **Port K**
    Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefor care must be taken not to clear this bit.
  - **Port M[7:6]**
    PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
  - **Port P6**
    PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.
  - **Port S[7:4]**
    PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
  - **PAD[15:8] (ATD1 channels)**
    Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

Document References

The Device User Guide provides information about the MC9S12DJ64 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-2** for names and versions of the referenced documents throughout the Device User Guide.

  - 4K byte RAM
- Two 8-channel Analog-to-Digital Converters
  - 10-bit resolution
  - External conversion trigger capability
- 1M bit per second, CAN 2.0 A, B software compatible module
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Enhanced Capture Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
  - Usable as interrupt inputs
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)
- Byte Data Link Controller (BDLC)
  - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
- Inter-IC Bus (IIC)
  - Compatible with I2C Bus standard
  - Multi-master operation
  - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP or 80 QFP package

$001F - $001F INT map 2 of 2 (HCS12 Interrupt)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $0027 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020 - $0027	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0028 - $002F BKP (HCS12 Breakpoint)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0028	BKPCT0	Read:	BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
		Write:								
$0029	BKPCT1	Read:	BK0MBH	BK0MBL	BK1MBH	BK1MBL	BK0RWE	BK0RW	BK1RWE	BK1RW
		Write:								
$002A	BKP0X	Read:	0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
		Write:								
$002B	BKP0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002C	BKP0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$002D	BKP1X	Read:	0	0	BK1V5	BK1V4	BK1V3	BK1V2	BK1V1	BK1V0
		Write:								
$002E	BKP1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002F	BKP1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0030 - $0031 MMC map 4 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033 MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0033	DDRK	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C2	PWMDTY6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00C3	PWMDTY7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00C4	PWMSDN	Read:	PWMIF	PWMIE	PWMRSTRT	PWMLVL	0	PWM7IN	PWM7INL	PWM7ENA
		Write:								
$00C5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCI0BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00C9	SCI0BDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00CA	SCI0CR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00CB	SCI0CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00CC	SCI0SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCI0SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00CE	SCI0DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCI0DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCI1BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCI1BDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00D2	SCI1CR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00D3	SCI1CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00D4	SCI1SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$024A	DDRS	Read:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
$024B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
$024C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
$024D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
$024E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								
$0253	RDRM	Read:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		Write:								
$0254	PERM	Read:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
$0255	PPSM	Read:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
$0256	WOMM	Read:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
$0257	MODRR	Read:	0	0	0	MODRR4	0	0	MODRR1	MODRR0
		Write:								
$0258	PTP	Read:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$025B	RDRP	Read:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$025C	PERP	Read:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$025D	PPSP	Read:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$025E	PIEP	Read:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		Write:								
$025F	PIFP	Read:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		Write:								
$0260	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0262	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

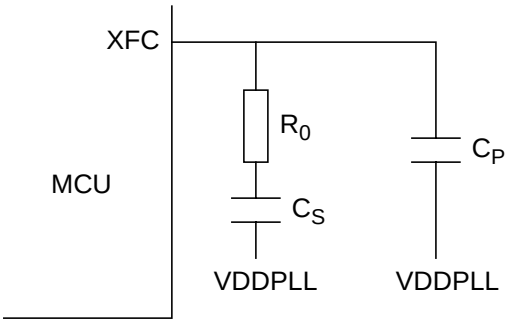


Figure 2-3 PLL Loop Filter Connections

2.3.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the

instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. This pin has a permanently enabled pull-up device.

2.3.7 PAD15 / AN15 / ETRIG1 — Port AD Input Pin of ATD1

PAD15 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

2.3.8 PAD[14:08] / AN[14:08] — Port AD Input Pins ATD1

PAD14 - PAD08 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD1.

2.3.9 PAD07 / AN07 / ETRIG0 — Port AD Input Pin of ATD0

PAD07 is a general purpose input pin and analog input AN0 of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

2.3.10 PAD[06:00] / AN[06:00] — Port AD Input Pins of ATD0

PAD06 - PAD00 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD0.

2.3.11 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.12 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.13 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.
The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.

2.3.46 PP3 / KWP3 / PWM3 — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output.

2.3.47 PP2 / KWP2 / PWM2 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output.

2.3.48 PP1 / KWP1 / PWM1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output.

2.3.49 PP0 / KWP0 / PWM0 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output.

2.3.50 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS6 is a general purpose input or output pin. It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.51 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.52 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.53 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.54 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.3.55 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.56 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.57 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.58 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

2.4 Power Supply Pins

MC9S12DJ64 power and ground pins are described below.

NOTE: *All VSS pins must be connected together in the application.*

Table 2-2 MC9S12DJ64 Power and Ground Connection Summary

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
VDD1, 2	13, 65	2.5V	Internal power and ground generated by internal regulator
VSS1, 2	14, 66	0V	
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

Section 10 Analog to Digital Converter (ATD) Block Description

There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12DJ64. Consult the ATD_10B8C Block User Guide for information about each Analog to Digital Converter module. When the ATD_10B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 11 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 12 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12DJ64 device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 13 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 14 J1850 (BDLC) Block Description

Consult the BDLC Block User Guide for information about the J1850 module.

Section 15 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 16 Flash EEPROM 64K Block Description

Figure 22-1 Recommended PCB Layout 112LQFP Colpitts Oscillator

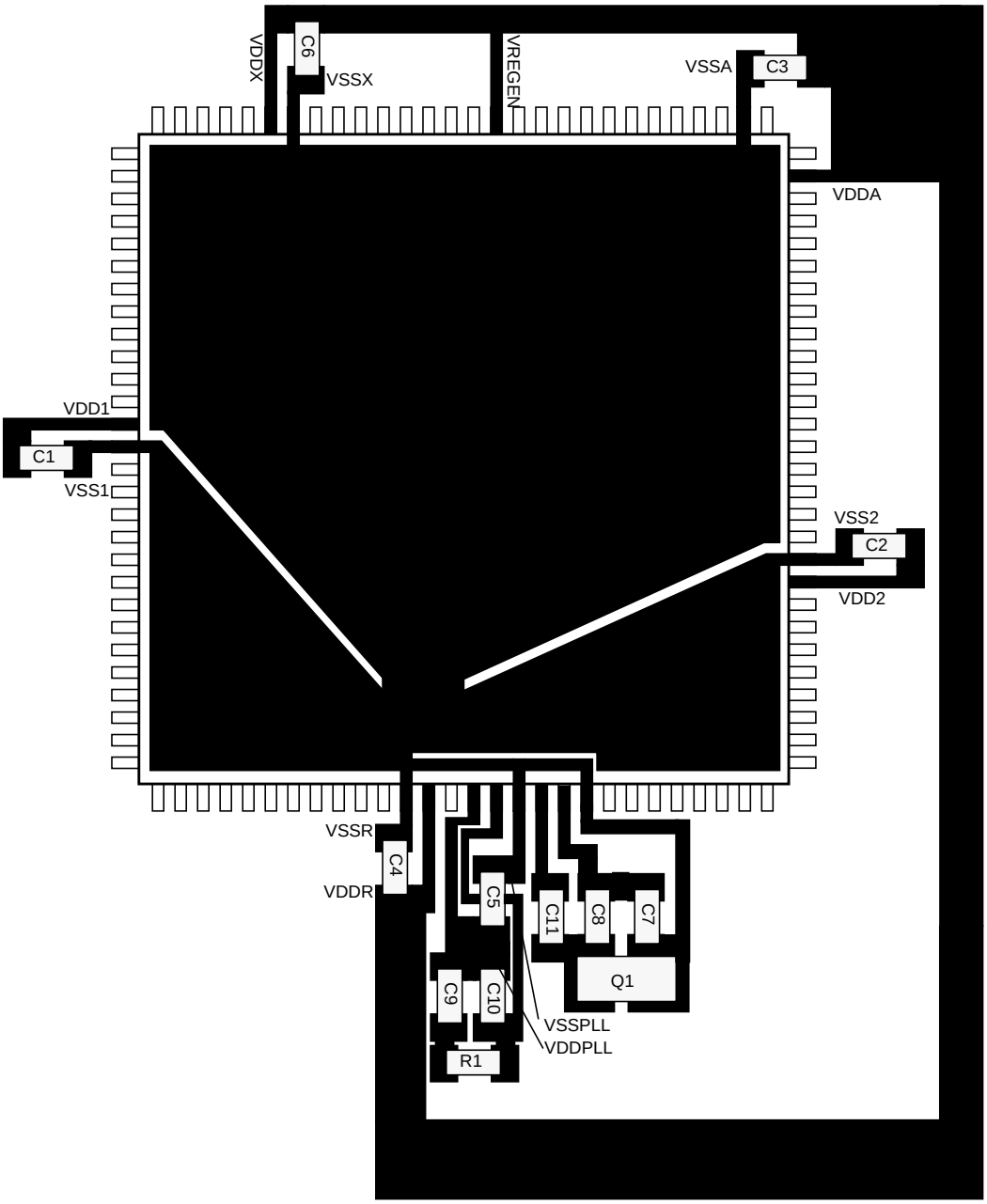
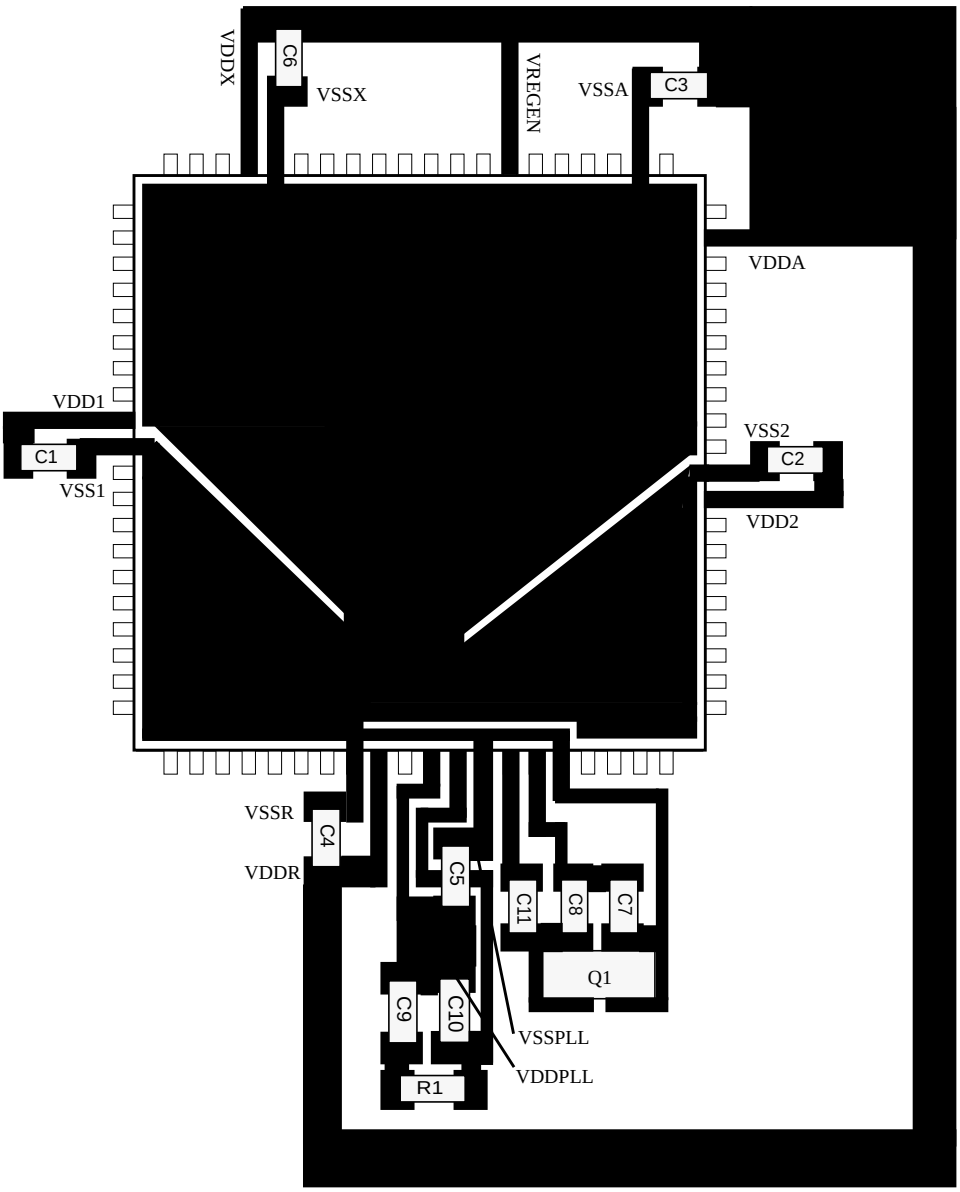


Figure 22-2 Recommended PCB Layout for 80QFP Colpitts Oscillator



A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.0	V
7	Analog Reference	$V_{RH,}$ V_{RL}	-0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [3]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[4]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST [5]	I_{DT}	-0.25	0	mA
13	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. Beyond absolute maximum ratings device might be damaged.
2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.
4. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.
5. This pin is clamped low to V_{SSR}, but not clamped high. This pin must be tied low in applications.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	–	–	31	°C/W
4	T	Junction to Case LQFP112	θ_{JC}	–	–	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	–	–	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	–	–	51	°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	–	–	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	–	–	27	°C/W
9	T	Junction to Case QFP80	θ_{JC}	–	–	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	–	–	3	°C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}-V_{RL}	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=5.0 Volts)	t_{REC}			20	µs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

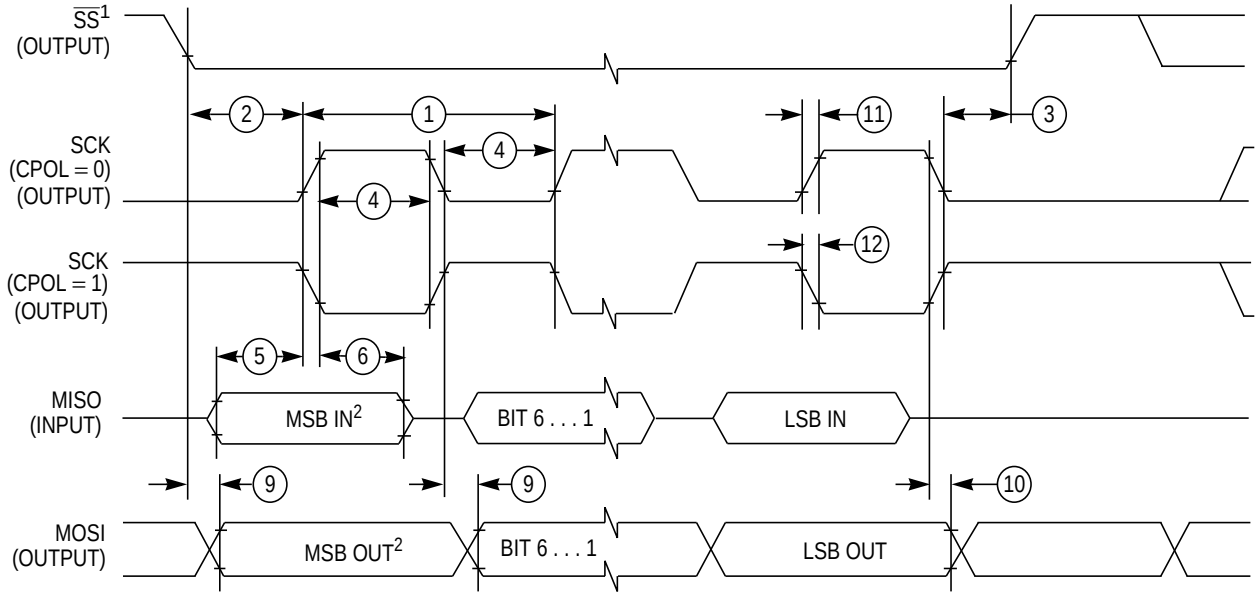
Table A-9 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input Source Resistance	R_S	-	-	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

A.7 SPI

A.7.1 Master Mode

Figure A-5 and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-18**.



1. If configured as output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-5 SPI Master Timing (CPHA = 0)