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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I <sup>2</sup> C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12d64cfue

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Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.15	22 July 2003	22 July 2003		Mentioned "S12 LRAE" bootloader in Flash section Section Document References: corrected S12 CPU document reference
V01.16	24 Feb. 2004	24 Feb. 2004		Added 3L86D maskset with corresponding Part ID Table Oscillator Characteristics: Added more details for EXTAL pin
V01.17	21 May 2004	21 May 2004		Added 4L86D maskset with corresponding Part ID Table "MC9S12DJ64 Memory Map out of Reset": corrected \$1000 - \$3fff memory in single chip modes to "unimplemented".
V01.18	13 July 2004	13 July 2004		Added MC9S12D32 and MC9S12A32
V01.19	2 Sept. 2004	2 Sept. 2004		Appendix, Table "Oscillator Characteristics": changed item 13 VIH,EXTAL min value from 0.7*VDDPLL to 0.75*VDDPLL item 14 VIL,EXTAL max value from 0.3*VDDPLL to 0.25*VDDPLL
V01.20	6 April 2005	6 April 2005		Table "Assigned Part ID Numbers": added mask set number0M89CTable "NVM Reliability Characteristics": added footnote concerningdata retention

# **List of Tables**

Table 0-1 D	Derivati	ve Differences	15
Table 0-2 D	Docume	ent References	17
Table 1-1 D	Device	Memory Map for MC9S12DJ64	25
Table 1-2 D	Device	Memory Map for MC9S12D32	28
\$0000 - \$0	000F	MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)	30
\$0010 - \$0	0014	MMC map 1 of 4 (HCS12 Module Mapping Control)	30
\$0015 - \$0	0016	INT map 1 of 2 (HCS12 Interrupt)	31
\$0017 - \$0	0019	Reserved	31
\$001A - \$	001B	Device ID Register (Table 1-4)	31
\$001C - \$	001D	MMC map 3 of 4 (HCS12 Module Mapping Control, Table 1-5)	31
\$001E - \$	001E	MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)	31
\$001F - \$0	001F	INT map 2 of 2 (HCS12 Interrupt)	32
\$0020 - \$0	0027	Reserved	32
\$0028 - \$0	002F	BKP (HCS12 Breakpoint)	32
\$0030 - \$0	0031	MMC map 4 of 4 (HCS12 Module Mapping Control)	32
\$0032 - \$0	0033	MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)	32
\$0034 - \$0	003F	CRG (Clock and Reset Generator)	33
\$0040 - \$0	007F	ECT (Enhanced Capture Timer 16 Bit 8 Channels)	33
\$0080 - \$0	009F	ATD0 (Analog to Digital Converter 10 Bit 8 Channel)	36
\$00A0 - \$	00C7	PWM (Pulse Width Modulator 8 Bit 8 Channel)	37
\$00C8 - \$	00CF	SCI0 (Asynchronous Serial Interface)	39
\$00D0 - \$	00D7	SCI1 (Asynchronous Serial Interface)	39
\$00D8 - \$	00DF	SPI0 (Serial Peripheral Interface)	40
\$00E0 - \$	00E7	IIC (Inter IC Bus)	40
\$00E8 - \$	00EF	BDLC (Bytelevel Data Link Controller J1850)	41
\$00F0 - \$0	00FF	Reserved	41
\$0100 - \$0	010F	Flash Control Register (fts64k)	41
\$0110 - \$0	011B	EEPROM Control Register (eets1k)	42
\$011C - \$	011F	Reserved for RAM Control Register	42
\$0120 - \$0	013F	ATD1 (Analog to Digital Converter 10 Bit 8 Channel)	43
\$0140 - \$0	017F	CAN0 (Freescale Scalable CAN - FSCAN)	44
Table 1-3 D	Detailed	SCAN Foreground Receive and Transmit Buffer Layout	45
\$0180 - \$0	023F	Reserved	46

\$0240 -	\$027F PIM (Port Integration Module)	46
\$0280 -	\$03FF Reserved	48
Table 1-4	Assigned Part ID Numbers	
Table 1-5	Memory size registers	
Table 2-1	Signal Properties	54
Table 2-2	MC9S12DJ64 Power and Ground Connection Summary	64
Table 4-1	Mode Selection	69
Table 4-2	Clock Selection Based on PE7	69
Table 4-3	Voltage Regulator VREGEN	70
Table 5-1	Interrupt Vector Locations	73
Table 22-1	Suggested External Component Values	81
Table A-1	Absolute Maximum Ratings	89
Table A-2	ESD and Latch-up Test Conditions	90
Table A-3	ESD and Latch-Up Protection Characteristics	90
Table A-4	Operating Conditions	91
Table A-5	Thermal Package Characteristics	93
Table A-6	5V I/O Characteristics	94
Table A-7	Supply Current Characteristics	95
Table A-8	ATD Operating Characteristics	97
Table A-9	ATD Electrical Characteristics	98
Table A-10	ATD Conversion Performance	99
Table A-11	NVM Timing Characteristics	102
Table A-12	NVM Reliability Characteristics	103
Table A-13	Voltage Regulator Recommended Load Capacitances	105
Table A-14	Startup Characteristics	107
Table A-15	Oscillator Characteristics	108
Table A-16	PLL Characteristics	112
Table A-17	MSCAN Wake-up Pulse Characteristics	113
Table A-18	SPI Master Mode Timing Characteristics	116
Table A-19	SPI Slave Mode Timing Characteristics	118
Table A-20	Expanded Bus Timing Characteristics	121

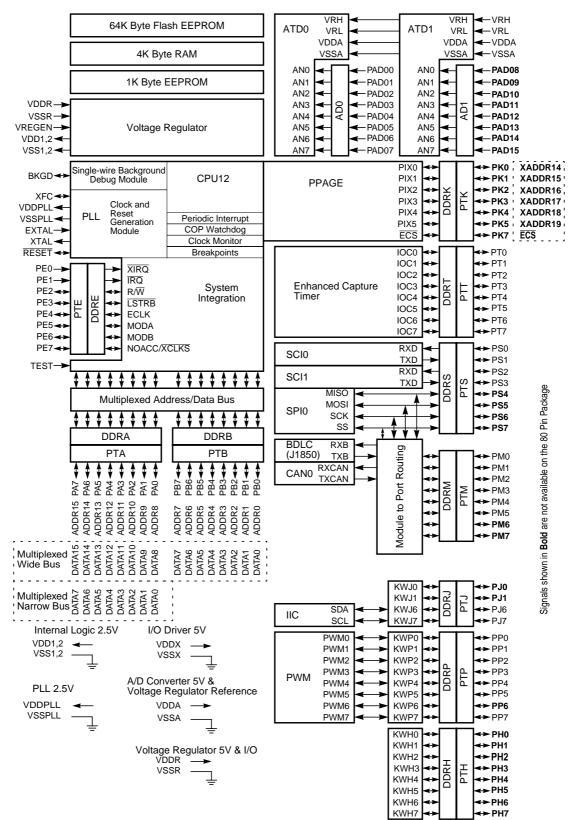


MC9S12DJ64 Device User Guide — V01.20

# 1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DJ64 device.





#### Figure 1-1 MC9S12DJ64 Block Diagram

Address	Module	Size (Bytes)
\$C000 - \$FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at \$FF80 - \$FFFF	16384

\$001F - \$001F

Address \$001F

#### INT map 2 of 2 (HCS12 Interrupt)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HPRIO Rea Wri	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0

#### \$0020 - \$0027

#### Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0020 -	Reserved	Read:	0	0	0	0	0	0	0	0
\$0027	Reserveu	Write:								

#### \$0028 - \$002F

#### **BKP (HCS12 Breakpoint)**

A	N		D:+ 7	D:1-0	Dite	D:4 4	D:+ 0	D:+ 0	D:14	D:1 0
Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0028	BKPCT0	Read:	BKEN BKFULL	BKBDM	BKTAG	0	0	0	0	
<b>Φ</b> 0020	BRECIU	Write:	DREN	DRFULL	DKDDIVI	DRIAG				
\$0029	BKPCT1	Read:	вкомвн	BKOMBL	BK1MBH	BK1MBL	<b>BKORWE</b>	<b>BK0RW</b>	BK1RWE	BK1RW
φ0029	DRECTI	Write:	DRUNDIT	DRUNDL			DRURWE	BRURW	DRINVE	DRINW
\$002A	BKP0X	Read:	0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
ψυυΖΑ	DILLON	Write:					DRUVS	BRUVZ	BRUVI	
\$002B	BKP0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:	Dit 15	14	15					
\$002C	BKP0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
φ002C	DRFUL	Write:		0						BIL U
\$002D	BKP1X	Read:	0	0	BK1V5	BK1V4	BK1V3	BK1V2	BK1V1	BK1V0
9002D	DREIX	Write:			BRIVS	DR1V4	DKTV5	DRTVZ	DRIVI	DRIVU
\$002E	BKP1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
φ002E		Write:	DILTO	14	13	12		10	9	DILO
\$002F	BKP1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
φυυ2Γ	DRPIL	Write:		0	5	4	3	2		DILU

#### \$0030 - \$0031

#### MMC map 4 of 4 (HCS12 Module Mapping Control)

Address	Name	]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0030 PPAG	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
	PPAGE	Write:								
\$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

#### \$0032 - \$0033

#### MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name	[	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0032	PORTK	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0033	DDRK	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

#### \$0034 - \$003F

### CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
<b>\$000</b>	onnit	Write:						01112		01110
\$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
φυυυυ		Write:								_
\$0036	CTFLG	Read:	0	0	0	0	0	0	0	0
φυσσυ	TEST ONLY	Write:								
\$0037	CRGFLG	Read:	RTIF	PORF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM
<b>Q</b> 0001		Write:				2001				
\$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0
	oncontri	Write:								
\$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:								
\$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		Write:								
\$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:			-		-			
\$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:			-	-				
\$003D	FORBYP	Read:	0	0	0	0	0	0	0	0
	TEST ONLY	Write:								
\$003E	CTCTL	Read:	0	0	0	0	0	0	0	0
ΨυυσΕ	TEST ONLY	Write:								
\$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
φυυσι		Write:	Bit 7	6	5	4	3	2	1	Bit 0

#### \$0040 - \$007F

### ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0040	TIOS	Read: Write:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
\$0041	CFORC	Read:	0	0	0	0	0	0	0	0
φ00 <del>4</del> Ι	CFORC	Write:	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
\$0042	OC7M	Read: Write:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
\$0043	OC7D	Read: Write:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
\$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
φ00 <del>44</del>		Write:								
\$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
ψ00 <del>-</del> 0		Write:								
\$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
φυυτυ	reenti	Write:		10000	TOTINE	1110/				
\$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
<b>ÇUU</b>		Write:								
\$0048	TCTL1	Read: Write:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
\$0049	TCTL2	Read: Write:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0

### **\$00E8 - \$00EF** BDLC (Bytelevel Data Link Controller J1850)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00E8	DLCBCR1	Read:	IMSG	CLKS	0	0	0	0	IE	WCM
<b>QUOLO</b>	DEODOIN	Write:	INICO	OLINO						Wolf
\$00E9	DLCBSVR	Read:	0	0	13	12	l1	10	0	0
φ00L9	DLODSVI	Write:								
\$00EA	DLCBCR2	Read:	SMRST	DLOOP	RX4XE	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
<b>JUULA</b>	DLODGRZ	Write:	51011151	DLOOI	N/4/L	NDI 5	ILOD			
\$00EB	DLCBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
φ00EB	DLCBDK	Write:	וט	DO	D5	D4	03	DZ		DU
\$00EC	DLCBARD	Read:	0	RXPOL	0	0	BO3	BO2	BO1	BO0
φ00EC	DLCBARD	Write:		NAFUL			B03	602	BOT	воо
\$00ED	DLCBRSR	Read:	0	0	R5	R4	R3	R2	R1	R0
ΦΟΟΕΡ	DLCDRSR	Write:			КЭ	Κ4	кэ	RΖ	K I	RU
¢oorr	DLCSCR	Read:	0	0	0		0	0	0	0
\$00EE	DLCSCK	Write:				BDLCE				
\$00EF	DLCBSTAT	Read:	0	0	0	0	0	0	0	IDLE
φυυ≝F	DLCDSTAI	Write:								

#### \$00F0 - \$00FF

#### Reserved

Address	Name	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00F0 -	Reserved	Read:	0	0	0	0	0	0	0	0
\$00FF	Reserveu	Write:								

#### \$0100 - \$010F

### Flash Control Register (fts64k)

			·i							
Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0100	FCLKDIV	Read: Write:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
¢0101	FSEC	Read:	KEYEN	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
\$0101	FSEC	Write:								
\$0102	Reserved	Read:	0	0	0	0	0	0	0	0
\$010Z	Reserved	Write:								
\$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
φ0103	FUNEG	Write:	OBEIE	COLE	KE IACC					
\$0104	FPROT	Read: Write:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
\$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
φ0105	FSTAI	Write:	CDEIF		FVIOL	ACCERR		DLAINN		
\$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
φ0100	FCIND	Write:		CIVIDBO	CIVIDBS			CIVIDBZ		CIVIDBO
\$0107	Reserved	Read:	0	0	0	0	0	0	0	0
ψ010 <i>1</i>	iteseiveu	Write:								
\$0108	FADDRHI	Read:	Bit 14	Bit 14	13	12	11	10	9	Bit 8
ψυτυυ	TADDRIII	Write:	DICIT	DICIT	10	12		10	3	Dit O
\$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
ψυτυυ	I NEEKLO	Write:		U	0	т	0	۷	I	

\$0100 - \$010F

Address \$010A

\$010B

\$010C -

\$010F

#### Flash Control Register (fts64k)

Name	[	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDATAHI	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
FDATALO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reserved	Read:	0	0	0	0	0	0	0	0
Reserveu	Write:								

#### \$0110 - \$011B

### **EEPROM Control Register (eets1k)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
<b>QUITO</b>	LOLINDIV	Write:		TREIVO	LBIVO	LDIVI	LDIVO	LDIVZ	LDIVI	EBIVO
\$0111	Reserved	Read:	0	0	0	0	0	0	0	0
φυττι	Reserved	Write:								
\$0112	Reserved	Read:	0	0	0	0	0	0	0	0
φυτιζ	Reserveu	Write:								
\$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
φυτισ	LONEG	Write:	OBEIE	COLE						
¢0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
\$0114	EFROI	Write:	EFOFEN				EFDIS		EFI	EFU
\$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
φυτισ	ESTAI	Write:	ODEIF		FVIOL	ACCERN		DLAINN		
\$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
φυτιο	ECIMID	Write:		CIVIDBO	CIVIDBS			CIVIDBZ		CIVIDBO
\$0117	Reserved for	Read:	0	0	0	0	0	0	0	0
φυτιγ	Factory Test	Write:								
<b>©0440</b>		Read:	0	0	0	0	0	0	0	D:4 0
\$0118	EADDRHI	Write:								Bit 8
¢0440		Read:		0	F	4	0	0	4	
\$0119	EADDRLO	Write:	Bit 7	6	5	4	3	2	1	Bit 0
<b>©</b> 044A		Read:		4.4	40	40		10	0	D:4 0
\$011A	EDATAHI	Write:	Bit 15	14	13	12	11	10	9	Bit 8
¢011P		Read:	Dit 7	6	F	Λ	2	2	1	Dit 0
\$011B	EDATALO	Write:	Bit 7	6	5	4	3	2	1	Bit 0

#### \$011C - \$011F

### **Reserved for RAM Control Register**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$011C -	Reserved	Read:	0	0	0	0	0	0	0	0
\$011F	Reserveu	Write:								

### \$0240 - \$027F

### **PIM (Port Integration Module)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0263	RDRH	Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
\$0264	PERH	Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
\$0265	PPSH	Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
\$0266	PIEH	Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
\$0267	PIFH	Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
\$0268	PTJ	Read: Write:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
\$0269	PTIJ	Read:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
<i><b>Q0200</b></i>	1 110	Write:								
\$026A	DDRJ	Read: Write:	DDRJ7	DDRJ7	0	0	0	0	DDRJ1	DDRJ0
\$026B	RDRJ	Read: Write:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
\$026C	PERJ	Read: Write:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
\$026D	PPSJ	Read: Write:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
\$026E	PIEJ	Read:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
ΨULUL	1120	Write:		11200						
\$026F	PIFJ	Read: Write:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
\$0270 -	Reserved	Read:	0	0	0	0	0	0	0	0
\$027F	176961 460	Write:								

#### \$0280 - \$03FF

#### Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0280 -	Pagaruad	Read:	0	0	0	0	0	0	0	0
\$03FF	Reserved	Write:								

instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of  $\overline{\text{RESET}}$ . This pin has a permanently enabled pull-up device.

# 2.3.7 PAD15 / AN15 / ETRIG1 — Port AD Input Pin of ATD1

PAD15 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

# 2.3.8 PAD[14:08] / AN[14:08] - Port AD Input Pins ATD1

PAD14 - PAD08 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD1.

# 2.3.9 PAD07 / AN07 / ETRIG0 — Port AD Input Pin of ATD0

PAD07 is a general purpose input pin and analog input AN0 of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

# 2.3.10 PAD[06:00] / AN[06:00] — Port AD Input Pins of ATD0

PAD06 - PAD00 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD0.

# 2.3.11 PA[7:0] / ADDR[15:8] / DATA[15:8] - Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

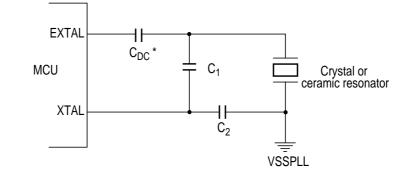
# 2.3.12 PB[7:0] / ADDR[7:0] / DATA[7:0] - Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

# 2.3.13 PE7 / NOACC / XCLKS — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or "free" cycle. This signal will assert when the CPU is not using the bus.

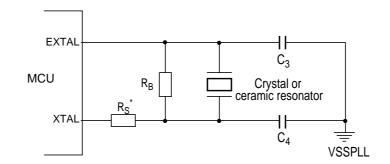
The  $\overline{\text{XCLKS}}$  is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of  $\overline{\text{RESET}}$ . If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.



\* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal

Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value  $C_{DC}$ .

### Figure 2-4 Colpitts Oscillator Connections (PE7=1)



\* Rs can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-5 Pierce Oscillator Connections (PE7=0)

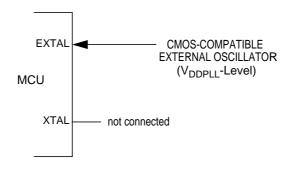


Figure 2-6 External Clock Connections (PE7=0)

### 4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

### 4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode or via a sequence of BDM commands. Unsecuring is also possible via the Backdoor Key Access. Refer to Flash Block Guide for details.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

# 4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

### 4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

## 4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

### 4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and data bus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

**NOTE:** Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature  $T_A$  and the junction temperature  $T_J$ . For power dissipation calculations refer to Section A.1.8 Power Dissipation and Thermal Characteristics.

Rating	Symbol	Min	Тур	Max	Unit
I/O, Regulator and Analog Supply Voltage	V <sub>DD5</sub>	4.5	5	5.25	V
Digital Logic Supply Voltage <sup>1</sup>	V <sub>DD</sub>	2.35	2.5	2.75	V
PLL Supply Voltage <sup>1</sup>	V <sub>DDPLL</sub>	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	$\Delta_{VDDX}$	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	$\Delta_{VSSX}$	-0.1	0	0.1	V
Oscillator	f <sub>osc</sub>	0.5	-	16	MHz
Bus Frequency	f <sub>bus</sub>	0.25 <sup>2</sup>	-	25	MHz
MC9S12DJ64 <b>C</b>					
Operating Junction Temperature Range	Т <sub>Ј</sub>	-40	-	100	°C
Operating Ambient Temperature Range <sup>3</sup>	T <sub>A</sub>	-40	27	85	°C
MC9S12DJ64V					
Operating Junction Temperature Range	Т <sub>Ј</sub>	-40	-	120	°C
Operating Ambient Temperature Range <sup>3</sup>	T <sub>A</sub>	-40	27	105	°C
MC9S12DJ64 <b>M</b>					
Operating Junction Temperature Range	Т <sub>Ј</sub>	-40	-	140	°C
Operating Ambient Temperature Range <sup>3</sup>	T <sub>A</sub>	-40	27	125	°C

#### Table A-4 Operating Conditions

NOTES:

1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.

2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.

3. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T<sub>A</sub> and device junction temperature T<sub>J</sub>.

## A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature  $(T_J)$  in °C can be obtained from:

$$\mathsf{T}_{\mathsf{J}} = \mathsf{T}_{\mathsf{A}} + (\mathsf{P}_{\mathsf{D}} \bullet \Theta_{\mathsf{J}} \mathsf{A})$$

 $T_{I}$  = Junction Temperature, [°C]

NOTES:

1. PLL off 2. At those low power dissipation levels  $T_J = T_A$  can be assumed

#### MC9S12DJ64 Device User Guide — V01.20

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

#### A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage  $\leq 1LSB$ , then the external filter capacitor,  $C_f \geq 1024 * (C_{INS}-C_{INN})$ .

#### A.2.2.3 Current Injection

There are two cases to consider.

- 1. A current is injected into the channel being converted. The channel being stressed has conversion values of 3FF (FF in 8-bit mode) for analog inputs greater than  $V_{RH}$  and 000 for values less than  $V_{RL}$  unless the current is higher than specified as disruptive condition.
- 2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as  $V_{ERR} = K * R_S * I_{INJ}$ , with  $I_{INJ}$  being the sum of the currents injected into the two pins adjacent to the converted channel.

Condit	Conditions are shown in Table A-4 unless otherwise noted											
Num	С	Rating	Symbol	Min	Тур	Max	Unit					
1	С	Max input Source Resistance	R <sub>S</sub>	-	-	1	KΩ					
2	т	Total Input Capacitance Non Sampling Sampling	C <sub>INN</sub> C <sub>INS</sub>			10 22	pF					
3	С	Disruptive Analog Input Current	I <sub>NA</sub>	-2.5		2.5	mA					
4	С	Coupling Ratio positive current injection	К <sub>р</sub>			10 <sup>-4</sup>	A/A					
5	С	Coupling Ratio negative current injection	K <sub>n</sub>			10 <sup>-2</sup>	A/A					

### **Table A-9 ATD Electrical Characteristics**



