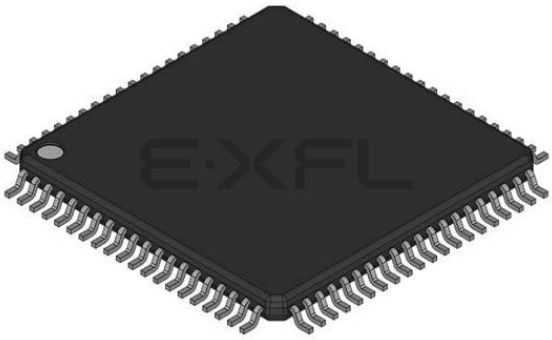

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12d64cfuer

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.06	20 Aug. 2002	20 Aug. 2002		NVM electricals updated Subsection "Detailed Register Map: Address corrections Preface, Table "Document references": added OSC User Guide New section "Oscillator (OSC) Block Description"
V01.07	20 Sept. 2002	20 Sept. 2002		Electrical Characteristics: -> Section "General": removed preliminary disclaimer ->Table "Supply Current Characteristics": changed max Run IDD from 65mA to 50mA changes max Wait IDD from 40mA to 30mA changed max Stop IDD from 50uA to 100uA Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock
V01.08	25 Sept. 2002	25 Sept. 2002		Table "5V I/O Characteristics": Corrected Input Leakage Current to +/- 1 uA Section "Part ID assignment": Located on start of next page for better readability
V01.09	10 Oct. 2002	10 Oct. 2002		Added MC9S12A64 derivative to cover sheet and "Derivative Differences" Table Corrected in footnote of Table "PLL Characteristics": f_{OSC} = 4MHz
V01.10	8 Nov. 2002	8 Nov. 2002		Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0 and/or BDLC Table "ESD and Latch-up Test Conditions": changed pulse numbers from 3 to 1 Table "ESD and Latch-Up Protection Characteristics": changed parameter classification from C to T Table "5V I/O Characteristics": removed foot note from "Input Leakage Current" Table " Supply Current Characteristics": updated Stop and Pseudo Stop currents
V01.11	24 Jan. 2003	24 Jan. 2003		Subsection "Detailed Register Map": Corrected several entries Subsection "Unsecuring the Microcontroller": Added more details Table "Operating Conditions": improved footnote 1 wording, applied footnote 1 to PLL Supply Voltage.
V01.12	31 Mar. 2003	31 Mar. 2003		Tables "SPI Master/Slave Mode Timing Characteristics: Corrected Operating Frequency Appendix 'NVM, Flash and EEPROM': Replaced 'burst programming' by 'row programming Table "Operating Conditions": corrected minimum bus frequency to 0.25MHz Section "Feature List": ECT features changed to "Four pulse accumulators ..."
V01.13	20 May 2003	20 May 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides Table "Signal Properties" corrected pull resistor reset state for PE7 and PE4-PE2. Table "Absolute Maximum Ratings" corrected footnote on clamp of TEST pin.
V01.14	10 June 2003	10 June 2003		Added cycle definition to "CPU 12 Block Description". Added register reset values to MMC and MEBI block descriptions. Diagram "Clock Connections": Connect Bus Clock to HCS12 Core

Section 3 System Clock Description

Section 4 Modes of Operation

Section 5 Resets and Interrupts

Section 6 HCS12 Core Block Description

Derivative Differences and Document References

Derivative Differences

Table 0-1 shows the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Derivative Differences

Generic device	MC9S12DJ64	MC9S12D64	MC9S12A64	MC9S12D32	MC9S12A32
CAN0	1	1	0	1	0
J1850/BDLC	1	0	0	0	0
Packages	112LQFP, 80QFP	112LQFP, 80QFP	112LQFP, 80QFP	80QFP	80QFP
Mask Set	L86D	L86D	L86D	L86D	L86D
Temp Options	M, V, C	M, V, C	C	M, V, C	C
Package Codes	PV, FU	PV, FU	PV, FU	FU	FU
Note	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office

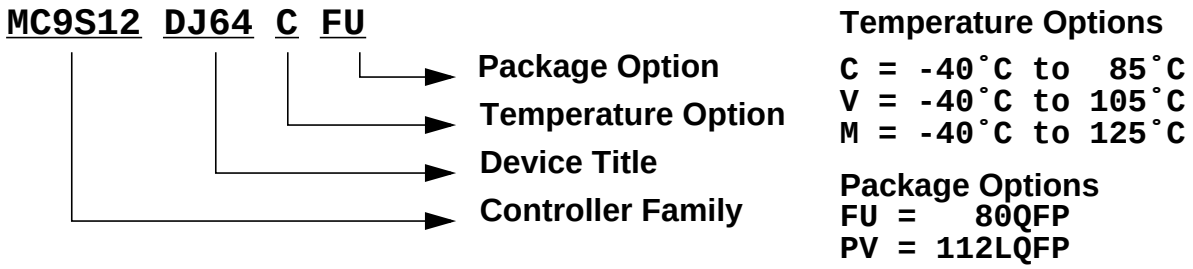


Figure 0-1 Order Partnumber Example

The following items should be considered when using a derivative.

- **Registers**
  - Do not write or read CAN0 registers (after reset: address range $0140 - $017F), if using a derivative without CAN0 (see **Table 0-1**).
  - Do not write or read BDLC registers (after reset: address range $00E8 - $00EF), if using a derivative without BDLC (see **Table 0-1**).
- **Interrupts**
  - Fill the four CAN0 interrupt vectors ($FFB0 - $FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0 (see **Table 0-1**).
  - Fill the BDLC interrupt vector ($FFC2, $FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **Table 0-1**).

Table 1-1 Device Memory Map for MC9S12DJ64

Address	Module	Size (Bytes)
$C000 - $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 - $FFFF	16384

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0063	PACN2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0064	PACN1 (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0065	PACN0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0066	MCCTL	Read:	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
		Write:				ICLAT	FLMC			
$0067	MCFLG	Read:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
		Write:								
$0068	ICPAR	Read:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Write:								
$0069	DLYCT	Read:	0	0	0	0	0	0	DLY1	DLY0
		Write:								
$006A	ICOVW	Read:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Write:								
$006B	ICSYS	Read:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
		Write:								
$006C	Reserved	Read:								
		Write:								
$006D	TIMTST Test Only	Read:	0	0	0	0	0	0	TCBYP	0
		Write:								
$006E	Reserved	Read:								
		Write:								
$006F	Reserved	Read:								
		Write:								
$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$007C	TC2H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATD0CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATD0CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATD0CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATD0CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATD0CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATD0CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0086	ATD0STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATD0TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATD0TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008B	ATD0STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008D	ATD0DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$008E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$008F	PORTAD0	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$0090	ATD0DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATD0DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0092	ATD0DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATD0DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATD0DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATD0DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATD0DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATD0DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATD0DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATD0DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATD0DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATD0DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATD0DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATD0DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATD0DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATD0DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A0	PWME	Read:	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$00A1	PWMPOL	Read:	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$00A2	PWMCLK	Read:	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$00A3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$00A4	PWMCAE	Read:	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$00A5	PWMCTL	Read:	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$00A6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A7	PWMPRSC Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A8	PWMSCLA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	ATD1CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0121	ATD1CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0122	ATD1CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0123	ATD1CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0124	ATD1CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0125	ATD1CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0126	ATD1STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0127	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0128	ATD1TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0129	ATD1TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$012A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012B	ATD1STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$012C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012D	ATD1DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$012E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012F	PORTAD1	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$0130	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0131	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0132	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0133	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0134	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0135	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0136	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0137	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0138	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

Table 2-1 Signal Properties

Pin Name Function1	Pin Name Function2	Pin Name Function3	Pin Name Function4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	None	None	Oscillator Pins
XTAL	—	—	—				
$\overline{\text{RESET}}$	—	—	—	VDDR			External Reset
TEST	—	—	—	N.A.			Test Input
VREGEN	—	—	—	VDDX			Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL			PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD15	**AN15**	**ETRIG1**	**—**	VDDA	None	None	**Port AD Input, Analog Input AN7 of ATD1, External Trigger Input of ATD1**
PAD[14:08]	**AN[14:08]**	**—**	**—**				**Port AD Inputs, Analog Inputs AN[6:0] of ATD1**
PAD07	AN07	ETRIG0	—				Port AD Input, Analog Input AN7 of ATD0, External Trigger Input of ATD0
PAD[06:00]	AN[06:00]	—	—				Port AD Inputs, Analog Inputs AN[6:0] of ATD0
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	PUCR/ PUPAE	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—		PUCR/ PUPBE		Port B I/O, Multiplexed Address/Data
PE7	NOACC	$\overline{\text{XCLKS}}$	—		PUCR/ PUPEE	Mode depen-dant[1]	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—		While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—				Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—		PUCR/ PUPEE	Mode depen-dant[1]	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—				Port E I/O, Byte Strobe, Tag Low
PE2	R/$\overline{\text{W}}$	—	—				Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—			Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—				Port E Input, Non Maskable Interrupt
PH7	**KWH7**	—	—		PERH/ PPSH	Disabled	**Port H I/O, Interrupt**
PH6	**KWH6**	—	—				**Port H I/O, Interrupt**
PH5	**KWH5**	—	—				**Port H I/O, Interrupt**
PH4	**KWH4**	—	—				**Port H I/O, Interrupt**
PH3	**KWH3**	—	—				**Port H I/O, Interrupt**
PH2	**KWH2**	—	—				**Port H I/O, Interrupt**
PH1	**KWH1**	—	—				**Port H I/O, Interrupt**
PH0	**KWH0**	—	—				**Port H I/O, Interrupt**

Mnemonic	Pin Number 112-pin QFP	Nominal Voltage	Description
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5.0V	Internal Voltage Regulator enable/disable

2.4.1 VDDX, VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDX and VSSX are the supplies for Ports J, K, M, P, T and S.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDR and VSSR are the supplies for Ports A, B, E and H.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: *No load allowed except for bypass capacitors.*

2.4.4 VDDA, VSSA — Power Supply Pins for ATD0/ATD1 and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the two analog to digital converters. It also provides the reference for the internal voltage regulator. This allows the supply voltage to ATD0/ATD1 and the reference voltage to be bypassed independently.

Section 6 HCS12 Core Block Description

6.1 CPU12 Block Description

Consult the CPU12 Reference Manual for information on the CPU.

6.1.1 Device-specific information

When the CPU12 Reference Manual refers to *cycles* this is equivalent to *Bus Clock periods*.
So *1 cycle* is equivalent to *1 Bus Clock period*.

6.2 HCS12 Module Mapping Control (MMC) Block Description

Consult the MMC Block Guide for information on the HCS12 Module Mapping Control module.

6.2.1 Device-specific information

- INITEE
  - Reset state: $01
  - Bits EE11-EE15 are "Write once in Normal and Emulation modes and write anytime in Special modes".
- PPAGE
  - Reset state: $00
  - Register is "Write anytime in all modes"
- MEMSIZ0
  - Reset state: $11
- MEMSIZ1
  - Reset state: $80

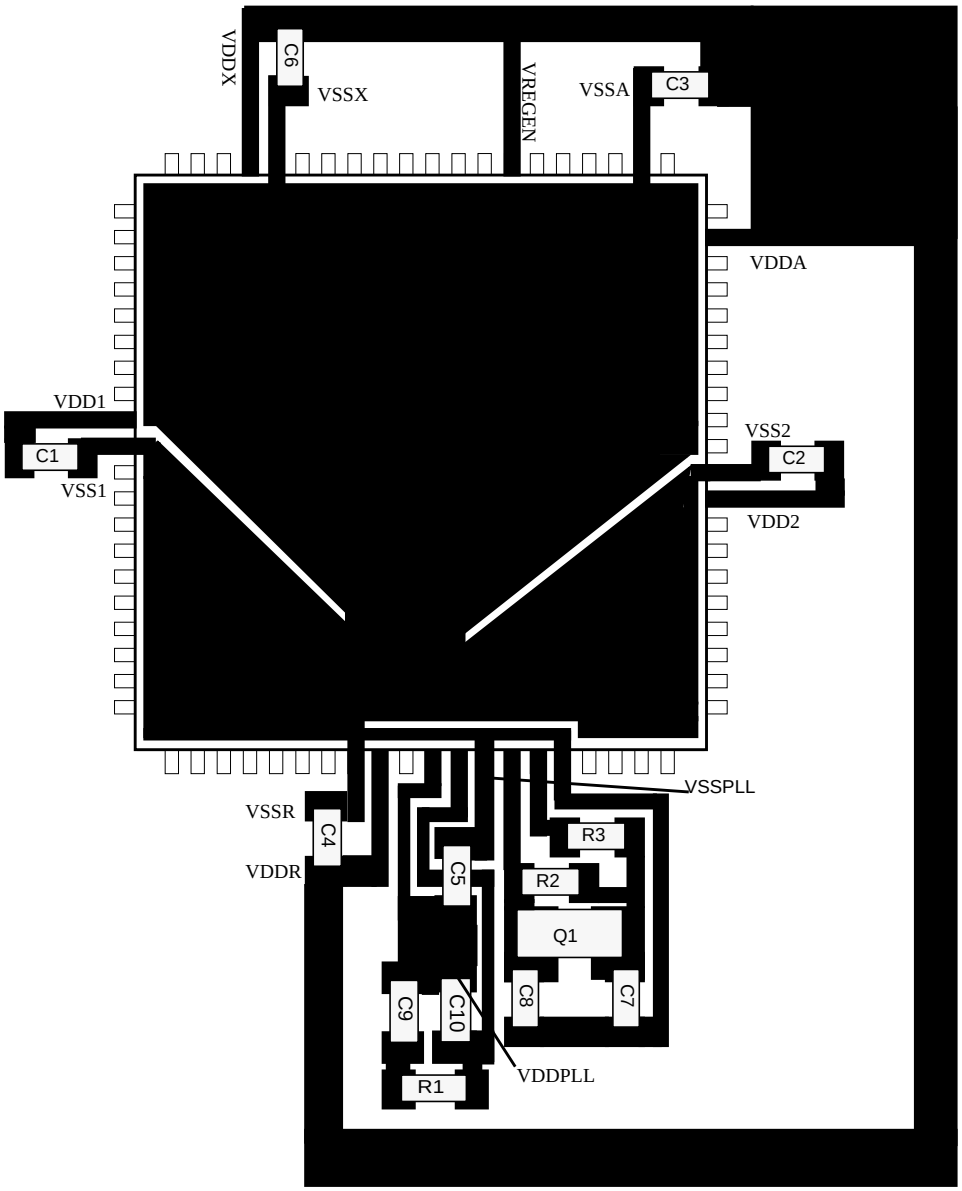
6.3 HCS12 Multiplexed External Bus Interface (MEBI) Block Description

Consult the MEBI Block Guide for information on HCS12 Multiplexed External Bus Interface module.

6.3.1 Device-specific information

- PUCR
  - Reset state: $90

Figure 22-4 Recommended PCB Layout for 80QFP Pierce Oscillator



NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to* ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	4.5	5	5.25	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage [1]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator	f_{osc}	0.5	-	16	MHz
Bus Frequency	f_{bus}	0.25[2]	-	25	MHz
MC9S12DJ64**C** Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	85	°C
MC9S12DJ64**V** Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	105	°C
MC9S12DJ64**M** Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.
3. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}-V_{RL}	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=5.0 Volts)	t_{REC}			20	µs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted
$V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV
$f_{ATDCLK} = 2.0MHz$

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB		20		mV
6	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error[1]	AE	-1.5	±1.0	1.5	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-11** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Row Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Row programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

A.6 MSCAN

Table A-17 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs