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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12d64mfue

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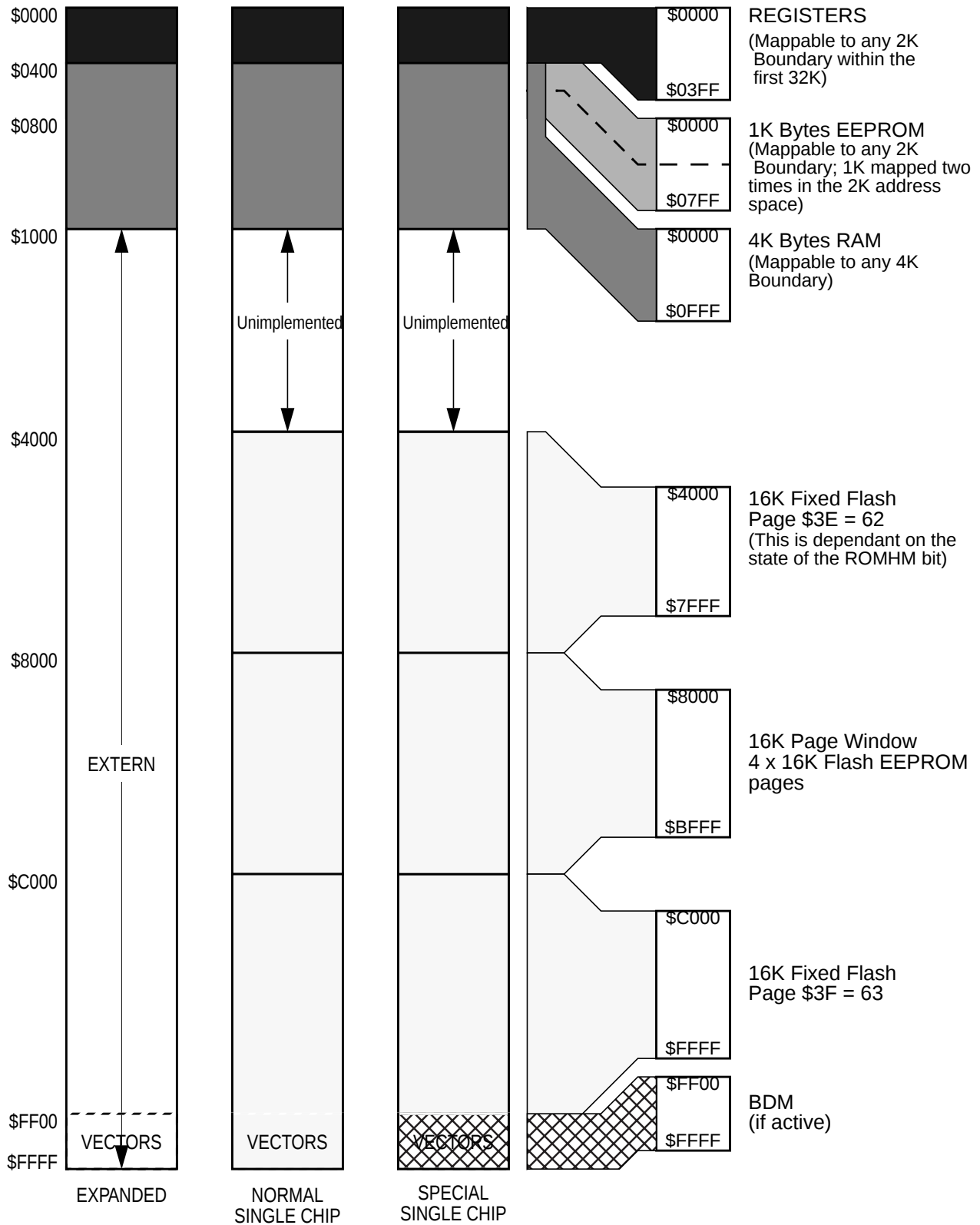
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Figure 1-2 MC9S12DJ64 Memory Map out of Reset



1.5.1 Detailed Register Map

\$0000 - \$000F

MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
\$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
\$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
\$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
\$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
\$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
\$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
\$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
\$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								

\$0100 - \$010F**Flash Control Register (fts64k)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$010A	FDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$010B	FDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$010C - \$010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0110 - \$011B**EEPROM Control Register (eets1k)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
\$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0112	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
\$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
\$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
\$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
\$0117	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0118	EADDRHI	Read:	0	0	0	0	0	0	0	Bit 8
		Write:								
\$0119	EADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$011A	EDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$011B	EDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$011C - \$011F**Reserved for RAM Control Register**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$011C - \$011F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0120 - \$013F**ATD1 (Analog to Digital Converter 10 Bit 8 Channel)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0120	ATD1CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0121	ATD1CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0122	ATD1CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
\$0123	ATD1CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
\$0124	ATD1CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
\$0125	ATD1CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
\$0126	ATD1STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
\$0127	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0128	ATD1TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0129	ATD1TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
\$012A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$012B	ATD1STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
\$012C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$012D	ATD1DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$012E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$012F	PORTAD1	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
\$0130	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0131	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0132	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0133	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0134	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0135	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0136	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$0137	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$0138	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

\$0120 - \$013F**ATD1 (Analog to Digital Converter 10 Bit 8 Channel)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0139	ATD1DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013A	ATD1DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013B	ATD1DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013C	ATD1DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013D	ATD1DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013E	ATD1DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013F	ATD1DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

\$0140 - \$017F**CAN0 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								

\$0140 - \$017F**CAN0 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0150 - \$0153	CAN0IDAR0 - CAN0IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0154 - \$0157	CAN0IDMR0 - CAN0IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0158 - \$015B	CAN0IDAR4 - CAN0IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$015C - \$015F	CAN0IDMR4 - CAN0IDMR7	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0160 - \$016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see Table 1-3							
		Write:								
\$0170 - \$017F	CAN0TXFG	Read:	FOREGROUND TRANSMIT BUFFER see Table 1-3							
		Write:								

Table 1-3 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
\$0160	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN0RIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
\$0161	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CAN0RIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
\$0162	Standard ID	Read:								
	CAN0RIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
\$0163	Standard ID	Read:								
	CAN0RIDR3	Write:								
\$0164 - \$016B	CAN0RDSR0 - CAN0RDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
		Read:					DLC3	DLC2	DLC1	DLC0
\$016C	CAN0RDLR	Write:								
\$016D	Reserved	Read:								
		Write:								
		Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
\$016E	CAN0RTSRH	Write:								
		Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
\$016F	CAN0RTSRL	Write:								
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
\$0170	CAN0TIDR0	Write:								
	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
\$0171	CAN0TIDR1	Write:								
	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
		Write:								

\$0240 - \$027F**PIM (Port Integration Module)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0263	RDRH	Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
\$0264	PERH	Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
\$0265	PPSH	Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
\$0266	PIEH	Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
\$0267	PIFH	Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
\$0268	PTJ	Read: Write:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
\$0269	PTIJ	Read: Write:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
\$026A	DDRJ	Read: Write:	DDRJ7	DDRJ7	0	0	0	0	DDRJ1	DDRJ0
\$026B	RDRJ	Read: Write:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
\$026C	PERJ	Read: Write:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
\$026D	PPSJ	Read: Write:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
\$026E	PIEJ	Read: Write:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
\$026F	PIFJ	Read: Write:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
\$0270 - \$027F	Reserved	Read: Write:	0	0	0	0	0	0	0	0

\$0280 - \$03FF**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0280 - \$03FF	Reserved	Read: Write:	0	0	0	0	0	0	0	0

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

6.4 HCS12 Interrupt (INT) Block Description

Consult the INT Block Guide for information on the HCS12 Interrupt module.

6.5 HCS12 Background Debug (BDM) Block Description

Consult the BDM Block Guide for information on the HCS12 Background Debug module.

6.5.1 Device-specific information

When the BDM Block Guide refers to *alternate clock* this is equivalent to *Oscillator Clock*.

6.6 HCS12 Breakpoint (BKP) Block Description

Consult the BKP Block Guide for information on the HCS12 Breakpoint module.

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

The Low Voltage Reset feature of the CRG is not available on this device.

Section 8 Oscillator (OSC) Block Description

Consult the OSC Block User Guide for information about the Oscillator module.

8.1 Device-specific information

The $\overline{\text{XCLKS}}$ input signal is active low (see 2.3.13 PE7 / NOACC / XCLKS — Port E I/O Pin 7).

Section 9 Enhanced Capture Timer (ECT) Block Description

Consult the ECT_16B8C Block User Guide for information about the Enhanced Capture Timer module. When the ECT_16B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 10 Analog to Digital Converter (ATD) Block Description

There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12DJ64. Consult the ATD_10B8C Block User Guide for information about each Analog to Digital Converter module. When the ATD_10B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 11 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 12 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12DJ64 device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 13 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 14 J1850 (BDLC) Block Description

Consult the BDLC Block User Guide for information about the J1850 module.

Section 15 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 16 Flash EEPROM 64K Block Description

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For $R_{DS(on)}$ is valid:

$$R_{DS(on)} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DS(on)} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics¹

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB ²	θ_{JA}	—	—	54	$^{\circ}\text{C/W}$
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes ³	θ_{JA}	—	—	41	$^{\circ}\text{C/W}$
3	T	Junction to Board LQFP112	θ_{JB}	—	—	31	$^{\circ}\text{C/W}$
4	T	Junction to Case LQFP112	θ_{JC}	—	—	11	$^{\circ}\text{C/W}$
5	T	Junction to Package Top LQFP112	Ψ_{JT}	—	—	2	$^{\circ}\text{C/W}$
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	$^{\circ}\text{C/W}$
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	$^{\circ}\text{C/W}$
8	T	Junction to Board QFP80	θ_{JB}	—	—	27	$^{\circ}\text{C/W}$
9	T	Junction to Case QFP80	θ_{JC}	—	—	14	$^{\circ}\text{C/W}$
10	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	3	$^{\circ}\text{C/W}$

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{WTS} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the $\overline{XCLKS}$ signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UOSC} . The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA} .

Table A-15 Oscillator Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5		16	MHz
1b	C	Crystal oscillator range (Pierce) ¹	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			μA
3	C	Oscillator start-up time (Colpitts)	t_{UOSC}		8^2	100^3	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency ⁴	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high	t_{EXTH}	9.5			ns
9	D	External square wave rise time	t_{EXTR}			1	ns
10	D	External square wave fall time	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V
13	P	EXTAL Pin Input High Voltage ⁴	$V_{IH,EXTAL}$	$0.75 \cdot V_{DDPLL}$			V
	T	EXTAL Pin Input High Voltage ⁴	$V_{IH,EXTAL}$			$V_{DDPLL} + 0.3$	V
14	P	EXTAL Pin Input Low Voltage ⁴	$V_{IL,EXTAL}$			$0.25 \cdot V_{DDPLL}$	V
	T	EXTAL Pin Input Low Voltage ⁴	$V_{IL,EXTAL}$	$V_{DDPLL} - 0.3$			V
15	C	EXTAL Pin Input Hysteresis ⁴	$V_{HYS,EXTAL}$		250		mV

The phase detector relationship is given by:

$$K_{\Phi} = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (\text{synr} + 1) = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth $f_C=10\text{kHz}$:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_{\Phi}} = 2 \cdot \pi \cdot 50 \cdot 10\text{kHz} / (316.7\text{Hz}/\Omega) = 9.9\text{k}\Omega \approx 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) = 5.19\text{nF} \approx 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \quad C_p = 470\text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock f_{cmp} , the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.

A.6 MSCAN

Table A-17 MSCAN Wake-up Pulse Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	μs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			μs

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-9** with the actual timing values shown on table **Table A-20**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

B.2 112-pin LQFP package

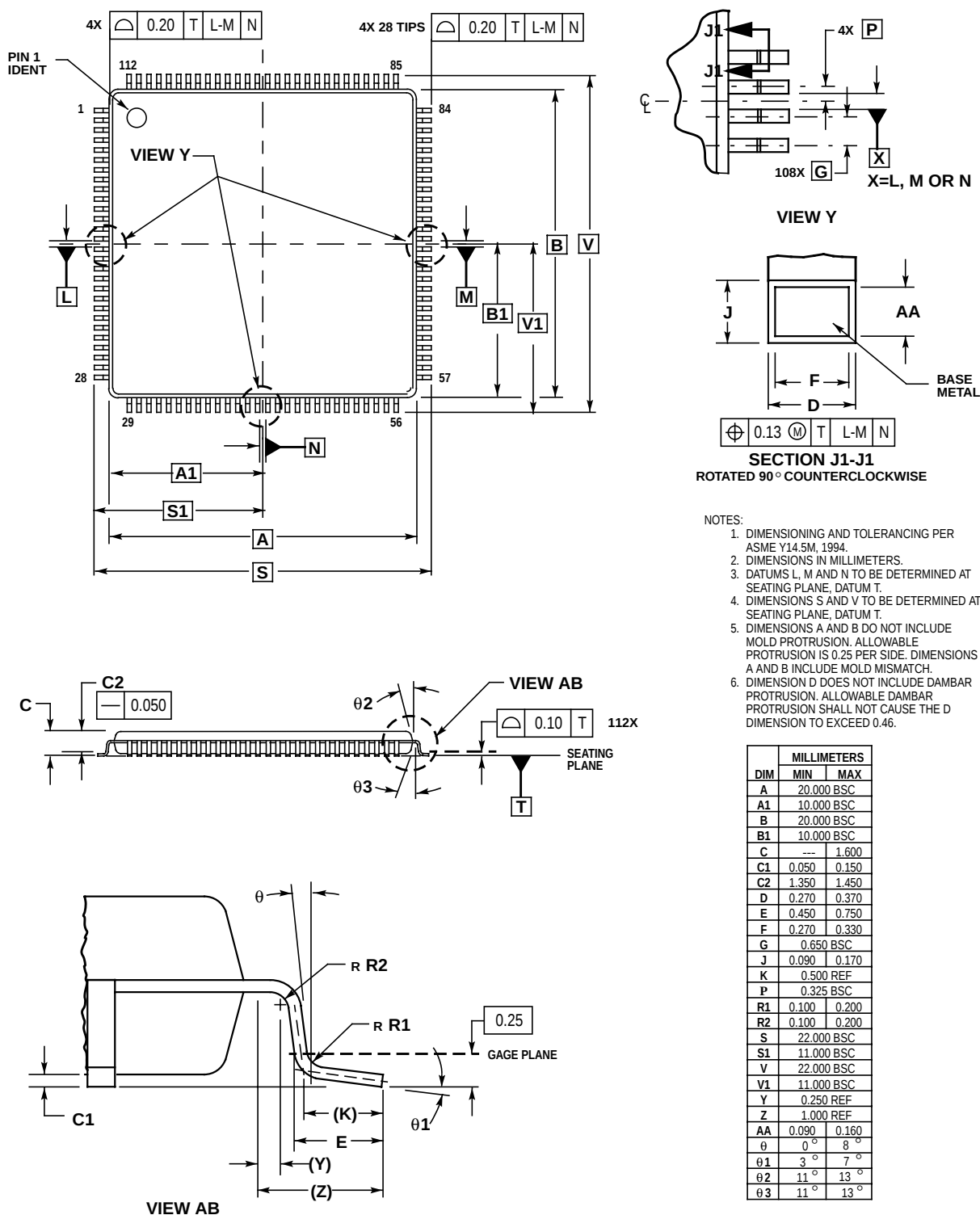


Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)

