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Applications of "Embedded - Microcontrollers"

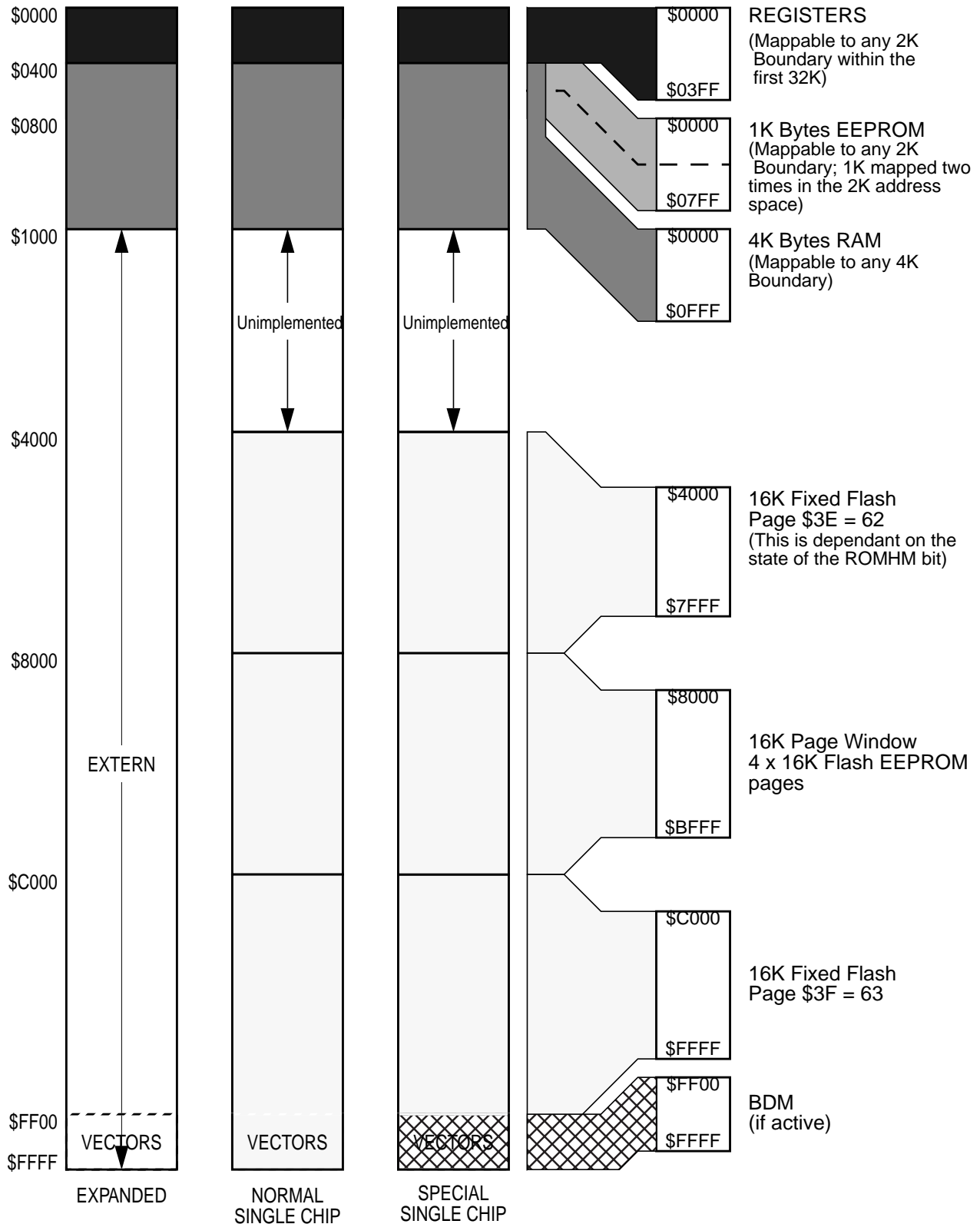| Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12d64vpver

Table of Contents

Figure 1-2 MC9S12DJ64 Memory Map out of Reset

$0010 - $0014   **MMC map 1 of 4 (HCS12 Module Mapping Control)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0012	INITEE	Read:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		Write:								
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
$0014	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0015 - $0016   **INT map 1 of 2 (HCS12 Interrupt)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

$0017 - $0019   **Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0017 - $0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$001A - $001B   **Device ID Register (Table 1-4)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

$001C - $001D   **MMC map 3 of 4 (HCS12 Module Mapping Control, Table 1-5)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

$001E - $001E   **MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

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$00A0 - $00C7   **PWM (Pulse Width Modulator 8 Bit 8 Channel)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A9	PWMSCLB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00AA	PWMSCNTA Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00AB	PWMSCNTB Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00AC	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AD	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AE	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00AF	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B0	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B2	PWMCNT6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B3	PWMCNT7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00B4	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B5	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B6	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B7	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B8	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00B9	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BA	PWMPER6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BB	PWMPER7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BC	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BD	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BE	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00BF	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C0	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00C1	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

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$00A0 - $00C7   PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C2	PWMDTY6	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00C3	PWMDTY7	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$00C4	PWMSDN	Read:	PWMIF	PWMIE	PWMRSTRT	PWMLVL	0	PWM7IN	PWM7INL	PWM7ENA
		Write:								
$00C5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C8 - $00CF   SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCI0BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00C9	SCI0BDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00CA	SCI0CR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00CB	SCI0CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00CC	SCI0SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCI0SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00CE	SCI0DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCI0DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D0 - $00D7   SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCI1BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCI1BDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00D2	SCI1CR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00D3	SCI1CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00D4	SCI1SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								

$00D0 - $00D7   SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D5	SCI1SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D8 - $00DF   SPI0 (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPI0CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00D9	SPI0CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPI0BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPI0SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DD	SPI0DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7   IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D 0
		Write:								
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

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$0240 - $027F   **PIM (Port Integration Module)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0263	RDRH	Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
$0264	PERH	Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
$0265	PPSH	Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
$0266	PIEH	Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
$0267	PIFH	Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
$0268	PTJ	Read: Write:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
$0269	PTIJ	Read: Write:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
$026A	DDRJ	Read: Write:	DDRJ7	DDRJ7	0	0	0	0	DDRJ1	DDRJ0
$026B	RDRJ	Read: Write:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
$026C	PERJ	Read: Write:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
$026D	PPSJ	Read: Write:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
$026E	PIEJ	Read: Write:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
$026F	PIFJ	Read: Write:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
$0270 - $027F	Reserved	Read: Write:	0	0	0	0	0	0	0	0

$0280 - $03FF   **Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0280 - $03FF	Reserved	Read: Write:	0	0	0	0	0	0	0	0

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Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12DJ64 is available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). The MC9S12D32 is only available in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1** and **Figure 2-2** show the pin assignments.

2.3.30 PJ6 / KWJ6 / SDA / RXCAN0 — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial data pin SDA of the IIC module. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0).

2.3.31 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.32 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit. For a complete list of modes refer to **4.2 Chip Configuration Summary**.

2.3.33 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

2.3.34 PM7 — Port M I/O Pin 7

PM7 is a general purpose input or output pin.

2.3.35 PM6 — Port M I/O Pin 6

PM6 is a general purpose input or output pin.

2.3.36 PM5 / TXCAN0 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.37 PM4 / RXCAN0 / MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

Table 4-2 Clock Selection Based on PE7

PE7 = $\overline{\text{XCLKS}}$	Description
0	Pierce Oscillator/external clock selected

Table 4-3 Voltage Regulator VREGEN

VREGEN	Description
1	Internal Voltage Regulator enabled
0	Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,

- Protection of the contents of EEPROM,

- Operation in single-chip mode,

- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

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6.4 HCS12 Interrupt (INT) Block Description

Consult the INT Block Guide for information on the HCS12 Interrupt module.

6.5 HCS12 Background Debug (BDM) Block Description

Consult the BDM Block Guide for information on the HCS12 Background Debug module.

6.5.1 Device-specific information

When the BDM Block Guide refers to *alternate clock* this is equivalent to *Oscillator Clock*.

6.6 HCS12 Breakpoint (BKP) Block Description

Consult the BKP Block Guide for information on the HCS12 Breakpoint module.

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

The Low Voltage Reset feature of the CRG is not available on this device.

Section 8 Oscillator (OSC) Block Description

Consult the OSC Block User Guide for information about the Oscillator module.

8.1 Device-specific information

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.13 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 9 Enhanced Capture Timer (ECT) Block Description

Consult the ECT_16B8C Block User Guide for information about the Enhanced Capture Timer module. When the ECT_16B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

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A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 1 1	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	T	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	T	Machine Model (MM)	V_{MM}	200	-	V
3	T	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	T	Latch-up Current at $T_A = 125°C$ positive negative	I_{LAT}	+100 -100	-	mA
5	T	Latch-up Current at $T_A = 27°C$ positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

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Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	–	–	31	°C/W
4	T	Junction to Case LQFP112	θ_{JC}	–	–	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	–	–	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	–	–	51	°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	–	–	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	–	–	27	°C/W
9	T	Junction to Case QFP80	θ_{JC}	–	–	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	–	–	3	°C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10   ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV $f_{ATDCLK} = 2.0MHz$							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	−1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	−2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB		20		mV
6	P	8-Bit Differential Nonlinearity	DNL	−0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	−1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error[1]	AE	-1.5	±1.0	1.5	Counts

NOTES:
 1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table A-12   NVM Reliability Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
		Conditions are shown in **Table A-4** unless otherwise noted					
1	C	Data Retention at an average junction temperature of $T_{Javg} = 85°C$[1]	t_{NVMRET}	15			Years
2	C	Flash number of Program/Erase cycles	n_{FLPE}	10,000			Cycles
3	C	EEPROM number of Program/Erase cycles ($-40°C \leq T_J \leq 0°C$)	n_{EEPE}	10,000			Cycles
4	C	EEPROM number of Program/Erase cycles ($0°C < T_J \leq 140°C$)	n_{EEPE}	100,000			Cycles

NOTES:
1. Total time at the maximum guaranteed device operating temperature <= 1 year

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A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the $\overline{XCLKS}$ signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-15 Oscillator Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
Conditions are shown in **Table A-4** unless otherwise noted
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5		16	MHz
1b	C	Crystal oscillator range (Pierce) [1]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			μA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}		8^2	100^3	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [4]	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high	t_{EXTH}	9.5			ns
9	D	External square wave rise time	t_{EXTR}			1	ns
10	D	External square wave fall time	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V
13	P	EXTAL Pin Input High Voltage[4]	$V_{IH,EXTAL}$	$0.75*V_{DDPLL}$			V
	T	EXTAL Pin Input High Voltage[4]	$V_{IH,EXTAL}$			$V_{DDPLL}+ 0.3$	V
14	P	EXTAL Pin Input Low Voltage[4]	$V_{IL,EXTAL}$			$0.25*V_{DDPLL}$	V
	T	EXTAL Pin Input Low Voltage[4]	$V_{IL,EXTAL}$	$V_{DDPLL} - 0.3$			V
15	C	EXTAL Pin Input Hysteresis[4]	$V_{HYS,EXTAL}$		250		mV