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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dj64cpve

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.06	20 Aug. 2002	20 Aug. 2002		NVM electricals updated Subsection "Detailed Register Map: Address corrections Preface, Table "Document references": added OSC User Guide New section "Oscillator (OSC) Block Description"
V01.07	20 Sept. 2002	20 Sept. 2002		Electrical Characteristics: -> Section "General": removed preliminary disclaimer ->Table "Supply Current Characteristics": changed max Run IDD from 65mA to 50mA changes max Wait IDD from 40mA to 30mA changed max Stop IDD from 50uA to 100uA Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock
V01.08	25 Sept. 2002	25 Sept. 2002		Table "5V I/O Characteristics": Corrected Input Leakage Current to +/- 1 uA Section "Part ID assignment": Located on start of next page for better readability
V01.09	10 Oct. 2002	10 Oct. 2002		Added MC9S12A64 derivative to cover sheet and "Derivative Differences" Table Corrected in footnote of Table "PLL Characteristics": f_{OSC} = 4MHz
V01.10	8 Nov. 2002	8 Nov. 2002		Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0 and/or BDLC Table "ESD and Latch-up Test Conditions": changed pulse numbers from 3 to 1 Table "ESD and Latch-Up Protection Characteristics": changed parameter classification from C to T Table "5V I/O Characteristics": removed foot note from "Input Leakage Current" Table " Supply Current Characteristics": updated Stop and Pseudo Stop currents
V01.11	24 Jan. 2003	24 Jan. 2003		Subsection "Detailed Register Map": Corrected several entries Subsection "Unsecuring the Microcontroller": Added more details Table "Operating Conditions": improved footnote 1 wording, applied footnote 1 to PLL Supply Voltage.
V01.12	31 Mar. 2003	31 Mar. 2003		Tables "SPI Master/Slave Mode Timing Characteristics: Corrected Operating Frequency Appendix 'NVM, Flash and EEPROM': Replaced 'burst programming' by 'row programming Table "Operating Conditions": corrected minimum bus frequency to 0.25MHz Section "Feature List": ECT features changed to "Four pulse accumulators ..."
V01.13	20 May 2003	20 May 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides Table "Signal Properties" corrected pull resistor reset state for PE7 and PE4-PE2. Table "Absolute Maximum Ratings" corrected footnote on clamp of TEST pin.
V01.14	10 June 2003	10 June 2003		Added cycle definition to "CPU 12 Block Description". Added register reset values to MMC and MEBI block descriptions. Diagram "Clock Connections": Connect Bus Clock to HCS12 Core

- **Ports**
  - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **Table 0-1**).
  - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **Table 0-1**).
  - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DJ64 Block User Guide), if using a derivative without CAN0 (see **Table 0-1**).
- **Pins not available in 80 pin QFP package**
  - **Port H**
    In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).
  - **Port J[1:0]**
    Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+$026C.
  - **Port K**
    Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefor care must be taken not to clear this bit.
  - **Port M[7:6]**
    PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
  - **Port P6**
    PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.
  - **Port S[7:4]**
    PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
  - **PAD[15:8] (ATD1 channels)**
    Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

Document References

The Device User Guide provides information about the MC9S12DJ64 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-2** for names and versions of the referenced documents throughout the Device User Guide.

Table 1-2 Device Memory Map for MC9S12D32

Address	Module	Size (Bytes)
$0000 - $000F	HCS12 Multiplexed External Bus Interface	16
$0010 - $0014	HCS12 Module Mapping Control	5
$0015 - $0016	HCS12 Interrupt	2
$0017 - $0019	Reserved	3
$001A - $001B	Device ID register (PARTID)	2
$001C - $001D	HCS12 Module Mapping Control	2
$001E	HCS12 Multiplexed External Bus Interface	1
$001F	HCS12 Interrupt	1
$0020 - $0027	Reserved	8
$0028 - $002F	HCS12 Breakpoint Module	8
$0030 - $0031	HCS12 Module Mapping Control	2
$0032 - $0033	HCS12 Multiplexed External Bus Interface	2
$0034 - $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 - $007F	Enhanced Capture Timer 16-bit 8 channels	64
$0080 - $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
$00A0 - $00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$00C8 - $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 - $00D7	Serial Communications Interface 0 (SCI1)	8
$00D8 - $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 - $00E7	Inter IC Bus	8
$00E8 - $00EF	Byte Data Link Controller (BDLC)	8
$00F0 - $00FF	Reserved	16
$0100- $010F	Flash Control Register	16
$0110 - $011B	EEPROM Control Register	12
$011C - $011F	Reserved	4
$0120 - $013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
$0140 - $017F	Freescale Scalable Can (CAN0)	64
$0180 - $023F	Reserved	192
$0240 - $027F	Port Integration Module (PIM)	64
$0280 - $03FF	Reserved	384
$0000 - $07FF	EEPROM array 1k Array mapped twice in the address space	2048
$0000 - $0FFF	RAM array, lower half ($0000-$07FF not usable)	4096
$4000 - $7FFF	16k Fixed Flash EEPROM array (same as array from $8000 - $BFFF when ROMHM=0)	16384
$8000 - $FFFF	32K Fixed Flash EEPROM array	32768

$0080 - $009F ATD0 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0092	ATD0DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATD0DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATD0DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATD0DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATD0DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATD0DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATD0DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATD0DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATD0DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATD0DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATD0DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATD0DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATD0DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATD0DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00A0 - $00C7 PWM (Pulse Width Modulator 8 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A0	PWME	Read:	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$00A1	PWMPOL	Read:	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$00A2	PWMCLK	Read:	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$00A3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$00A4	PWMCAE	Read:	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$00A5	PWMCTL	Read:	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$00A6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A7	PWMPRSC Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00A8	PWMSCLA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0120 - $013F ATD1 (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	ATD1CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0121	ATD1CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0122	ATD1CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0123	ATD1CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0124	ATD1CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0125	ATD1CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0126	ATD1STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0127	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0128	ATD1TEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0129	ATD1TEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$012A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012B	ATD1STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$012C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012D	ATD1DIEN	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$012E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$012F	PORTAD1	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$0130	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0131	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0132	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0133	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0134	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0135	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0136	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0137	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0138	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$024A	DDRS	Read:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
$024B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
$024C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
$024D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
$024E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								
$0253	RDRM	Read:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		Write:								
$0254	PERM	Read:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
$0255	PPSM	Read:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
$0256	WOMM	Read:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
$0257	MODRR	Read:	0	0	0	MODRR4	0	0	MODRR1	MODRR0
		Write:								
$0258	PTP	Read:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$025B	RDRP	Read:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$025C	PERP	Read:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$025D	PPSP	Read:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$025E	PIEP	Read:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		Write:								
$025F	PIFP	Read:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		Write:								
$0260	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0262	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B after reset). The read-only value is a unique part ID for each revision of the chip. **Table 1-4** shows the assigned part ID number.

Table 1-4 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12DJ64	0L86D	$0200
MC9S12DJ64	1L86D	$0201
MC9S12DJ64	2L86D	$0201[2]
MC9S12DJ64	3L86D	$0203
MC9S12DJ64	4L86D	$0204
MC9S12DJ64	0M89C	$0204

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision
2. 1L86D is identical to 2L86D except improved ESD performance on 2L86D

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-5** shows the read-only values of these registers. Refer to HCS12 Module Mapping Control (MMC) Block Guide for further details.

Table 1-5 Memory size registers

Register name	Value
MEMSIZ0	$11
MEMSIZ1	$80

Table 2-1 Signal Properties

Pin Name Function1	Pin Name Function2	Pin Name Function3	Pin Name Function4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	None	None	Oscillator Pins
XTAL	—	—	—				
$\overline{\text{RESET}}$	—	—	—	VDDR			External Reset
TEST	—	—	—	N.A.			Test Input
VREGEN	—	—	—	VDDX			Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL			PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD15	**AN15**	**ETRIG1**	**—**	VDDA	None	None	**Port AD Input, Analog Input AN7 of ATD1, External Trigger Input of ATD1**
PAD[14:08]	**AN[14:08]**	**—**	**—**				**Port AD Inputs, Analog Inputs AN[6:0] of ATD1**
PAD07	AN07	ETRIG0	—				Port AD Input, Analog Input AN7 of ATD0, External Trigger Input of ATD0
PAD[06:00]	AN[06:00]	—	—				Port AD Inputs, Analog Inputs AN[6:0] of ATD0
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	PUCR/ PUPAE	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—		PUCR/ PUPBE		Port B I/O, Multiplexed Address/Data
PE7	NOACC	$\overline{\text{XCLKS}}$	—		PUCR/ PUPEE	Mode depen-dant[1]	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—		While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—				Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—		PUCR/ PUPEE	Mode depen-dant[1]	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—				Port E I/O, Byte Strobe, Tag Low
PE2	R/$\overline{\text{W}}$	—	—				Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—			Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—				Port E Input, Non Maskable Interrupt
PH7	**KWH7**	—	—		PERH/ PPSH	Disabled	**Port H I/O, Interrupt**
PH6	**KWH6**	—	—				**Port H I/O, Interrupt**
PH5	**KWH5**	—	—				**Port H I/O, Interrupt**
PH4	**KWH4**	—	—				**Port H I/O, Interrupt**
PH3	**KWH3**	—	—				**Port H I/O, Interrupt**
PH2	**KWH2**	—	—				**Port H I/O, Interrupt**
PH1	**KWH1**	—	—				**Port H I/O, Interrupt**
PH0	**KWH0**	—	—				**Port H I/O, Interrupt**

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

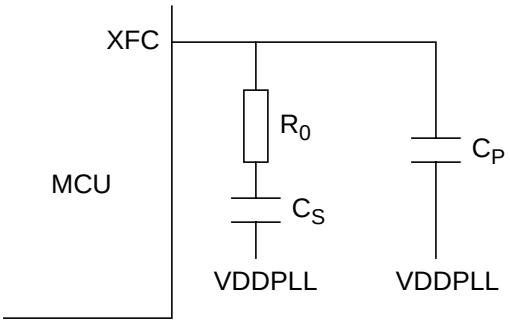
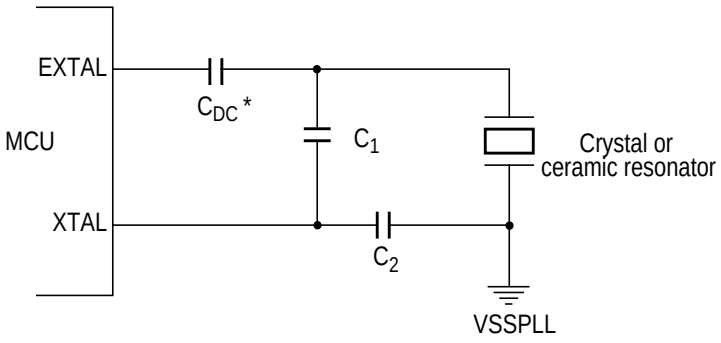


Figure 2-3 PLL Loop Filter Connections

2.3.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

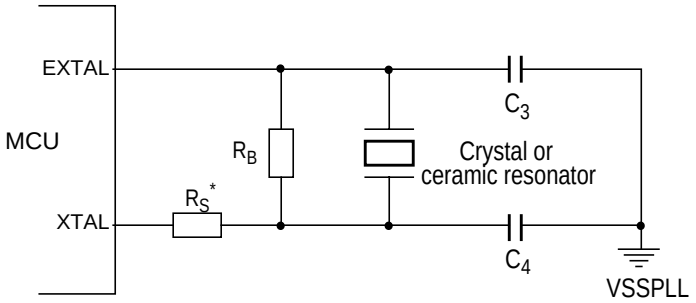
The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal

Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value C_{DC}.

Figure 2-4 Colpitts Oscillator Connections (PE7=1)



* Rs can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 2-5 Pierce Oscillator Connections (PE7=0)

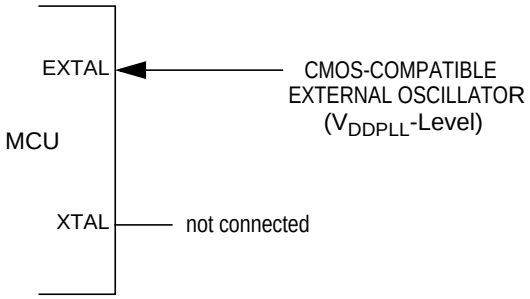


Figure 2-6 External Clock Connections (PE7=0)

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator.

NOTE: *No load allowed except for bypass capacitors.*

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

Consult the FTS64K Block User Guide for information about the flash module.

The "S12 LRAE" is a generic Load RAM and Execute (LRAE) program which will be programmed into the flash memory of this device during manufacture. This LRAE program will provide greater programming flexibility to the end users by allowing the device to be programmed directly using CAN or SCI after it is assembled on the PCB. Use of the LRAE program is at the discretion of the end user and, if not required, it must simply be erased prior to flash programming. For more details of the S12 LRAE and its implementation, please see the S12 LREA Application Note (AN2546/D).

It is planned that most HC9S12 devices manufactured after Q1 of 2004 will be shipped with the S12 LRAE programmed in the Flash . Exact details of the changeover (ie blank to programmed) for each product will be communicated in advance via GPCN and will be traceable by the customer via datecode marking on the device.

Please contact Freescale SPS Sales if you have any additional questions.

Section 17 EEPROM 1K Block Description

Consult the EETS1K Block User Guide for information about the EEPROM module.

Section 18 RAM Block Description

This module supports single-cycle misaligned word accesses.

Section 19 MSCAN Block Description

Consult the MSCAN Block User Guide for information about the Freescale Scalable CAN Module.

Section 20 Port Integration Module (PIM) Block Description

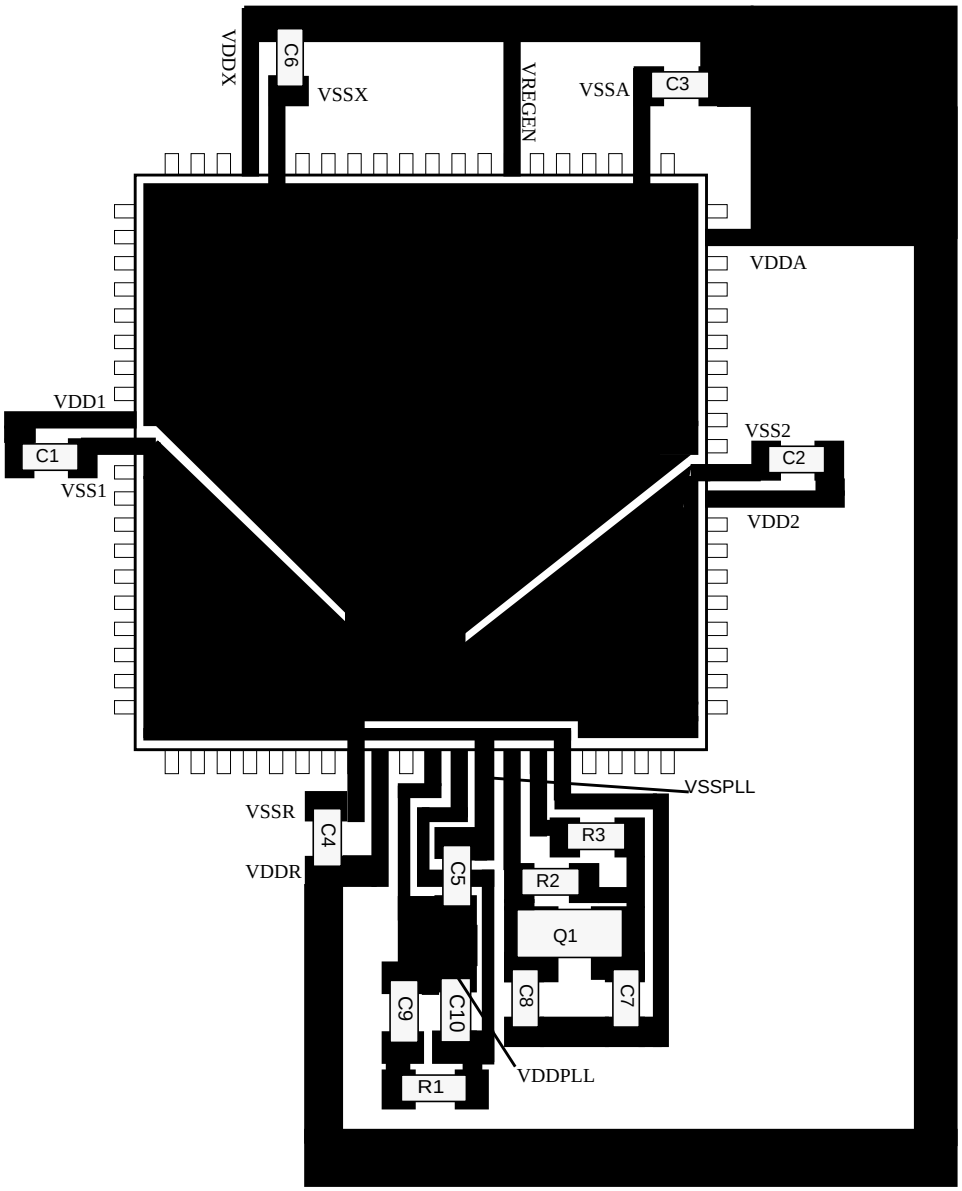
Consult the PIM_9DJ64 Block User Guide for information about the Port Integration Module.

Section 21 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

Section 22 Printed Circuit Board Layout Proposals

Figure 22-4 Recommended PCB Layout for 80QFP Pierce Oscillator



The phase detector relationship is given by:

$$K_\Phi = -\left|i_{ch}\right| \cdot K_V \qquad = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9) \qquad f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (\text{synr} + 1) \qquad = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C=10kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \qquad = 2*\pi*50*10\text{kHz}/(316.7\text{Hz}/\Omega)=9.9\text{k}\Omega=\sim 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) \qquad = 5.19\text{nF} =\sim 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \le C_p \le C_s/10 \qquad C_p = 470\text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-16 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		-100		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		60		MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$		38.5		µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$		3.5		µA
14	C	Jitter fit parameter 1[2]	j_1			1.1	%
15	C	Jitter fit parameter 2[2]	j_2			0.13	%

NOTES:

1. % deviation from target frequency
2. f_{OSC} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

A.7.2 Slave Mode

Figure A-7 and **Figure A-8** illustrate the slave mode timing. Timing values are shown in **Table A-19**.

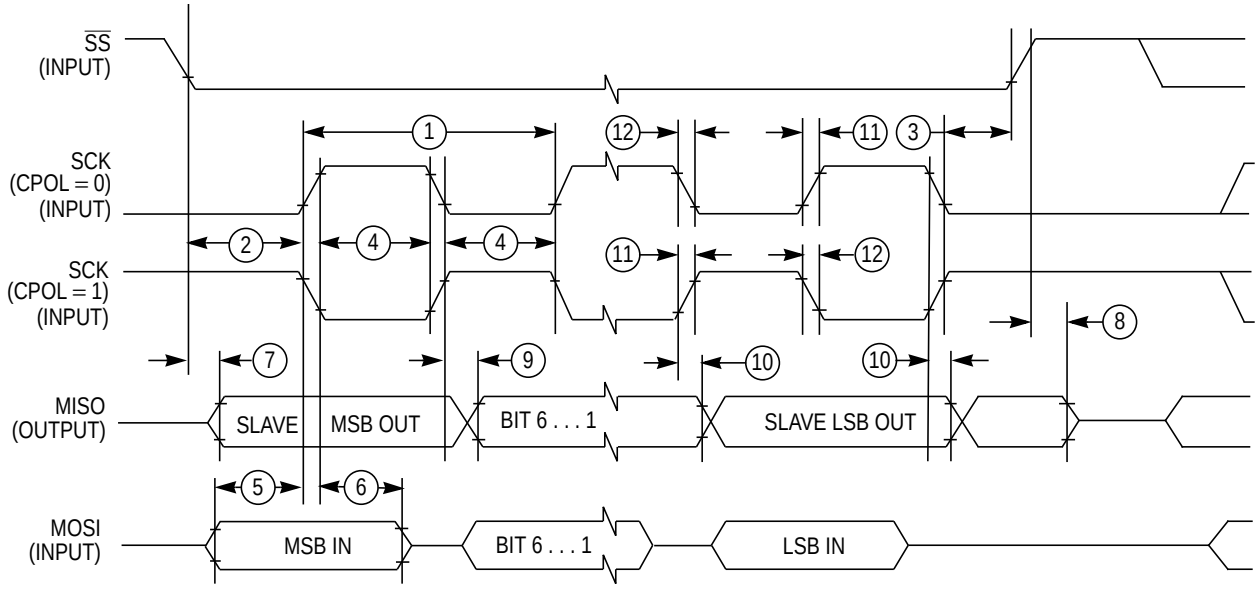


Figure A-7 SPI Slave Timing (CPHA = 0)

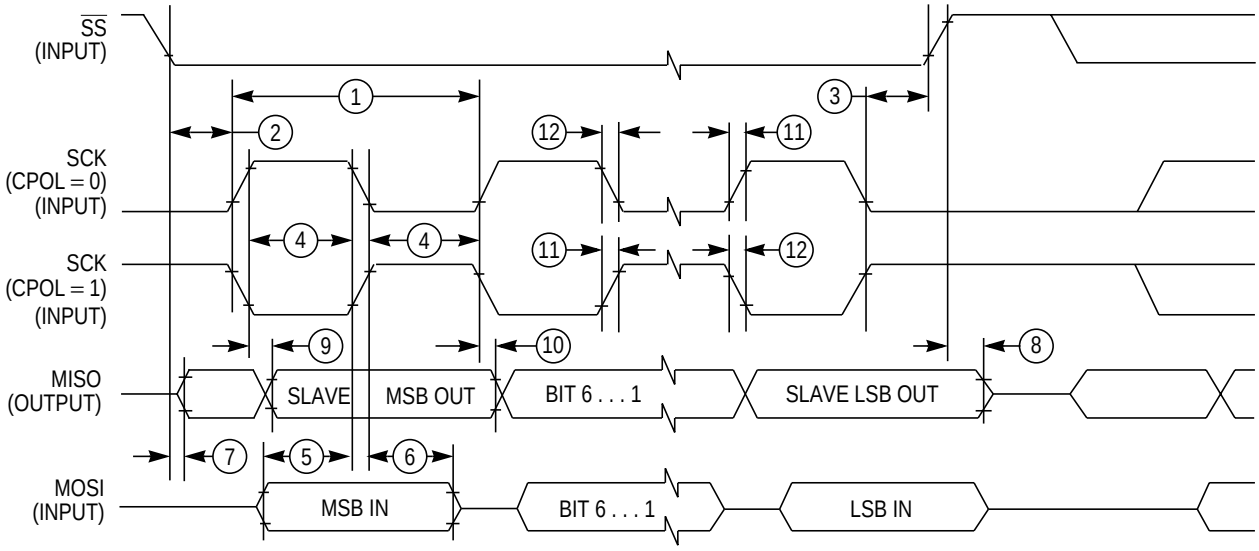


Figure A-8 SPI Slave Timing (CPHA =1)

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-9** with the actual timing values shown on table **Table A-20**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	11			ns
35	D	IPIPO[1:0] delay time[1] (PW_{EH}-t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:

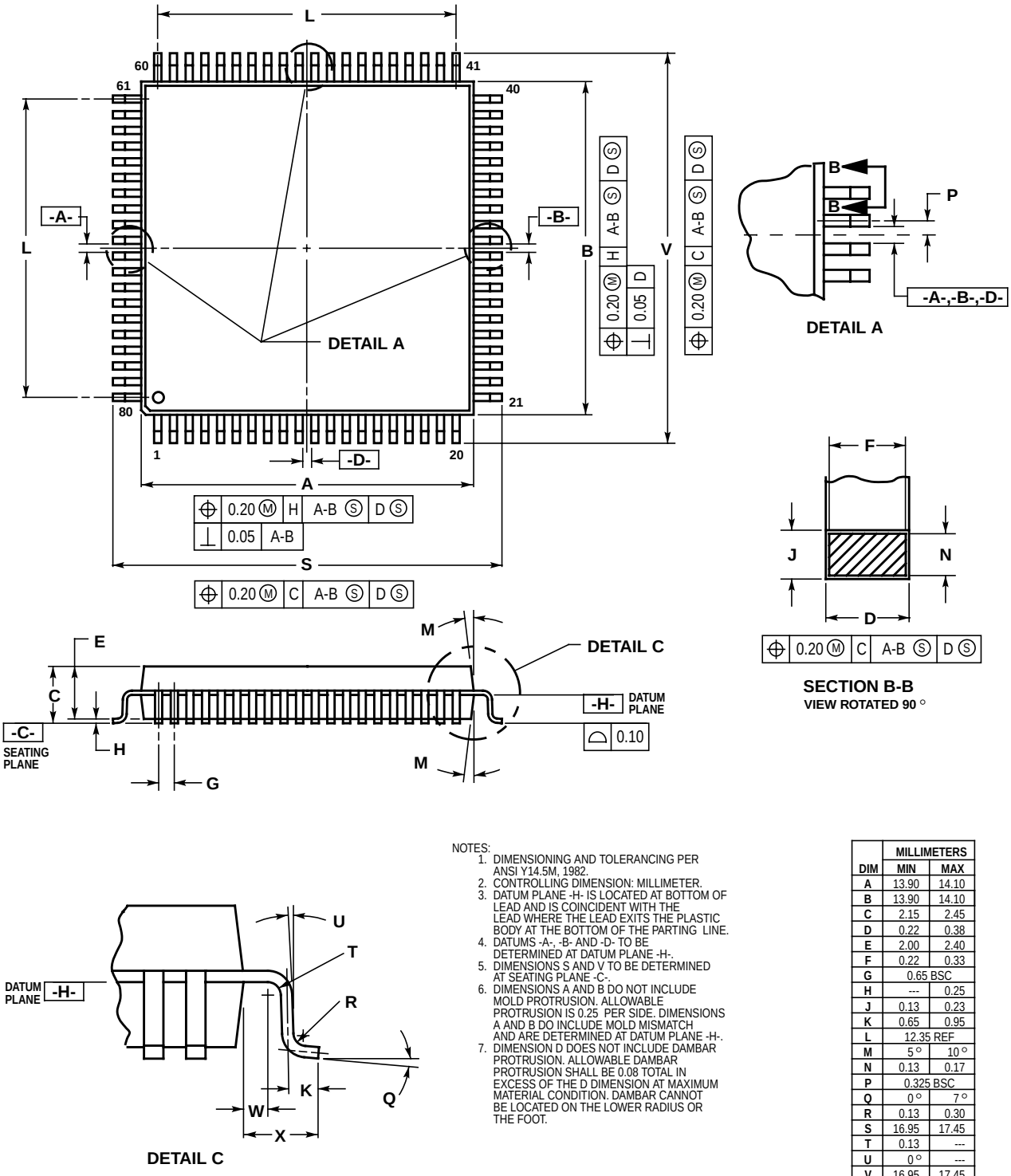
1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DJ64 and MC9S12D32 packages.

B.3 80-pin QFP package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure B-2 80-pin QFP Mechanical Dimensions (case no. 841B)