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Details

Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dj64mpve

Table 1-1 Device Memory Map for MC9S12DJ64

Address	Module	Size (Bytes)
\$C000 - \$FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at \$FF80 - \$FFFF	16384

1.5.1 Detailed Register Map

\$0000 - \$000F

MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
\$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
\$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
\$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
\$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
\$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
\$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
\$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
\$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								

\$0140 - \$017F**CAN0 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0150 - \$0153	CAN0IDAR0 - CAN0IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0154 - \$0157	CAN0IDMR0 - CAN0IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0158 - \$015B	CAN0IDAR4 - CAN0IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$015C - \$015F	CAN0IDMR4 - CAN0IDMR7	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0160 - \$016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see Table 1-3							
		Write:								
\$0170 - \$017F	CAN0TXFG	Read:	FOREGROUND TRANSMIT BUFFER see Table 1-3							
		Write:								

Table 1-3 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
\$0160	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN0RIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
\$0161	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CAN0RIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
\$0162	Standard ID	Read:								
	CAN0RIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
\$0163	Standard ID	Read:								
	CAN0RIDR3	Write:								
\$0164 - \$016B	CAN0RDSR0 - CAN0RDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
		Read:					DLC3	DLC2	DLC1	DLC0
\$016C	CAN0RDLR	Write:								
\$016D	Reserved	Read:								
		Write:								
		Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
\$016E	CAN0RTSRH	Write:								
		Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
\$016F	CAN0RTSRL	Write:								
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
\$0170	CAN0TIDR0	Write:								
	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
\$0171	CAN0TIDR1	Write:								
	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
		Write:								

Table 1-3 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

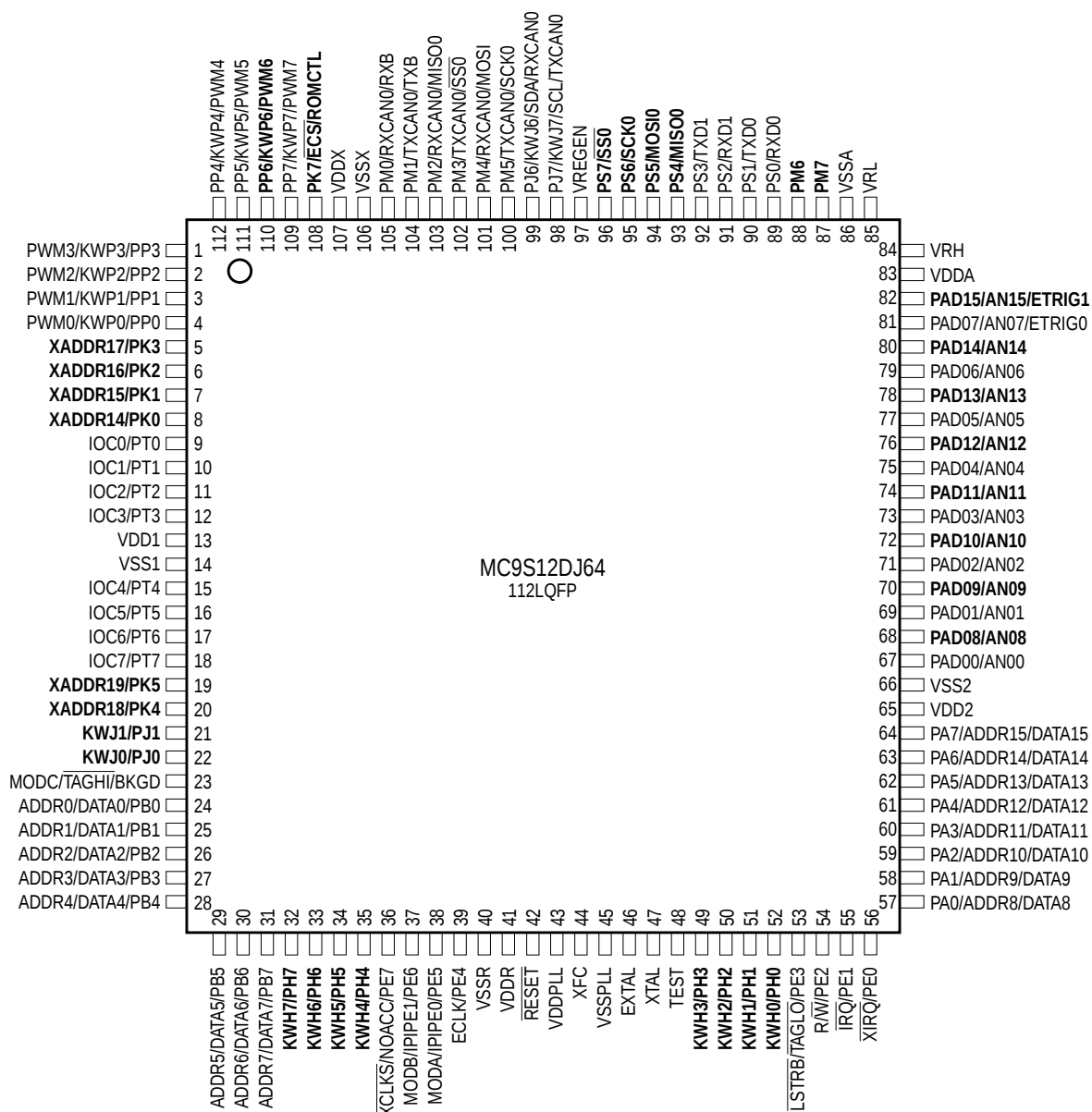
Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0172	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		Write:								
	Standard ID	Read:								
		Write:								
\$0173	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		Write:								
	Standard ID	Read:								
		Write:								
\$0174-\$017B	CAN0TDSR0 - CAN0TDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
\$017C	CAN0TDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
\$017D	CAN0TTBPR	Read:	PRI07	PRI06	PRI05	PRI04	PRI03	PRI02	PRI01	PRI00
		Write:								
\$017E	CAN0TTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
\$017F	CAN0TTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

\$0180 - \$023F**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0180 - \$023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0240 - \$027F**PIM (Port Integration Module)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0240	PTT	Read:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		Write:								
\$0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
\$0242	DDRT	Read:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		Write:								
\$0243	RDRT	Read:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		Write:								
\$0244	PERT	Read:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		Write:								
\$0245	PPST	Read:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		Write:								
\$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0248	PTS	Read:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		Write:								
\$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 2-1 Pin Assignments in 112-pin LQFP for MC9S12DJ64

Table 2-1 Signal Properties

Pin Name Function1	Pin Name Function2	Pin Name Function3	Pin Name Function4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	None	None	Oscillator Pins
XTAL	—	—	—				
RESET	—	—	—	VDDR			External Reset
TEST	—	—	—	N.A.			Test Input
VREGEN	—	—	—	VDDX			Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL			PLL Loop Filter
BKGD	TAGHI	MODC	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD15	AN15	ETRIG1	—	VDDA	None	None	Port AD Input, Analog Input AN7 of ATD1, External Trigger Input of ATD1
PAD[14:08]	AN[14:08]	—	—				Port AD Inputs, Analog Inputs AN[6:0] of ATD1
PAD07	AN07	ETRIG0	—				Port AD Input, Analog Input AN7 of ATD0, External Trigger Input of ATD0
PAD[06:00]	AN[06:00]	—	—				Port AD Inputs, Analog Inputs AN[6:0] of ATD0
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	PUCR/ PUPAE	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—		PUCR/ PUPBE		Port B I/O, Multiplexed Address/Data
PE7	NOACC	XCLKS	—		PUCR/ PUPEE	Mode depen- dant ¹	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—		While RESET pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—				Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—		PUCR/ PUPEE	Mode depen- dant ¹	Port E I/O, Bus Clock Output
PE3	LSTRB	TAGLO	—				Port E I/O, Byte Strobe, Tag Low
PE2	R/W	—	—				Port E I/O, R/W in expanded modes
PE1	IRQ	—	—			Up	Port E Input, Maskable Interrupt
PE0	XIRQ	—	—				Port E Input, Non Maskable Interrupt
PH7	KWH7	—	—		PERH/ PPSH	Disabled	Port H I/O, Interrupt
PH6	KWH6	—	—				Port H I/O, Interrupt
PH5	KWH5	—	—				Port H I/O, Interrupt
PH4	KWH4	—	—				Port H I/O, Interrupt
PH3	KWH3	—	—				Port H I/O, Interrupt
PH2	KWH2	—	—				Port H I/O, Interrupt
PH1	KWH1	—	—				Port H I/O, Interrupt
PH0	KWH0	—	—				Port H I/O, Interrupt

2.3.30 PJ6 / KWJ6 / SDA / RXCAN0 — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial data pin SDA of the IIC module. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0).

2.3.31 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.32 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit. For a complete list of modes refer to **4.2 Chip Configuration Summary**.

2.3.33 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

2.3.34 PM7 — Port M I/O Pin 7

PM7 is a general purpose input or output pin.

2.3.35 PM6 — Port M I/O Pin 6

PM6 is a general purpose input or output pin.

2.3.36 PM5 / TXCAN0 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.37 PM4 / RXCAN0 / MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

2.3.38 PM3 / TXCAN0 / $\overline{SS}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.39 PM2 / RXCAN0 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

2.3.40 PM1 / TXCAN0 / TXB — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

2.3.41 PM0 / RXCAN0 / RXB — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

2.3.42 PP7 / KWP7 / PWM7 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output.

2.3.43 PP6 / KWP6 / PWM6 — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output.

2.3.44 PP5 / KWP5 / PWM5 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output.

2.3.45 PP4 / KWP4 / PWM4 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output.

\$FFCA, \$FFCB	Modulus Down Counter underflow	I-Bit	MCCTL (MCZI)	\$CA
\$FFC8, \$FFC9	Pulse Accumulator B Overflow	I-Bit	PBCTL (PBOVI)	\$C8
\$FFC6, \$FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	\$C6
\$FFC4, \$FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	\$C4
\$FFC2, \$FFC3	BDLC	I-Bit	DLCBCR1 (IE)	\$C2
\$FFC0, \$FFC1	IIC Bus	I-Bit	IBCR (IBIE)	\$C0
\$FFBE, \$FFBF	Reserved	I-Bit	Reserved	\$BE
\$FFBC, \$FFBD		I-Bit		\$BC
\$FFBA, \$FFBB	EEPROM	I-Bit	ECNFG (CCIE, CBEIE)	\$BA
\$FFB8, \$FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	\$B8
\$FFB6, \$FFB7	CAN0 wake-up	I-Bit	CANRIER (WUPIE)	\$B6
\$FFB4, \$FFB5	CAN0 errors	I-Bit	CANRIER (CSCIE, OVRIE)	\$B4
\$FFB2, \$FFB3	CAN0 receive	I-Bit	CANRIER (RXFIE)	\$B2
\$FFB0, \$FFB1	CAN0 transmit	I-Bit	CANTIER (TXEIE2-TXEIE0)	\$B0
\$FFAE, \$FFAF	Reserved	I-Bit	Reserved	\$AE
\$FFAC, \$FFAD		I-Bit		\$AC
\$FFAA, \$FFAB		I-Bit		\$AA
\$FFA8, \$FFA9		I-Bit		\$A8
\$FFA6, \$FFA7		I-Bit		\$A6
\$FFA4, \$FFA5		I-Bit		\$A4
\$FFA2, \$FFA3		I-Bit		\$A2
\$FFA0, \$FFA1		I-Bit		\$A0
\$FF9E, \$FF9F		I-Bit		\$9E
\$FF9C, \$FF9D		I-Bit		\$9C
\$FF9A, \$FF9B		I-Bit		\$9A
\$FF98, \$FF99		I-Bit		\$98
\$FF96, \$FF97		I-Bit		\$96
\$FF94, \$FF95		I-Bit		\$94
\$FF92, \$FF93		I-Bit		\$92
\$FF90, \$FF91		I-Bit		\$90
\$FF8E, \$FF8F	Port P	I-Bit	PIEP (PIEP7-0)	\$8E
\$FF8C, \$FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)	\$8C
\$FF80 to \$FF8B	Reserved			

5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

Section 10 Analog to Digital Converter (ATD) Block Description

There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12DJ64. Consult the ATD_10B8C Block User Guide for information about each Analog to Digital Converter module. When the ATD_10B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 11 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 12 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12DJ64 device. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 13 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block User Guide for information about each Serial Peripheral Interface module.

Section 14 J1850 (BDLC) Block Description

Consult the BDLC Block User Guide for information about the J1850 module.

Section 15 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block User Guide for information about the Pulse Width Modulator module. When the PWM_8B8C Block User Guide refers to *freeze mode* this is equivalent to *active BDM mode*.

Section 16 Flash EEPROM 64K Block Description

Figure 22-4 Recommended PCB Layout for 80QFP Pierce Oscillator

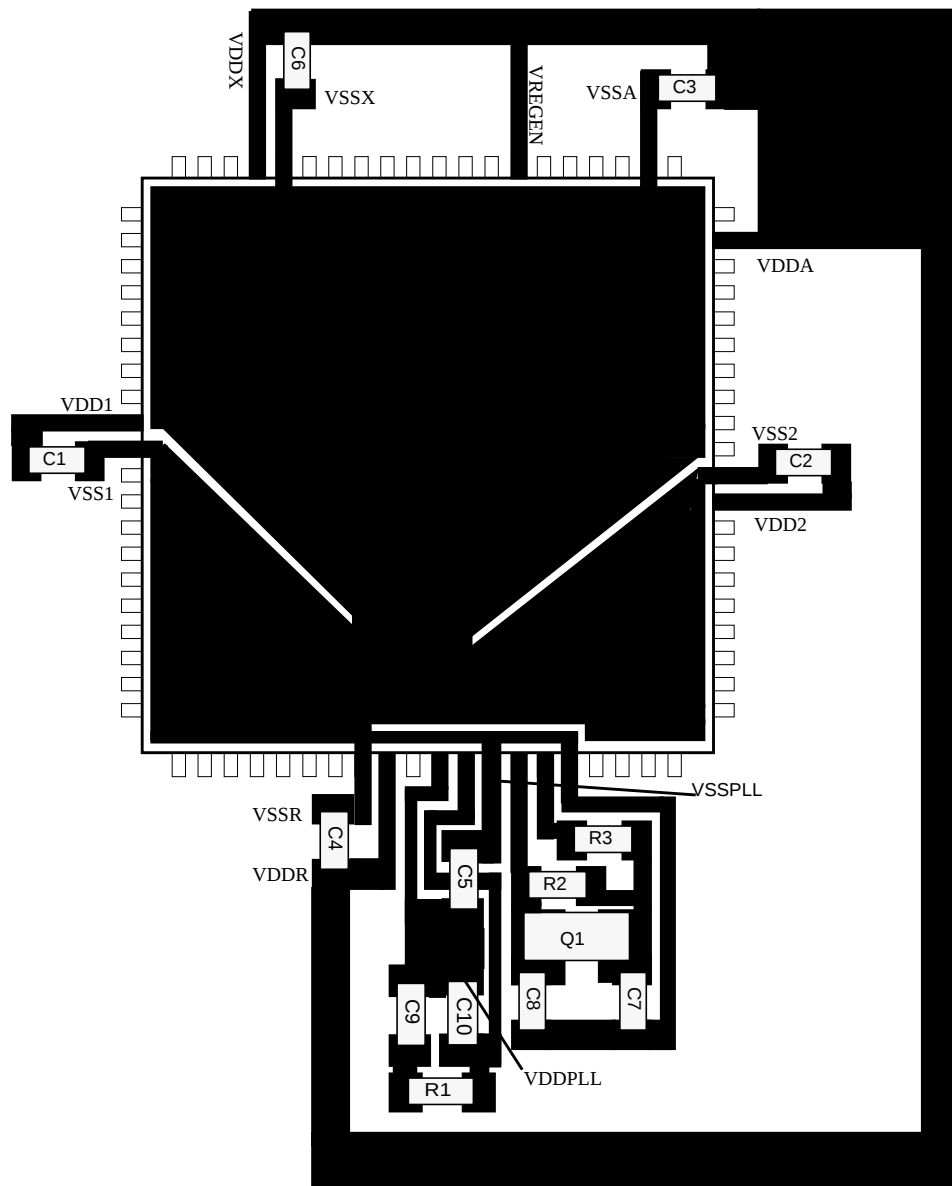


Table A-5 Thermal Package Characteristics¹

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB ²	θ_{JA}	—	—	54	$^{\circ}\text{C/W}$
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes ³	θ_{JA}	—	—	41	$^{\circ}\text{C/W}$
3	T	Junction to Board LQFP112	θ_{JB}	—	—	31	$^{\circ}\text{C/W}$
4	T	Junction to Case LQFP112	θ_{JC}	—	—	11	$^{\circ}\text{C/W}$
5	T	Junction to Package Top LQFP112	Ψ_{JT}	—	—	2	$^{\circ}\text{C/W}$
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	$^{\circ}\text{C/W}$
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	$^{\circ}\text{C/W}$
8	T	Junction to Board QFP80	θ_{JB}	—	—	27	$^{\circ}\text{C/W}$
9	T	Junction to Case QFP80	θ_{JC}	—	—	14	$^{\circ}\text{C/W}$
10	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	3	$^{\circ}\text{C/W}$

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reference Potential Low High	V_{RL} V_{RH}	V_{SSA} $V_{DDA}/2$		$V_{DDA}/2$ V_{DDA}	V V
2	C	Differential Reference Voltage ¹	$V_{RH}-V_{RL}$	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7		28 14	Cycles μs
5	D	ATD 8-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6		26 13	Cycles μs
6	D	Recovery Time ($V_{DDA}=5.0$ Volts)	t_{REC}			20	μs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

A.7 SPI

A.7.1 Master Mode

Figure A-5 and Figure A-6 illustrate the master mode timing. Timing values are shown in Table A-18.

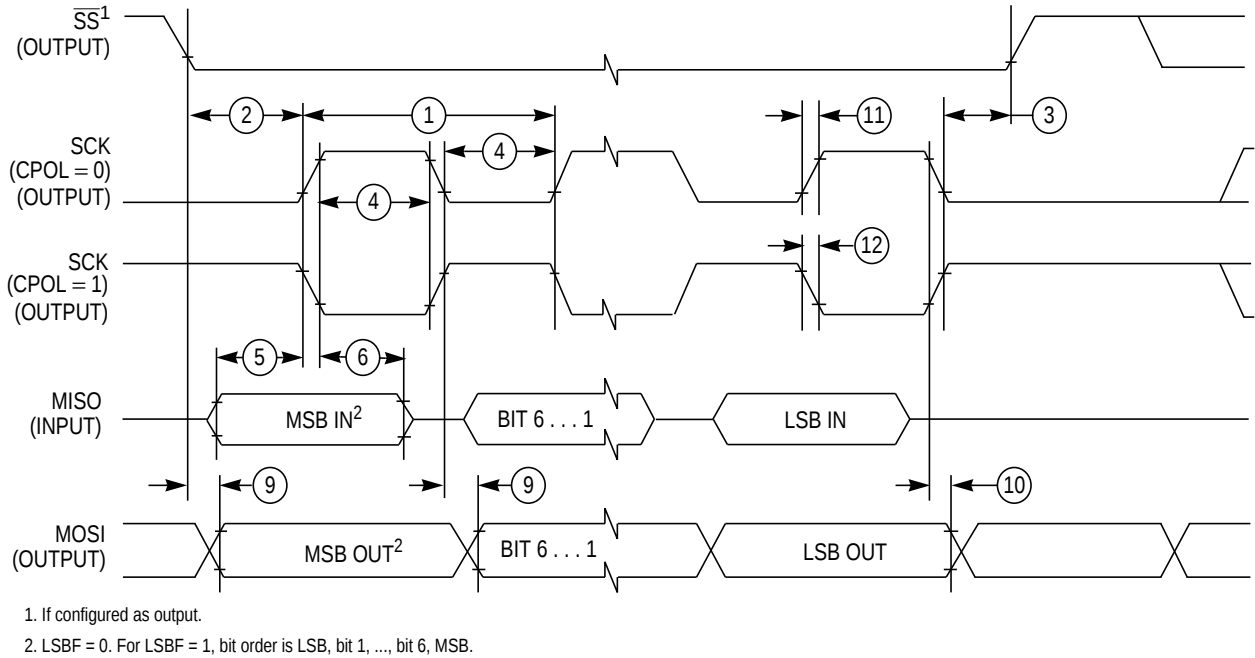


Figure A-5 SPI Master Timing (CPHA = 0)

A.7.2 Slave Mode

Figure A-7 and **Figure A-8** illustrate the slave mode timing. Timing values are shown in **Table A-19**.

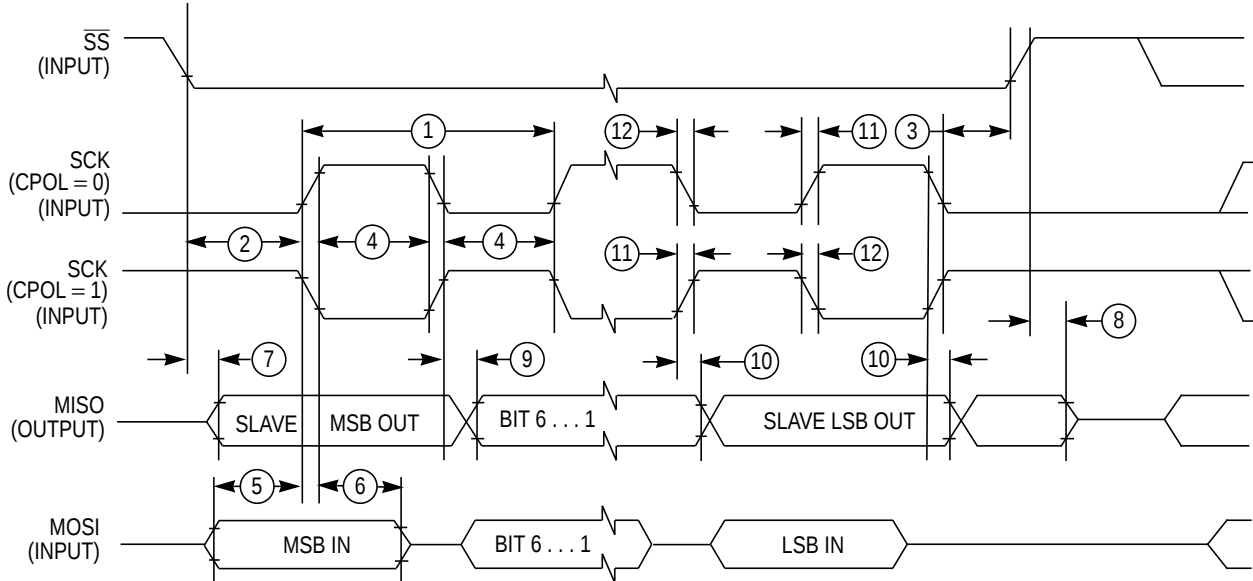


Figure A-7 SPI Slave Timing (CPHA = 0)

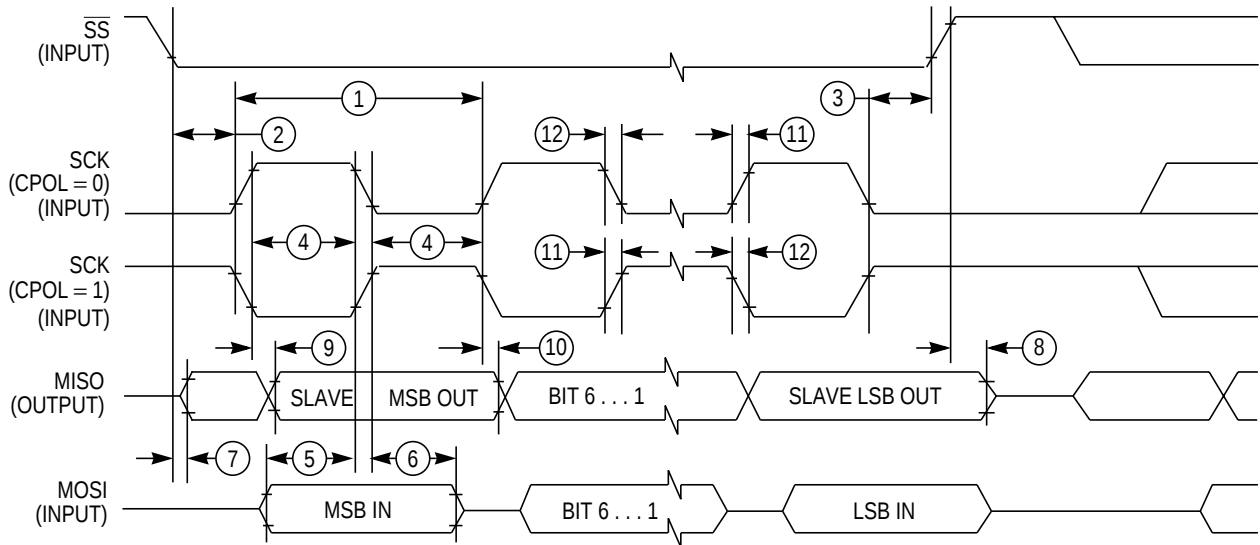


Figure A-8 SPI Slave Timing (CPHA = 1)

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DJ64 and MC9S12D32 packages.

B.2 112-pin LQFP package

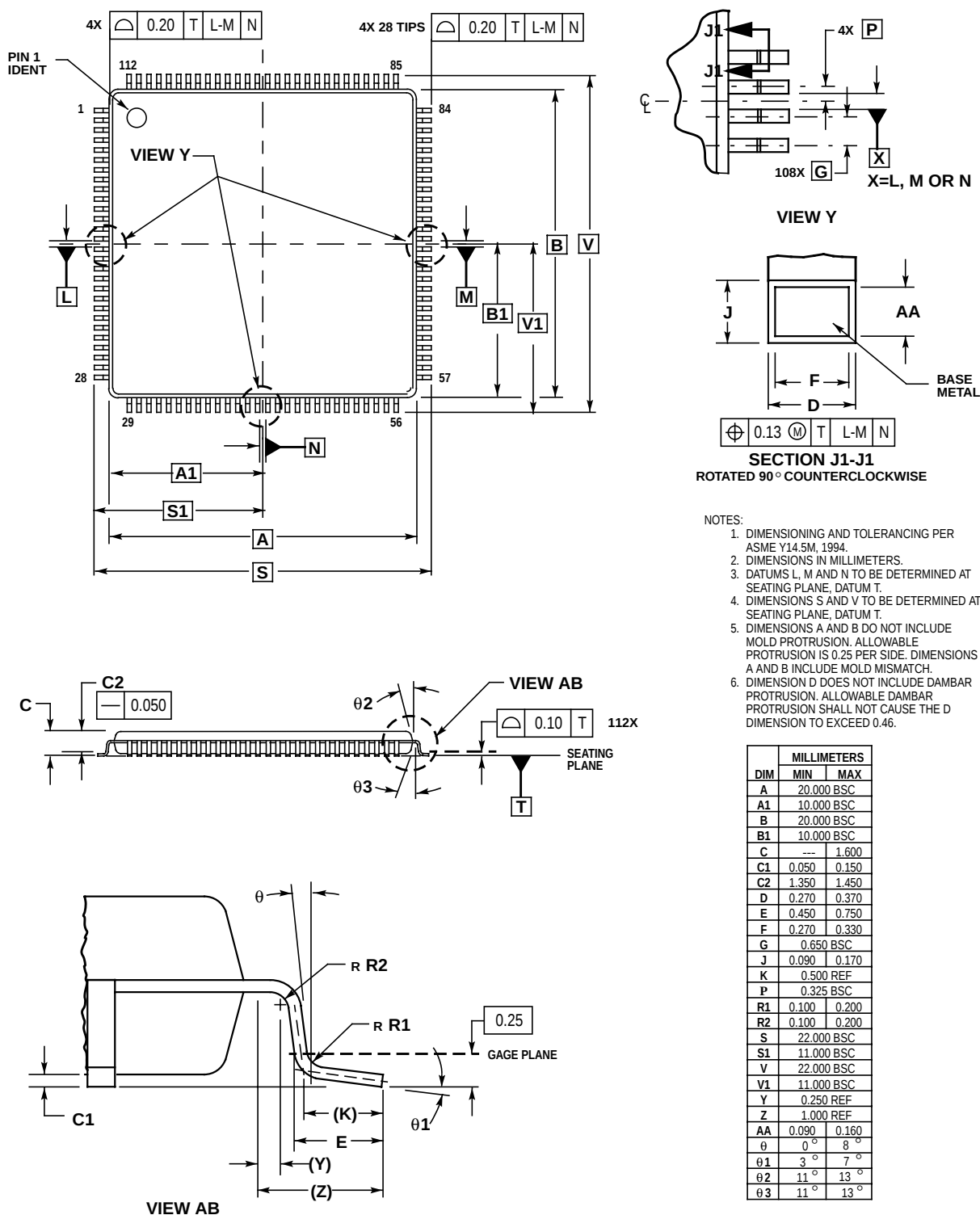


Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)

