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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12dj64vfue

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.06	20 Aug. 2002	20 Aug. 2002		NVM electricals updated Subsection "Detailed Register Map: Address corrections Preface, Table "Document references": added OSC User Guide New section "Oscillator (OSC) Block Description"
V01.07	20 Sept. 2002	20 Sept. 2002		Electrical Characteristics: -> Section "General": removed preliminary disclaimer ->Table "Supply Current Characteristics": changed max Run IDD from 65mA to 50mA changes max Wait IDD from 40mA to 30mA changed max Stop IDD from 50uA to 100uA Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock
V01.08	25 Sept. 2002	25 Sept. 2002		Table "5V I/O Characteristics": Corrected Input Leakage Current to +/- 1 uA Section "Part ID assignment": Located on start of next page for better readability
V01.09	10 Oct. 2002	10 Oct. 2002		Added MC9S12A64 derivative to cover sheet and "Derivative Differences" Table Corrected in footnote of Table "PLL Characteristics": $f_{OSC} = 4\text{MHz}$
V01.10	8 Nov. 2002	8 Nov. 2002		Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0 and/or BDLC Table "ESD and Latch-up Test Conditions": changed pulse numbers from 3 to 1 Table "ESD and Latch-Up Protection Characteristics": changed parameter classification from C to T Table "5V I/O Characteristics": removed foot note from "Input Leakage Current" Table " Supply Current Characteristics": updated Stop and Pseudo Stop currents
V01.11	24 Jan. 2003	24 Jan. 2003		Subsection "Detailed Register Map": Corrected several entries Subsection "Unsecuring the Microcontroller": Added more details Table "Operating Conditions": improved footnote 1 wording, applied footnote 1 to PLL Supply Voltage.
V01.12	31 Mar. 2003	31 Mar. 2003		Tables "SPI Master/Slave Mode Timing Characteristics: Corrected Operating Frequency Appendix 'NVM, Flash and EEPROM': Replaced 'burst programming' by 'row programming' Table "Operating Conditions": corrected minimum bus frequency to 0.25MHz Section "Feature List": ECT features changed to "Four pulse accumulators ..."
V01.13	20 May 2003	20 May 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides Table "Signal Properties" corrected pull resistor reset state for PE7 and PE4-PE2. Table "Absolute Maximum Ratings" corrected footnote on clamp of TEST pin.
V01.14	10 June 2003	10 June 2003		Added cycle definition to "CPU 12 Block Description". Added register reset values to MMC and MEBI block descriptions. Diagram "Clock Connections": Connect Bus Clock to HCS12 Core

2.3.21	PH7 / KWH7 — Port H I/O Pin 7	59
2.3.22	PH6 / KWH6 — Port H I/O Pin 6	60
2.3.23	PH5 / KWH5 — Port H I/O Pin 5	60
2.3.24	PH4 / KWH4 — Port H I/O Pin 2	60
2.3.25	PH3 / KWH3 — Port H I/O Pin 3	60
2.3.26	PH2 / KWH2 — Port H I/O Pin 2	60
2.3.27	PH1 / KWH1 — Port H I/O Pin 1	60
2.3.28	PH0 / KWH0 — Port H I/O Pin 0	60
2.3.29	PJ7 / KWJ7 / SCL / TXCAN0 — PORT J I/O Pin 7	60
2.3.30	PJ6 / KWJ6 / SDA / RXCAN0 — PORT J I/O Pin 6	61
2.3.31	PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]	61
2.3.32	PK7 / ECS / ROMCTL — Port K I/O Pin 7	61
2.3.33	PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]	61
2.3.34	PM7 — Port M I/O Pin 7	61
2.3.35	PM6 — Port M I/O Pin 6	61
2.3.36	PM5 / TXCAN0 / SCK0 — Port M I/O Pin 5	61
2.3.37	PM4 / RXCAN0 / MOSI0 — Port M I/O Pin 4	61
2.3.38	PM3 / TXCAN0 / SS0 — Port M I/O Pin 3	62
2.3.39	PM2 / RXCAN0 / MISO0 — Port M I/O Pin 2	62
2.3.40	PM1 / TXCAN0 / TXB — Port M I/O Pin 1	62
2.3.41	PM0 / RXCAN0 / RXB — Port M I/O Pin 0	62
2.3.42	PP7 / KWP7 / PWM7 — Port P I/O Pin 7	62
2.3.43	PP6 / KWP6 / PWM6 — Port P I/O Pin 6	62
2.3.44	PP5 / KWP5 / PWM5 — Port P I/O Pin 5	62
2.3.45	PP4 / KWP4 / PWM4 — Port P I/O Pin 4	62
2.3.46	PP3 / KWP3 / PWM3 — Port P I/O Pin 3	63
2.3.47	PP2 / KWP2 / PWM2 — Port P I/O Pin 2	63
2.3.48	PP1 / KWP1 / PWM1 — Port P I/O Pin 1	63
2.3.49	PP0 / KWP0 / PWM0 — Port P I/O Pin 0	63
2.3.50	PS7 / SS0 — Port S I/O Pin 7	63
2.3.51	PS6 / SCK0 — Port S I/O Pin 6	63
2.3.52	PS5 / MOSI0 — Port S I/O Pin 5	63
2.3.53	PS4 / MISO0 — Port S I/O Pin 4	63
2.3.54	PS3 / TXD1 — Port S I/O Pin 3	63
2.3.55	PS2 / RXD1 — Port S I/O Pin 2	64
2.3.56	PS1 / TXD0 — Port S I/O Pin 1	64

2.3.57	PS0 / RXD0 — Port S I/O Pin 0	64
2.3.58	PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]	64
2.4	Power Supply Pins	64
2.4.1	VDDX, VSSX — Power & Ground Pins for I/O Drivers	65
2.4.2	VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator 65	
2.4.3	VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins	65
2.4.4	VDDA, VSSA — Power Supply Pins for ATD0/ATD1 and VREG	65
2.4.5	VRH, VRL — ATD Reference Voltage Input Pins	66
2.4.6	VDDPLL, VSSPLL — Power Supply Pins for PLL	66
2.4.7	VREGEN — On Chip Voltage Regulator Enable	66

Section 3 System Clock Description

3.1	Overview.	67
-----	-------------------	----

Section 4 Modes of Operation

4.1	Overview.	69
4.2	Chip Configuration Summary	69
4.3	Security.	70
4.3.1	Securing the Microcontroller	70
4.3.2	Operation of the Secured Microcontroller	70
4.3.3	Unsecuring the Microcontroller	71
4.4	Low Power Modes	71
4.4.1	Stop	71
4.4.2	Pseudo Stop.	71
4.4.3	Wait	71
4.4.4	Run.	72

Section 5 Resets and Interrupts

5.1	Overview.	73
5.2	Vectors	73
5.2.1	Vector Table.	73
5.3	Effects of Reset	74
5.3.1	I/O pins.	74
5.3.2	Memory	75

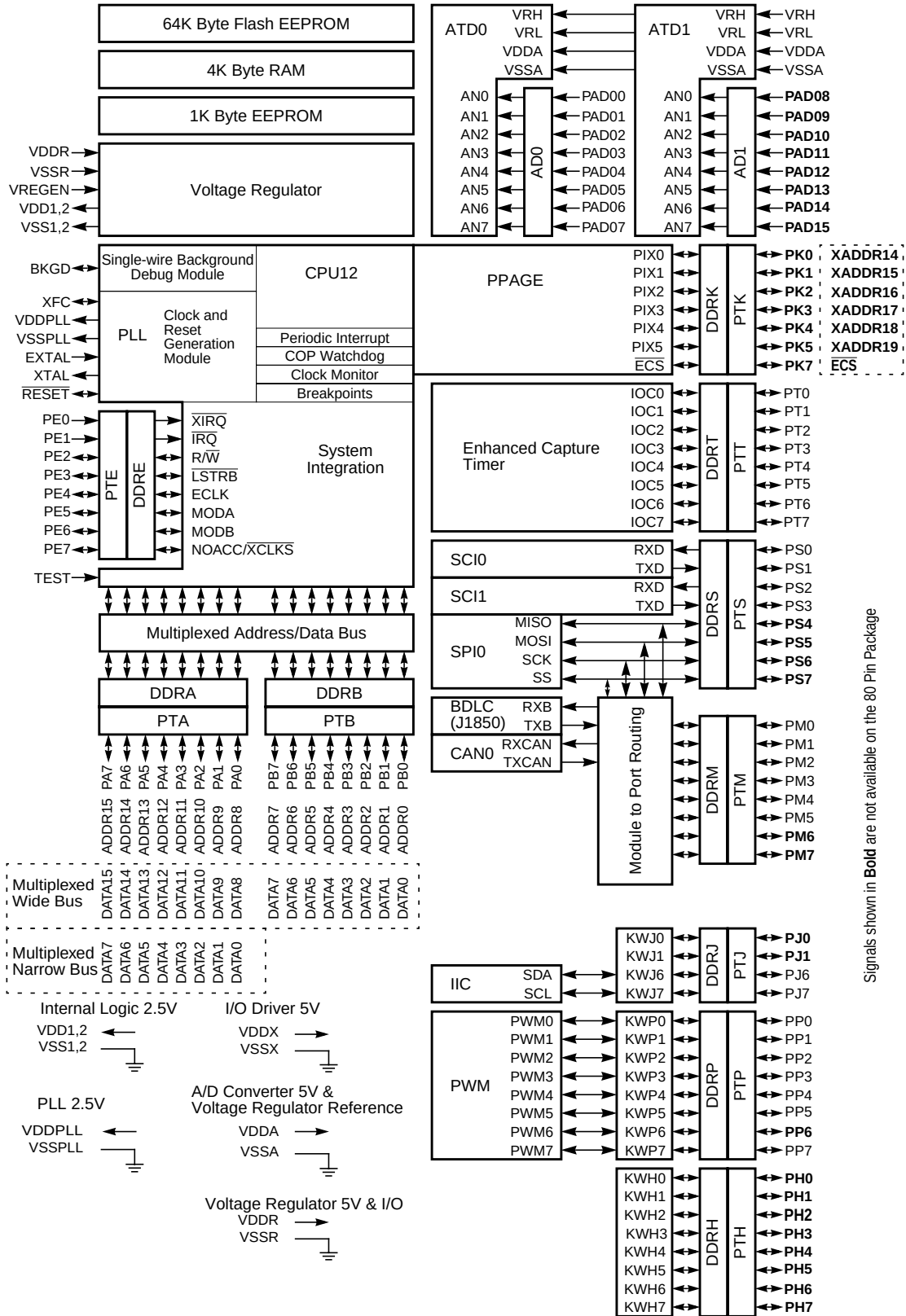
Section 6 HCS12 Core Block Description

Table 0-2 Document References

User Guide	Version	Document Order Number
HCS12 CPU Reference Manual	V02	S12CPUV2/D
HCS12 Module Mapping Control (MMC) Block Guide	V04	S12MMCV4/D
HCS12 Multiplexed External Bus Interface (MEBI) Block Guide	V03	S12MEBIV3/D
HCS12 Interrupt (INT) Block Guide	V01	S12INTV1/D
HCS12 Background Debug (BDM) Block Guide	V04	S12BDMV4/D
HCS12 Breakpoint (BKP) Block Guide	V01	S12BKPV1/D
Clock and Reset Generator (CRG) Block User Guide	V04	S12CRGV4/D
Oscillator (OSC) Block User Guide	V02	S12OSCV2/D
Enhanced Capture Timer 16 Bit 8 Channel (ECT_16B8C) Block User Guide	V01	S12ECT16B8CV1/D
Analog to Digital Converter 10 Bit 8 Channel (ATD_10B8C) Block User Guide	V02	S12ATD10B8CV2/D
Inter IC Bus (IIC) Block User Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block User Guide	V02	S12SCIV2/D
Serial Peripheral Interface (SPI) Block User Guide	V02	S12SPIV2/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide	V01	S12PWM8B8CV1/D
64K Byte Flash (FTS64K) Block User Guide	V01	S12FTS64KV1/D
1K Byte EEPROM (EETS1K) Block User Guide	V01	S12EETS1KV1/D
Byte Level Data Link Controller -J1850 (BDLC) Block User Guide	V01	S12BDLCV1/D
Freescale Scalable CAN (MSCAN) Block User Guide	V02	S12MSCANV2/D
Voltage Regulator (VREG) Block User Guide	V01	S12VREGV1/D
Port Integration Module (PIM_9DJ64) Block User Guide	V01	S12PIM9DJ64V1/D

- 4K byte RAM
- Two 8-channel Analog-to-Digital Converters
 - 10-bit resolution
 - External conversion trigger capability
- 1M bit per second, CAN 2.0 A, B software compatible module
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
- Enhanced Capture Timer
 - 16-bit main counter with 7-bit prescaler
 - 8 programmable input capture or output compare channels
 - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
 - Programmable period and duty cycle
 - 8-bit 8-channel or 16-bit 4-channel
 - Separate control for each pulse width and duty cycle
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
 - Fast emergency shutdown input
 - Usable as interrupt inputs
- Serial interfaces
 - Two asynchronous Serial Communications Interfaces (SCI)
 - Synchronous Serial Peripheral Interface (SPI)
- Byte Data Link Controller (BDLC)
 - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
- Inter-IC Bus (IIC)
 - Compatible with I2C Bus standard
 - Multi-master operation
 - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP or 80 QFP package

Figure 1-1 MC9S12DJ64 Block Diagram



\$0010 - \$0014**MMC map 1 of 4 (HCS12 Module Mapping Control)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0012	INITEE	Read:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		Write:								
\$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
\$0014	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0015 - \$0016**INT map 1 of 2 (HCS12 Interrupt)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
\$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

\$0017 - \$0019**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0017 - \$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$001A - \$001B**Device ID Register (Table 1-4)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
\$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

\$001C - \$001D**MMC map 3 of 4 (HCS12 Module Mapping Control, Table 1-5)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
\$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

\$001E - \$001E**MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

\$0040 - \$007F

ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0063	PACN2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0064	PACN1 (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0065	PACN0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0066	MCCTL	Read:	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
		Write:				ICLAT	FLMC			
\$0067	MCFLG	Read:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
		Write:								
\$0068	ICPAR	Read:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Write:								
\$0069	DLYCT	Read:	0	0	0	0	0	0	DLY1	DLY0
		Write:								
\$006A	ICOVW	Read:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Write:								
\$006B	ICSYS	Read:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
		Write:								
\$006C	Reserved	Read:								
		Write:								
\$006D	TIMTST	Read:	0	0	0	0	0	0	TCBYP	0
	Test Only	Write:								
\$006E	Reserved	Read:								
		Write:								
\$006F	Reserved	Read:								
		Write:								
\$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
\$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
\$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$00E8 - \$00EF**BDLC (Bytelevel Data Link Controller J1850)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00E8	DLCBCR1	Read:	IMSG	CLKS	0	0	0	0	IE	WCM
		Write:								
\$00E9	DLCBSVR	Read:	0	0	I3	I2	I1	I0	0	0
		Write:								
\$00EA	DLCBCR2	Read:	SMRST	DLOOP	RX4XE	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
		Write:								
\$00EB	DLCBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
\$00EC	DLCBARD	Read:	0	RXPOL	0	0	BO3	BO2	BO1	BO0
		Write:								
\$00ED	DLCBRSR	Read:	0	0	R5	R4	R3	R2	R1	R0
		Write:								
\$00EE	DLCSCR	Read:	0	0	0	BDLCE	0	0	0	0
		Write:								
\$00EF	DLCBSTAT	Read:	0	0	0	0	0	0	0	IDLE
		Write:								

\$00F0 - \$00FF**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00F0 - \$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0100 - \$010F**Flash Control Register (fts64k)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
\$0101	FSEC	Read:	KEYEN	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
\$0102	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
		Write:								
\$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
\$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
\$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
\$0107	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0108	FADDRHI	Read:	Bit 14	Bit 14	13	12	11	10	9	Bit 8
		Write:								
\$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$FFCA, \$FFCB	Modulus Down Counter underflow	I-Bit	MCCTL (MCZI)	\$CA
\$FFC8, \$FFC9	Pulse Accumulator B Overflow	I-Bit	PBCTL (PBOVI)	\$C8
\$FFC6, \$FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	\$C6
\$FFC4, \$FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	\$C4
\$FFC2, \$FFC3	BDLC	I-Bit	DLCBCR1 (IE)	\$C2
\$FFC0, \$FFC1	IIC Bus	I-Bit	IBCR (IBIE)	\$C0
\$FFBE, \$FFBF	Reserved	I-Bit	Reserved	\$BE
\$FFBC, \$FFBD		I-Bit		\$BC
\$FFBA, \$FFBB	EEPROM	I-Bit	ECNFG (CCIE, CBEIE)	\$BA
\$FFB8, \$FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	\$B8
\$FFB6, \$FFB7	CAN0 wake-up	I-Bit	CANRIER (WUPIE)	\$B6
\$FFB4, \$FFB5	CAN0 errors	I-Bit	CANRIER (CSCIE, OVRIE)	\$B4
\$FFB2, \$FFB3	CAN0 receive	I-Bit	CANRIER (RXFIE)	\$B2
\$FFB0, \$FFB1	CAN0 transmit	I-Bit	CANTIER (TXEIE2-TXEIE0)	\$B0
\$FFAE, \$FFAF	Reserved	I-Bit	Reserved	\$AE
\$FFAC, \$FFAD		I-Bit		\$AC
\$FFAA, \$FFAB		I-Bit		\$AA
\$FFA8, \$FFA9		I-Bit		\$A8
\$FFA6, \$FFA7		I-Bit		\$A6
\$FFA4, \$FFA5		I-Bit		\$A4
\$FFA2, \$FFA3		I-Bit		\$A2
\$FFA0, \$FFA1		I-Bit		\$A0
\$FF9E, \$FF9F		I-Bit		\$9E
\$FF9C, \$FF9D		I-Bit		\$9C
\$FF9A, \$FF9B		I-Bit		\$9A
\$FF98, \$FF99		I-Bit		\$98
\$FF96, \$FF97		I-Bit		\$96
\$FF94, \$FF95		I-Bit		\$94
\$FF92, \$FF93		I-Bit		\$92
\$FF90, \$FF91		I-Bit		\$90
\$FF8E, \$FF8F	Port P	I-Bit	PIEP (PIEP7-0)	\$8E
\$FF8C, \$FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)	\$8C
\$FF80 to \$FF8B	Reserved			

5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

NOTE: *For devices assembled in 80-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to **Table 2-1** for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For $R_{DS(on)}$ is valid:

$$R_{DS(on)} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DS(on)} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics¹

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB ²	θ_{JA}	—	—	54	$^{\circ}\text{C/W}$
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes ³	θ_{JA}	—	—	41	$^{\circ}\text{C/W}$
3	T	Junction to Board LQFP112	θ_{JB}	—	—	31	$^{\circ}\text{C/W}$
4	T	Junction to Case LQFP112	θ_{JC}	—	—	11	$^{\circ}\text{C/W}$
5	T	Junction to Package Top LQFP112	Ψ_{JT}	—	—	2	$^{\circ}\text{C/W}$
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	$^{\circ}\text{C/W}$
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	$^{\circ}\text{C/W}$
8	T	Junction to Board QFP80	θ_{JB}	—	—	27	$^{\circ}\text{C/W}$
9	T	Junction to Case QFP80	θ_{JC}	—	—	14	$^{\circ}\text{C/W}$
10	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	3	$^{\circ}\text{C/W}$

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reference Potential Low High	V_{RL} V_{RH}	V_{SSA} $V_{DDA}/2$		$V_{DDA}/2$ V_{DDA}	V V
2	C	Differential Reference Voltage ¹	$V_{RH}-V_{RL}$	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7		28 14	Cycles μs
5	D	ATD 8-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6		26 13	Cycles μs
6	D	Recovery Time ($V_{DDA}=5.0$ Volts)	t_{REC}			20	μs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table A-12 NVM Reliability Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Data Retention at an average junction temperature of $T_{Javg} = 85^{\circ}\text{C}^1$	t_{NVMRET}	15			Years
2	C	Flash number of Program/Erase cycles	n_{FLPE}	10,000			Cycles
3	C	EEPROM number of Program/Erase cycles ($-40^{\circ}\text{C} \leq T_J \leq 0^{\circ}\text{C}$)	n_{EEPE}	10,000			Cycles
4	C	EEPROM number of Program/Erase cycles ($0^{\circ}\text{C} < T_J \leq 140^{\circ}\text{C}$)	n_{EEPE}	100,000			Cycles

NOTES:

1. Total time at the maximum guaranteed device operating temperature ≤ 1 year

The phase detector relationship is given by:

$$K_{\Phi} = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (\text{synr} + 1) = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth $f_C=10\text{kHz}$:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_{\Phi}} = 2 \cdot \pi \cdot 50 \cdot 10\text{kHz} / (316.7\text{Hz}/\Omega) = 9.9\text{k}\Omega \approx 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) = 5.19\text{nF} \approx 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \quad C_p = 470\text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock f_{cmp} , the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.

A.7.2 Slave Mode

Figure A-7 and **Figure A-8** illustrate the slave mode timing. Timing values are shown in **Table A-19**.

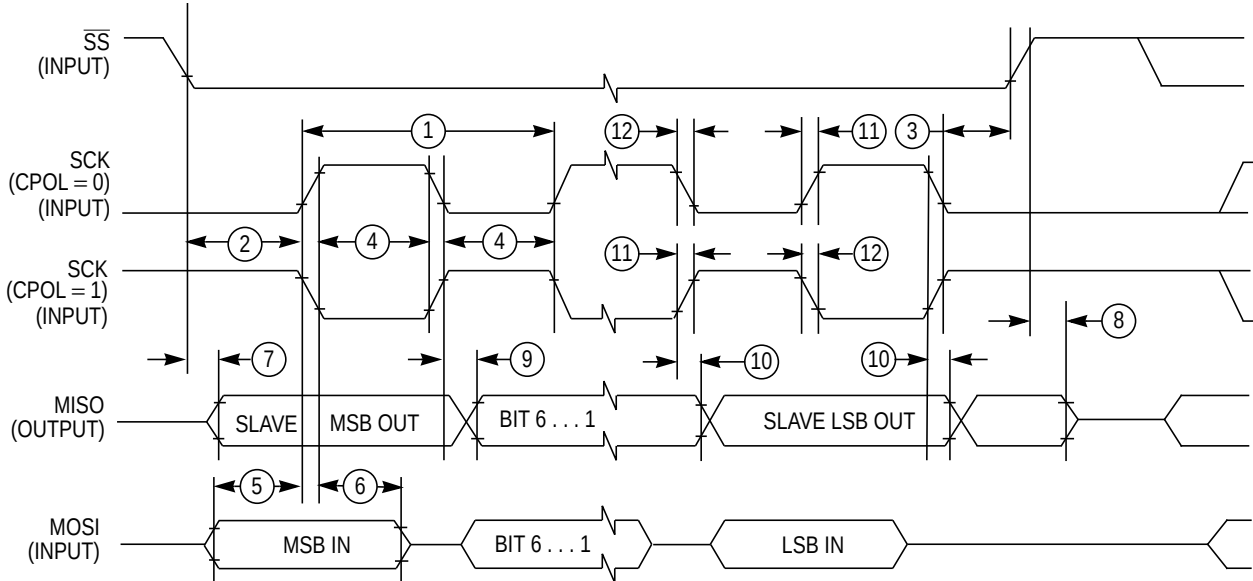


Figure A-7 SPI Slave Timing (CPHA = 0)

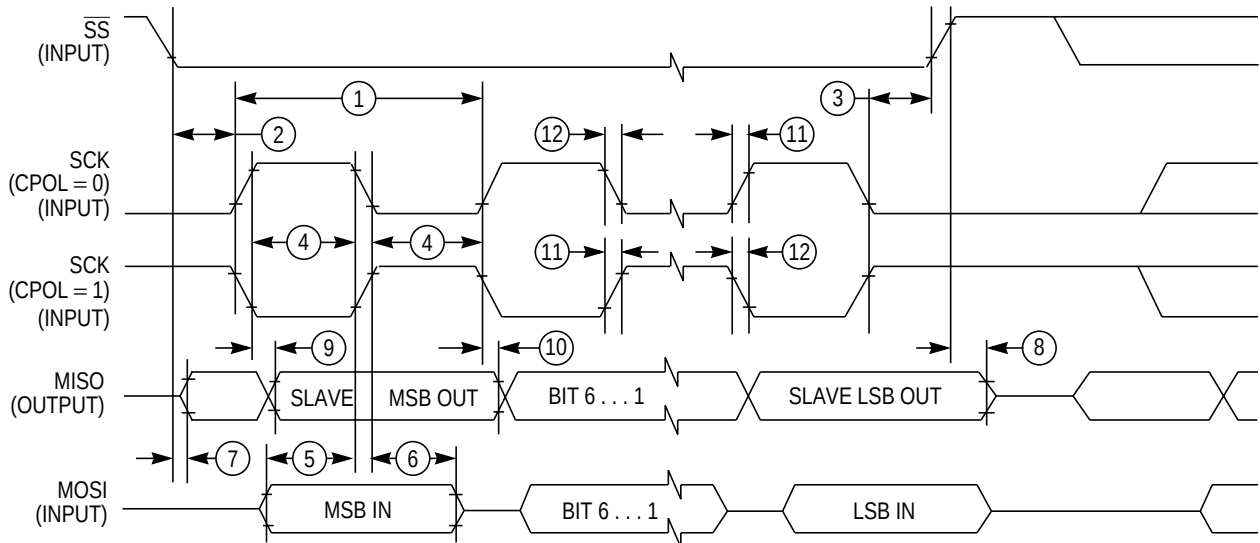


Figure A-8 SPI Slave Timing (CPHA = 1)

B.2 112-pin LQFP package

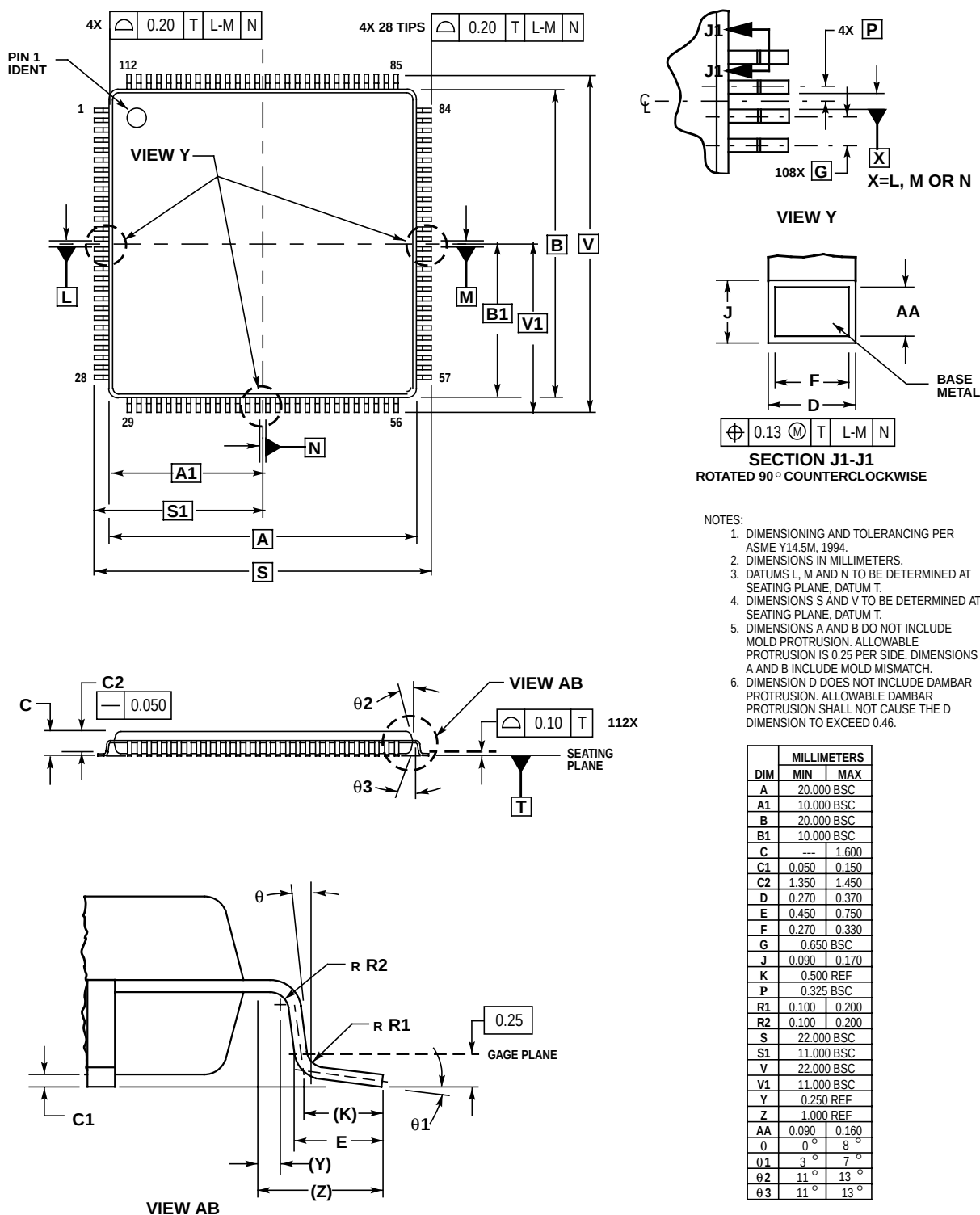


Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)