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Details

Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dj64vpve

- **Ports**
 - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **Table 0-1**).
 - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **Table 0-1**).
 - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DJ64 Block User Guide), if using a derivative without CAN0 (see **Table 0-1**).
- **Pins not available in 80 pin QFP package**
 - **Port H**
In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+\$0262) to \$FF, or enabling the pull resistors by writing a \$FF to the pull enable register (PERH at Base+\$0264).
 - **Port J[1:0]**
Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+\$026C.
 - **Port K**
Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUK = 1 in the register PUCR at Base+\$000C. Therefore care must be taken not to clear this bit.
 - **Port M[7:6]**
PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
 - **Port P6**
PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.
 - **Port S[7:4]**
PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
 - **PAD[15:8] (ATD1 channels)**
Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

Document References

The Device User Guide provides information about the MC9S12DJ64 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block Guides of the implemented modules. In an effort to reduce redundancy all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-2** for names and versions of the referenced documents throughout the Device User Guide.

- 4K byte RAM
- Two 8-channel Analog-to-Digital Converters
 - 10-bit resolution
 - External conversion trigger capability
- 1M bit per second, CAN 2.0 A, B software compatible module
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
- Enhanced Capture Timer
 - 16-bit main counter with 7-bit prescaler
 - 8 programmable input capture or output compare channels
 - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
 - Programmable period and duty cycle
 - 8-bit 8-channel or 16-bit 4-channel
 - Separate control for each pulse width and duty cycle
 - Center-aligned or left-aligned outputs
 - Programmable clock select logic with a wide range of frequencies
 - Fast emergency shutdown input
 - Usable as interrupt inputs
- Serial interfaces
 - Two asynchronous Serial Communications Interfaces (SCI)
 - Synchronous Serial Peripheral Interface (SPI)
- Byte Data Link Controller (BDLC)
 - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
- Inter-IC Bus (IIC)
 - Compatible with I2C Bus standard
 - Multi-master operation
 - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP or 80 QFP package

- I/O lines with 5V input and drive capability
- 5V A/D converter inputs
- Operation at 50MHz equivalent to 25MHz Bus Speed
- Development support
- Single-wire background debug™ mode (BDM)
- On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
 - Normal Single-Chip Mode
 - Normal Expanded Wide Mode
 - Normal Expanded Narrow Mode
 - Emulation Expanded Wide Mode
 - Emulation Expanded Narrow Mode
- Special Operating Modes
 - Special Single-Chip Mode with active Background Debug Mode
 - Special Test Mode (Freescale **use only**)
 - Special Peripheral Mode (Freescale **use only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

Figure 1-1 MC9S12DJ64 Block Diagram

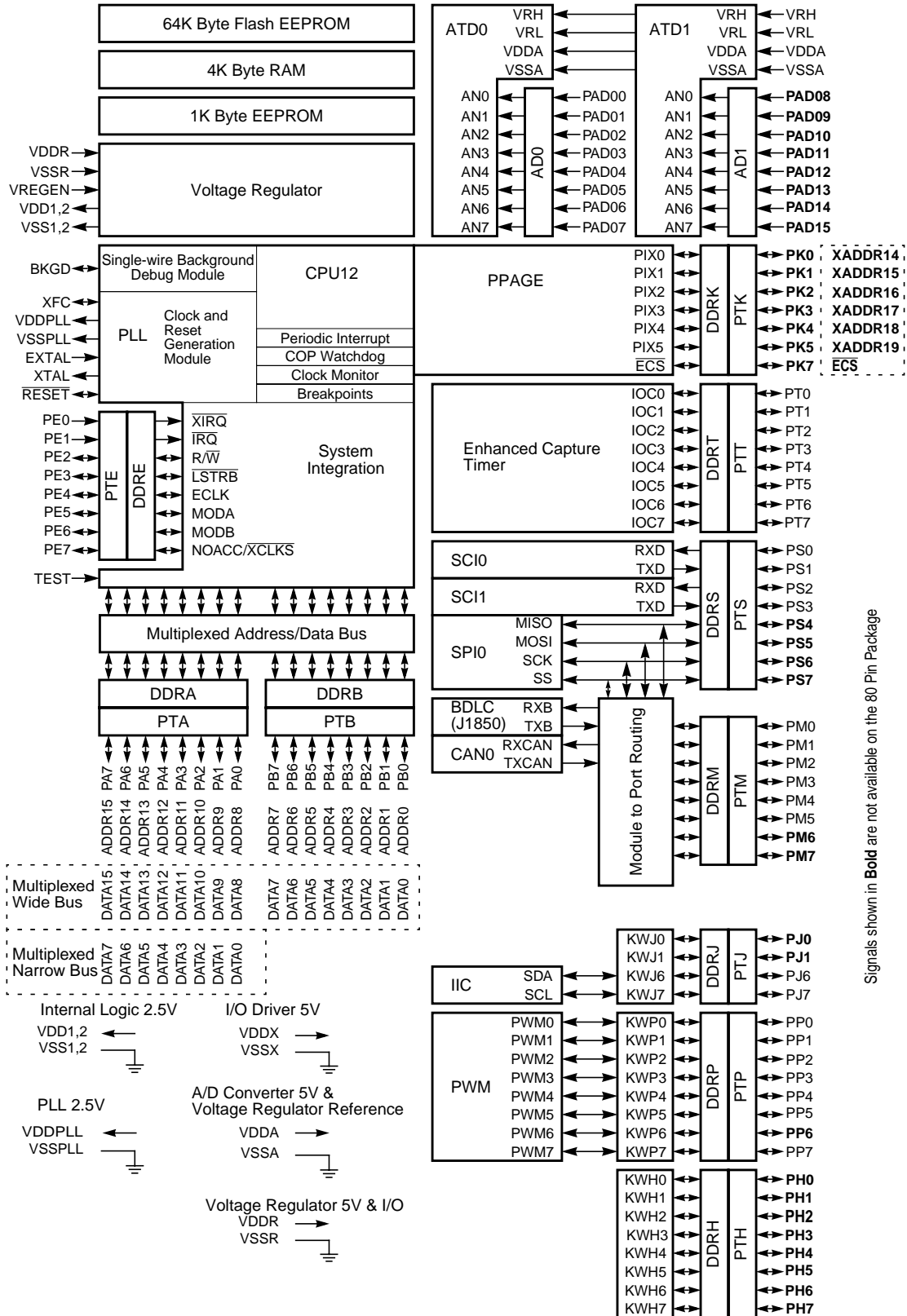
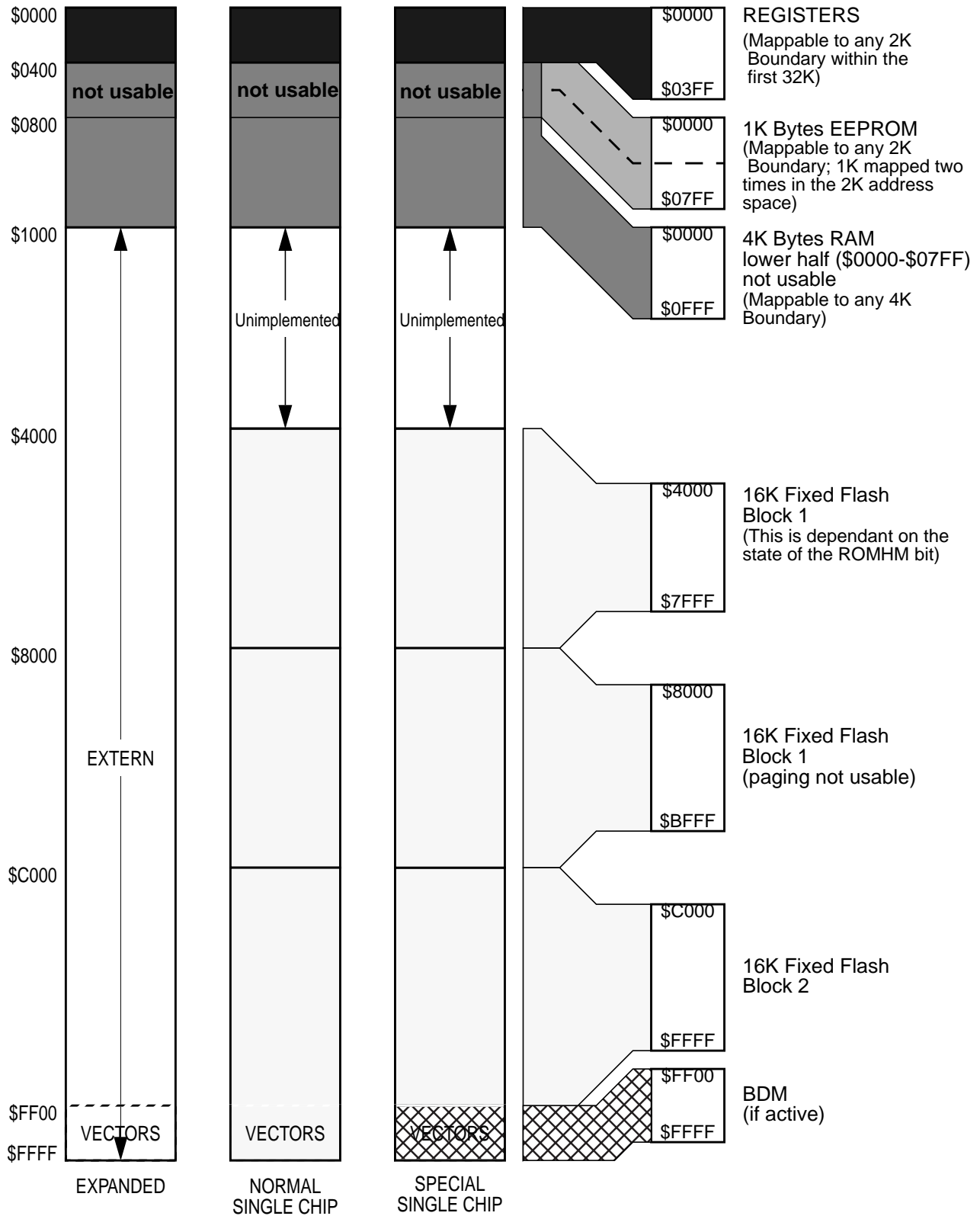


Table 1-1 Device Memory Map for MC9S12DJ64

Address	Module	Size (Bytes)
\$C000 - \$FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at \$FF80 - \$FFFF	16384

Figure 1-3 MC9S12D32 Memory Map out of Reset



\$0040 - \$007F**ECT (Enhanced Capture Timer 16 Bit 8 Channels)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0063	PACN2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0064	PACN1 (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0065	PACN0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0066	MCCTL	Read:	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
		Write:				ICLAT	FLMC			
\$0067	MCFLG	Read:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
		Write:								
\$0068	ICPAR	Read:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Write:								
\$0069	DLYCT	Read:	0	0	0	0	0	0	DLY1	DLY0
		Write:								
\$006A	ICOVW	Read:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Write:								
\$006B	ICSYS	Read:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
		Write:								
\$006C	Reserved	Read:								
		Write:								
\$006D	TIMTST	Read:	0	0	0	0	0	0	TCBYP	0
	Test Only	Write:								
\$006E	Reserved	Read:								
		Write:								
\$006F	Reserved	Read:								
		Write:								
\$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
\$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
\$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$00D0 - \$00D7**SCI1 (Asynchronous Serial Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00D5	SCI1SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
\$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
\$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

\$00D8 - \$00DF**SPI0 (Serial Peripheral Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00D8	SPI0CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
\$00D9	SPI0CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
\$00DA	SPI0BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
\$00DB	SPI0SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
\$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00DD	SPI0DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
\$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$00E0 - \$00E7**IIC (Inter IC Bus)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
\$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
\$00E2	IBCR	Read:	IBEN	IBIE	MS/SL	TX/RX	TXAK	0	0	IBSWAI
		Write:						RSTA		
\$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
\$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
\$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0120 - \$013F**ATD1 (Analog to Digital Converter 10 Bit 8 Channel)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0139	ATD1DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013A	ATD1DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013B	ATD1DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013C	ATD1DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013D	ATD1DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
\$013E	ATD1DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
\$013F	ATD1DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

\$0140 - \$017F**CAN0 (Freescale Scalable CAN - FSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses \$001A and \$001B after reset). The read-only value is a unique part ID for each revision of the chip. **Table 1-4** shows the assigned part ID number.

Table 1-4 Assigned Part ID Numbers

Device	Mask Set Number	Part ID ¹
MC9S12DJ64	0L86D	\$0200
MC9S12DJ64	1L86D	\$0201
MC9S12DJ64	2L86D	\$0201 ²
MC9S12DJ64	3L86D	\$0203
MC9S12DJ64	4L86D	\$0204
MC9S12DJ64	0M89C	\$0204

NOTES:

1. The coding is as follows:

Bit 15-12: Major family identifier

Bit 11-8: Minor family identifier

Bit 7-4: Major mask set revision number including FAB transfers

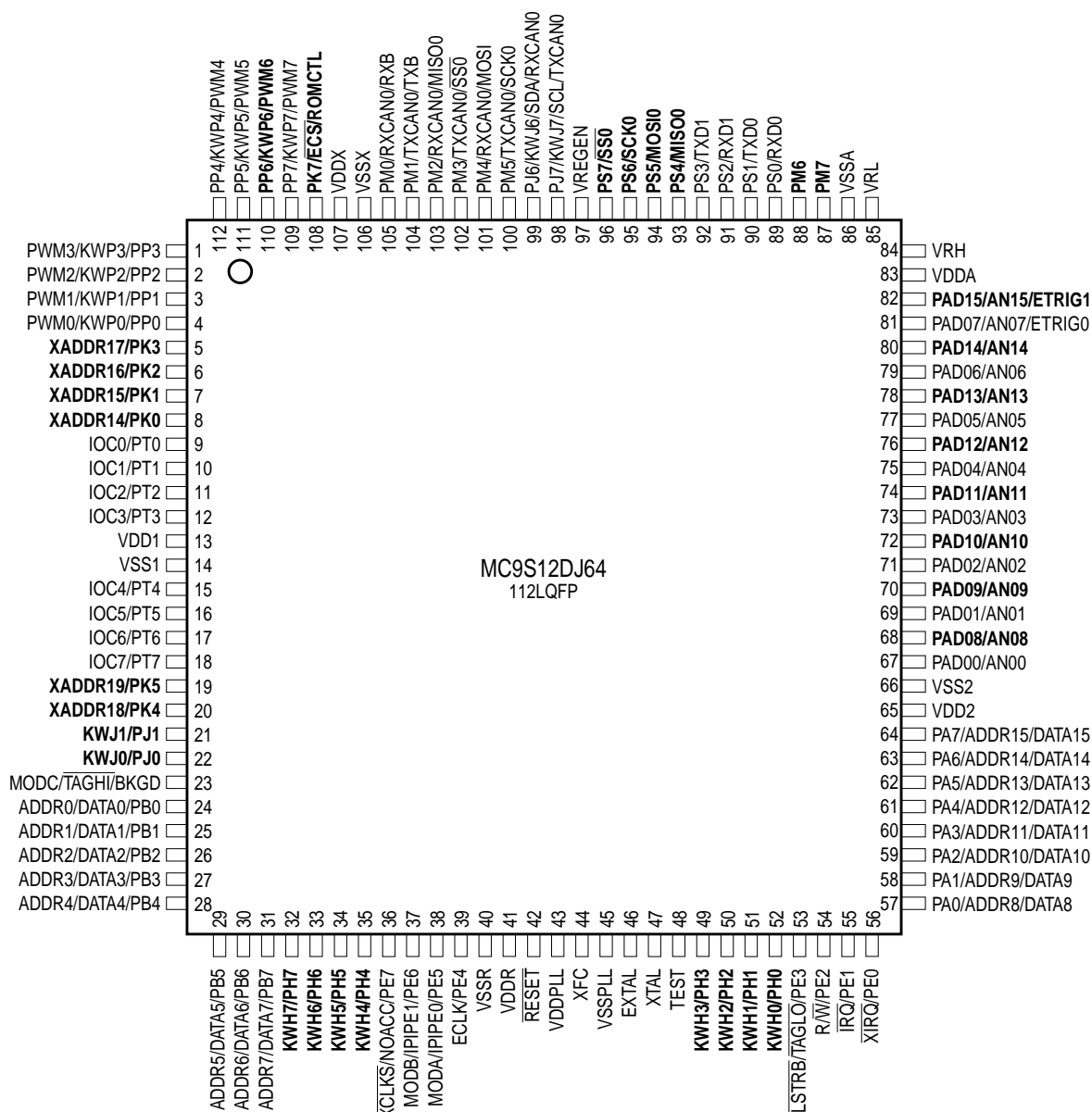
Bit 3-0: Minor - non full - mask set revision

2. 1L86D is identical to 2L86D except improved ESD performance on 2L86D

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses \$001C and \$001D after reset). **Table 1-5** shows the read-only values of these registers. Refer to HCS12 Module Mapping Control (MMC) Block Guide for further details.

Table 1-5 Memory size registers

Register name	Value
MEMSIZ0	\$11
MEMSIZ1	\$80



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 2-1 Pin Assignments in 112-pin LQFP for MC9S12DJ64

2.3.14 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.15 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.16 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.3.17 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

2.3.18 PE2 / $\text{R}/\overline{\text{W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.3.19 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.20 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.21 PH7 / KWH7 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.55 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.56 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.57 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.58 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

2.4 Power Supply Pins

MC9S12DJ64 power and ground pins are described below.

NOTE: All VSS pins must be connected together in the application.

Table 2-2 MC9S12DJ64 Power and Ground Connection Summary

Mnemonic	Pin Number	Nominal Voltage	Description
	112-pin QFP		
VDD1, 2	13, 65	2.5V	Internal power and ground generated by internal regulator
VSS1, 2	14, 66	0V	
VDDR	41	5.0V	External power and ground, supply to pin drivers and internal voltage regulator.
VSSR	40	0V	
VDDX	107	5.0V	External power and ground, supply to pin drivers.
VSSX	106	0V	
VDDA	83	5.0V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	86	0V	
VRL	85	0V	Reference voltages for the analog-to-digital converter.
VRH	84	5.0V	

Consult the FTS64K Block User Guide for information about the flash module.

The "S12 LRAE" is a generic Load RAM and Execute (LRAE) program which will be programmed into the flash memory of this device during manufacture. This LRAE program will provide greater programming flexibility to the end users by allowing the device to be programmed directly using CAN or SCI after it is assembled on the PCB. Use of the LRAE program is at the discretion of the end user and, if not required, it must simply be erased prior to flash programming. For more details of the S12 LRAE and its implementation, please see the S12 LREA Application Note (AN2546/D).

It is planned that most HC9S12 devices manufactured after Q1 of 2004 will be shipped with the S12 LRAE programmed in the Flash. Exact details of the changeover (ie blank to programmed) for each product will be communicated in advance via GPCN and will be traceable by the customer via datecode marking on the device.

Please contact Freescale SPS Sales if you have any additional questions.

Section 17 EEPROM 1K Block Description

Consult the EETS1K Block User Guide for information about the EEPROM module.

Section 18 RAM Block Description

This module supports single-cycle misaligned word accesses.

Section 19 MSCAN Block Description

Consult the MSCAN Block User Guide for information about the Freescale Scalable CAN Module.

Section 20 Port Integration Module (PIM) Block Description

Consult the PIM_9DJ64 Block User Guide for information about the Port Integration Module.

Section 21 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

Section 22 Printed Circuit Board Layout Proposals

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins. VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins. The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5} , the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage $\leq 1\text{LSB}$, then the external filter capacitor, $C_f \geq 1024 * (C_{\text{INS}} - C_{\text{INN}})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of \$3FF (\$FF in 8-bit mode) for analog inputs greater than V_{RH} and \$000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as $V_{\text{ERR}} = K * R_S * I_{\text{INJ}}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-9 ATD Electrical Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Max input Source Resistance	R_S	-	-	1	K Ω
2	T	Total Input Capacitance Non Sampling Sampling	C_{INN} C_{INS}			10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

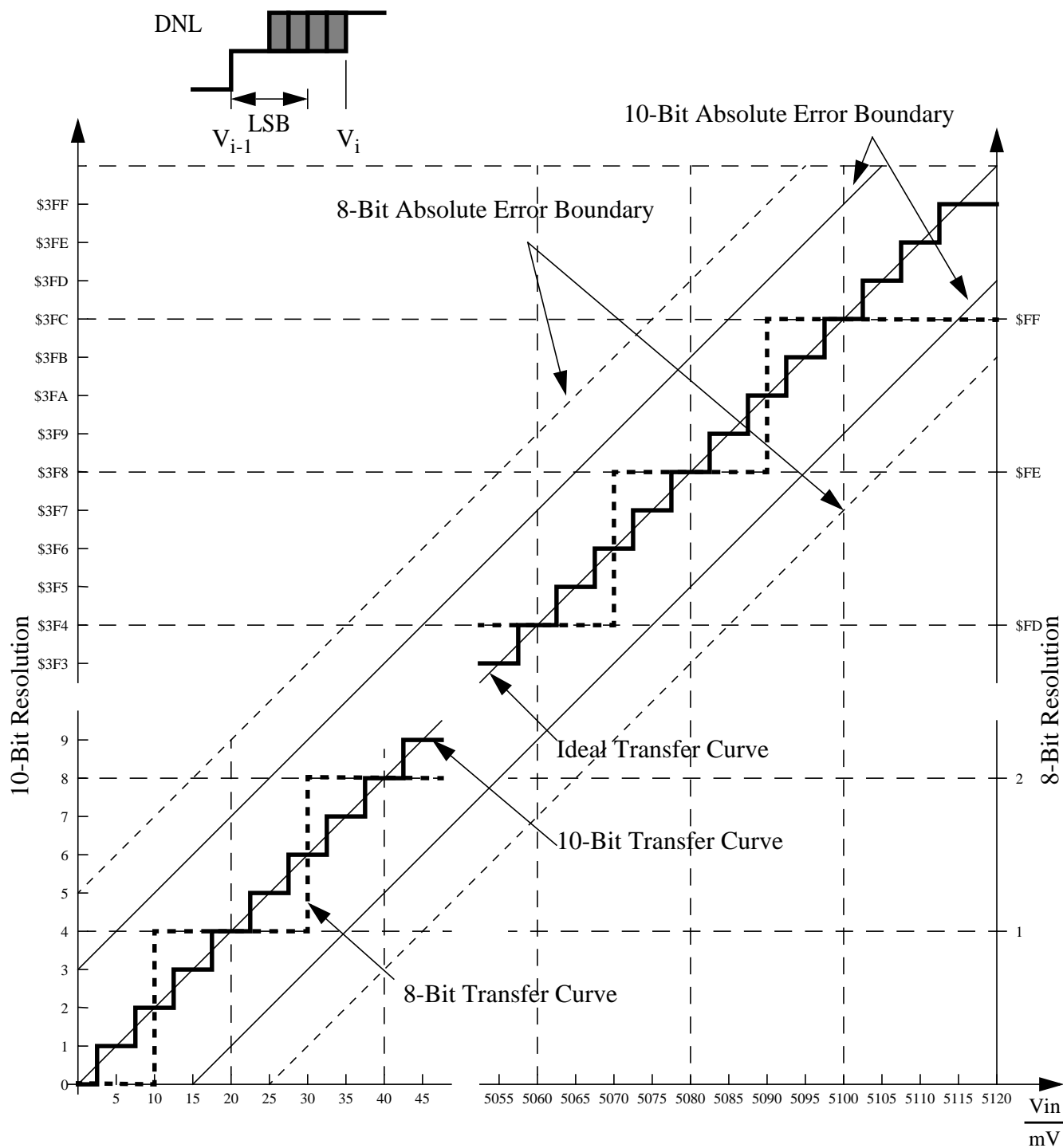


Figure A-1 ATD Accuracy Definitions

NOTE: Figure A-1 shows only definitions, for specification values refer to Table A-10.

A.7 SPI

A.7.1 Master Mode

Figure A-5 and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-18**.

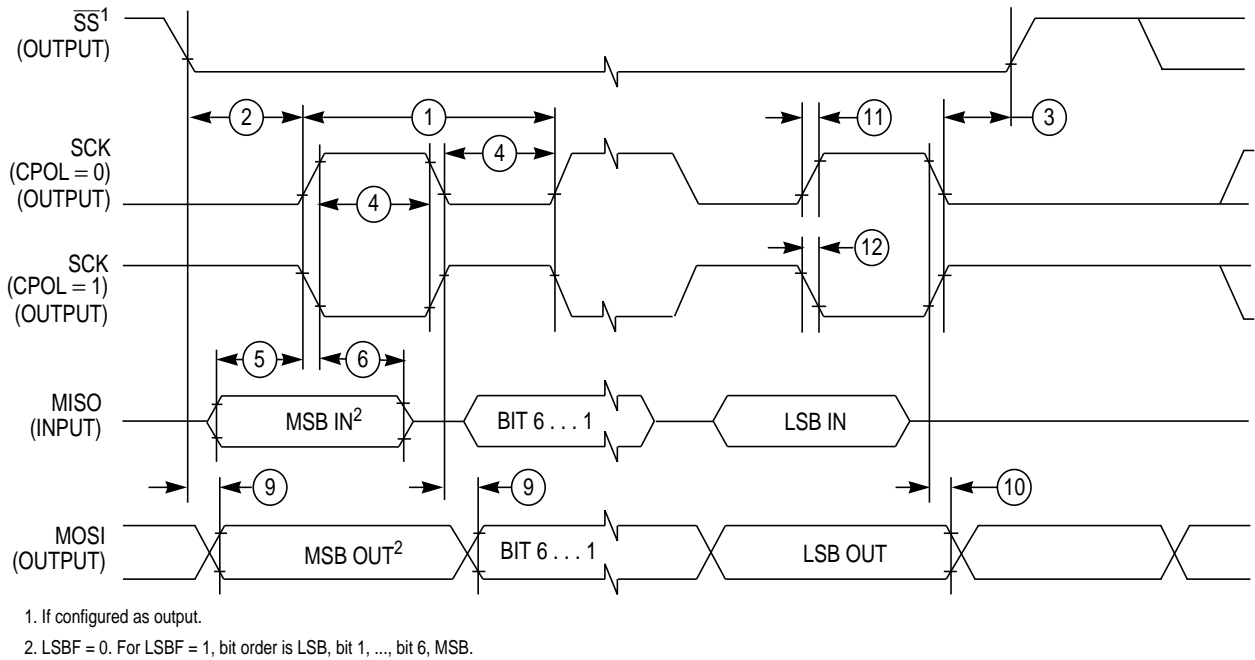


Figure A-5 SPI Master Timing (CPHA = 0)