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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12dg12f1cpver

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.06	20 Aug. 2002	20 Aug. 2002		NVM electricals updated Subsection "Detailed Register Map: Address corrections Preface, Table "Document references": added OSC User Guide New section "Oscillator (OSC) Block Description"
V01.07	20 Sept. 2002	20 Sept. 2002		Electrical Characteristics: -> Section "General": removed preliminary disclaimer ->Table "Supply Current Characteristics": changed max Run IDD from 65mA to 50mA changes max Wait IDD from 40mA to 30mA changed max Stop IDD from 50uA to 100uA Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock
V01.08	25 Sept. 2002	25 Sept. 2002		Table "5V I/O Characteristics": Corrected Input Leakage Current to +/- 1 uA Section "Part ID assignment": Located on start of next page for better readability
V01.09	10 Oct. 2002	10 Oct. 2002		Added MC9S12A64 derivative to cover sheet and "Derivative Differences" Table Corrected in footnote of Table "PLL Characteristics": f_{OSC} = 4MHz
V01.10	8 Nov. 2002	8 Nov. 2002		Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0 and/or BDLC Table "ESD and Latch-up Test Conditions": changed pulse numbers from 3 to 1 Table "ESD and Latch-Up Protection Characteristics": changed parameter classification from C to T Table "5V I/O Characteristics": removed foot note from "Input Leakage Current" Table " Supply Current Characteristics": updated Stop and Pseudo Stop currents
V01.11	24 Jan. 2003	24 Jan. 2003		Subsection "Detailed Register Map": Corrected several entries Subsection "Unsecuring the Microcontroller": Added more details Table "Operating Conditions": improved footnote 1 wording, applied footnote 1 to PLL Supply Voltage.
V01.12	31 Mar. 2003	31 Mar. 2003		Tables "SPI Master/Slave Mode Timing Characteristics: Corrected Operating Frequency Appendix 'NVM, Flash and EEPROM': Replaced 'burst programming' by 'row programming Table "Operating Conditions": corrected minimum bus frequency to 0.25MHz Section "Feature List": ECT features changed to "Four pulse accumulators ..."
V01.13	20 May 2003	20 May 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides Table "Signal Properties" corrected pull resistor reset state for PE7 and PE4-PE2. Table "Absolute Maximum Ratings" corrected footnote on clamp of TEST pin.
V01.14	10 June 2003	10 June 2003		Added cycle definition to "CPU 12 Block Description". Added register reset values to MMC and MEBI block descriptions. Diagram "Clock Connections": Connect Bus Clock to HCS12 Core

Derivative Differences and Document References

Derivative Differences

Table 0-1 shows the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Derivative Differences

Generic device	MC9S12DJ64	MC9S12D64	MC9S12A64	MC9S12D32	MC9S12A32
CAN0	1	1	0	1	0
J1850/BDLC	1	0	0	0	0
Packages	112LQFP, 80QFP	112LQFP, 80QFP	112LQFP, 80QFP	80QFP	80QFP
Mask Set	L86D	L86D	L86D	L86D	L86D
Temp Options	M, V, C	M, V, C	C	M, V, C	C
Package Codes	PV, FU	PV, FU	PV, FU	FU	FU
Note	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office	An errata exists contact Sales office

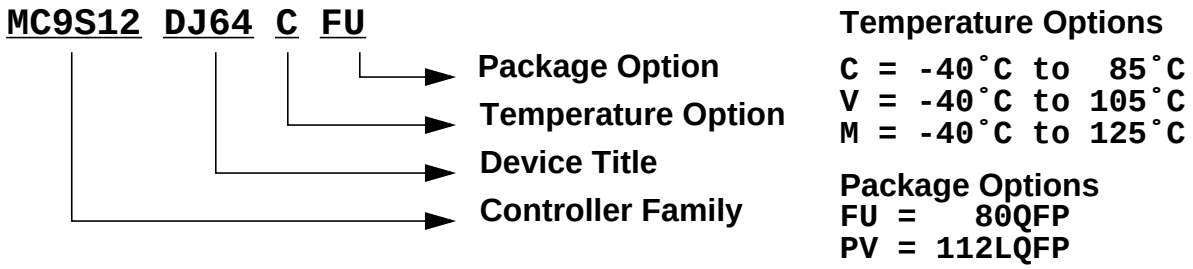


Figure 0-1 Order Partnumber Example

The following items should be considered when using a derivative.

- **Registers**
  - Do not write or read CAN0 registers (after reset: address range $0140 - $017F), if using a derivative without CAN0 (see **Table 0-1**).
  - Do not write or read BDLC registers (after reset: address range $00E8 - $00EF), if using a derivative without BDLC (see **Table 0-1**).
- **Interrupts**
  - Fill the four CAN0 interrupt vectors ($FFB0 - $FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0 (see **Table 0-1**).
  - Fill the BDLC interrupt vector ($FFC2, $FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **Table 0-1**).

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DJ64 device.

$0040 - $007F ECT (Enhanced Capture Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0063	PACN2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0064	PACN1 (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0065	PACN0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0066	MCCTL	Read:	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
		Write:				ICLAT	FLMC			
$0067	MCFLG	Read:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
		Write:								
$0068	ICPAR	Read:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Write:								
$0069	DLYCT	Read:	0	0	0	0	0	0	DLY1	DLY0
		Write:								
$006A	ICOVW	Read:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Write:								
$006B	ICSYS	Read:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
		Write:								
$006C	Reserved	Read:								
		Write:								
$006D	TIMTST Test Only	Read:	0	0	0	0	0	0	TCBYP	0
		Write:								
$006E	Reserved	Read:								
		Write:								
$006F	Reserved	Read:								
		Write:								
$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0100 - $010F Flash Control Register (fts64k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$010A	FDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$010B	FDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010C - $010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B EEPROM Control Register (eets1k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0112	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0117	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	0	0	Bit 8
		Write:								
$0119	EADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$011A	EDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$011B	EDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$011C - $011F Reserved for RAM Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$011C - $011F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0240 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$024A	DDRS	Read:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
$024B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
$024C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
$024D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
$024E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								
$0253	RDRM	Read:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		Write:								
$0254	PERM	Read:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
$0255	PPSM	Read:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
$0256	WOMM	Read:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
$0257	MODRR	Read:	0	0	0	MODRR4	0	0	MODRR1	MODRR0
		Write:								
$0258	PTP	Read:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0259	PTIP	Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$025B	RDRP	Read:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$025C	PERP	Read:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$025D	PPSP	Read:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$025E	PIEP	Read:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
		Write:								
$025F	PIFP	Read:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
		Write:								
$0260	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0261	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0262	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								

2.3.14 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.15 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.16 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.3.17 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

2.3.18 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.3.19 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.20 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.21 PH7 / KWH7 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.30 PJ6 / KWJ6 / SDA / RXCAN0 — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial data pin SDA of the IIC module. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0).

2.3.31 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.32 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit. For a complete list of modes refer to **4.2 Chip Configuration Summary**.

2.3.33 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

2.3.34 PM7 — Port M I/O Pin 7

PM7 is a general purpose input or output pin.

2.3.35 PM6 — Port M I/O Pin 6

PM6 is a general purpose input or output pin.

2.3.36 PM5 / TXCAN0 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.37 PM4 / RXCAN0 / MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Freescale Scalable Controller Area Network controller 0 (CAN0). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12DJ64 and MC9S12D32. Each mode has an associated default memory map and external bus configuration.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PK7 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	0	1	Emulation Expanded Narrow, BDM allowed
			1	0	
0	1	0	X	0	Special Test (Expanded Wide), BDM allowed
0	1	1	0	1	Emulation Expanded Wide, BDM allowed
			1	0	
1	0	0	X	1	Normal Single Chip, BDM allowed
1	0	1	0	0	Normal Expanded Narrow, BDM allowed
			1	1	
1	1	0	X	1	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal Expanded Wide, BDM allowed
			1	1	

For further explanation on the modes refer to the HCS12 Multiplexed External Bus Interface Block Guide.

Table 4-2 Clock Selection Based on PE7

PE7 = $\overline{\text{XCLKS}}$	Description
1	Colpitts Oscillator selected

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

$FFCA, $FFCB	Modulus Down Counter underflow	I-Bit	MCCTL (MCZI)	$CA
$FFC8, $FFC9	Pulse Accumulator B Overflow	I-Bit	PBCTL (PBOVI)	$C8
$FFC6, $FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	$C4
$FFC2, $FFC3	BDLC	I-Bit	DLCBCR1 (IE)	$C2
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBE, $FFBF	Reserved	I-Bit	Reserved	$BE
$FFBC, $FFBD		I-Bit		$BC
$FFBA, $FFBB	EEPROM	I-Bit	ECNFG (CCIE, CBEIE)	$BA
$FFB8, $FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	$B8
$FFB6, $FFB7	CAN0 wake-up	I-Bit	CANRIER (WUPIE)	$B6
$FFB4, $FFB5	CAN0 errors	I-Bit	CANRIER (CSCIE, OVRIE)	$B4
$FFB2, $FFB3	CAN0 receive	I-Bit	CANRIER (RXFIE)	$B2
$FFB0, $FFB1	CAN0 transmit	I-Bit	CANTIER (TXEIE2-TXEIE0)	$B0
$FFAE, $FFAF	Reserved	I-Bit	Reserved	$AE
$FFAC, $FFAD		I-Bit		$AC
$FFAA, $FFAB		I-Bit		$AA
$FFA8, $FFA9		I-Bit		$A8
$FFA6, $FFA7		I-Bit		$A6
$FFA4, $FFA5		I-Bit		$A4
$FFA2, $FFA3		I-Bit		$A2
$FFA0, $FFA1		I-Bit		$A0
$FF9E, $FF9F		I-Bit		$9E
$FF9C, $FF9D		I-Bit		$9C
$FF9A, $FF9B		I-Bit		$9A
$FF98, $FF99		I-Bit		$98
$FF96, $FF97		I-Bit		$96
$FF94, $FF95		I-Bit		$94
$FF92, $FF93		I-Bit		$92
$FF90, $FF91		I-Bit		$90
$FF8E, $FF8F	Port P	I-Bit	PIEP (PIEP7-0)	$8E
$FF8C, $FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)	$8C
$FF80 to $FF8B	Reserved			

5.3 Effects of Reset

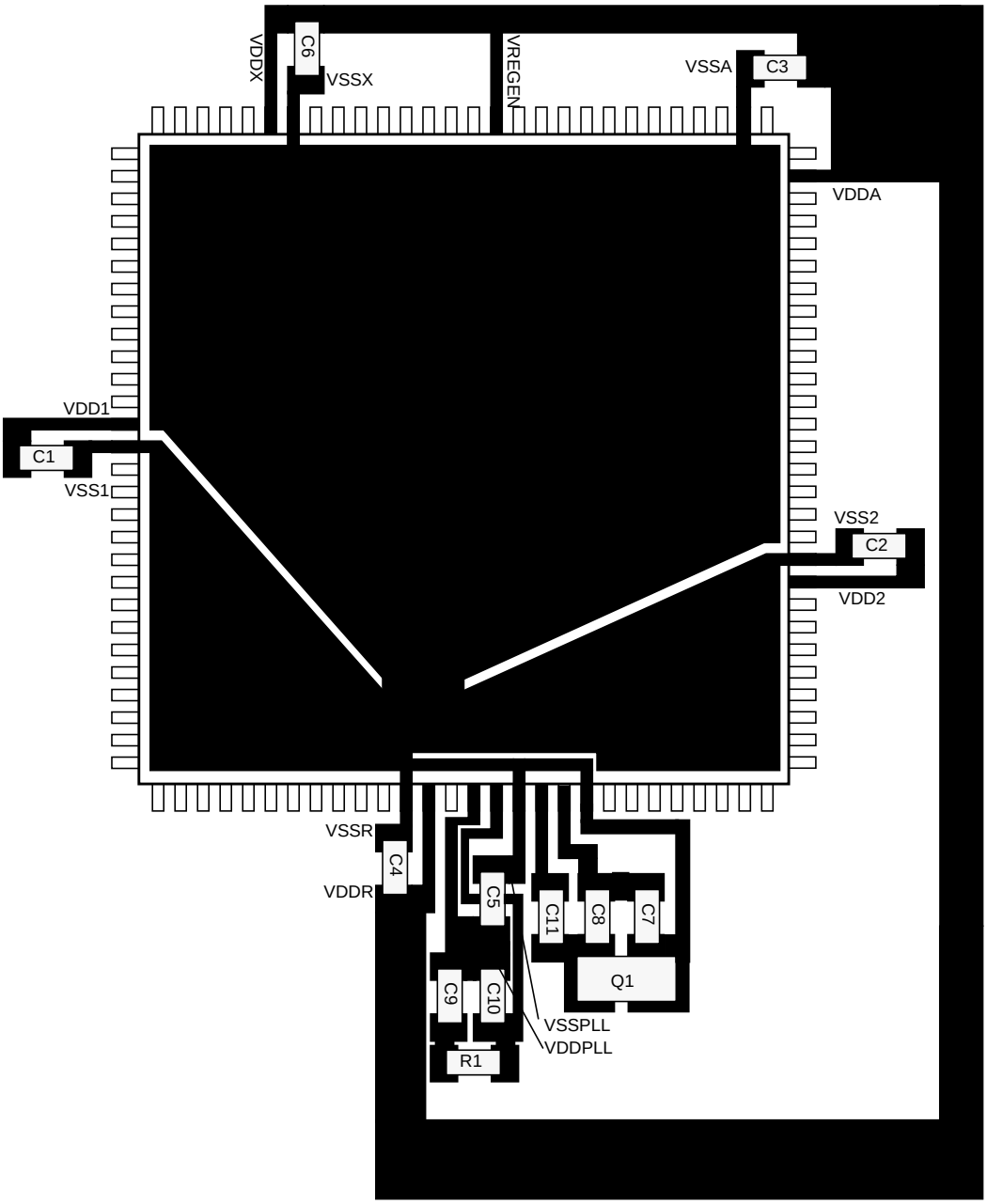
When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Multiplexed External Bus Interface (MEBI) Block Guide for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

Figure 22-1 Recommended PCB Layout 112LQFP Colpitts Oscillator



NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to* ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	4.5	5	5.25	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage [1]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator	f_{osc}	0.5	-	16	MHz
Bus Frequency	f_{bus}	0.25[2]	-	25	MHz
MC9S12DJ64**C** Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	85	°C
MC9S12DJ64**V** Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	105	°C
MC9S12DJ64**M** Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range [3]	T_A	-40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.
3. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			50	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled [1]	I_{DDW}			30 5	mA
3	 C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) [1, 2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		 370 400 450 550 600 650 800 850 1200	 500 1600 2100 5000	µA
4	 C C C C C C C	Pseudo Stop Current (RTI and COP enabled) [1, 2] -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		 570 600 650 750 850 1200 1500		µA
5	 C P C C P C P C P	Stop Current [2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		 12 25 100 130 160 200 350 400 600	 100 1200 1700 5000	µA

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}-V_{RL}	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=5.0 Volts)	t_{REC}			20	µs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

NOTES:
1. Depending on the crystal a damping series resistor might be necessary
2. f_{osc} = 4MHz, C = 22pF.
3. Maximum value is for extreme cases using high Q, low frequency crystals
4. Only valid if Pierce oscillator/external clock mode is selected

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

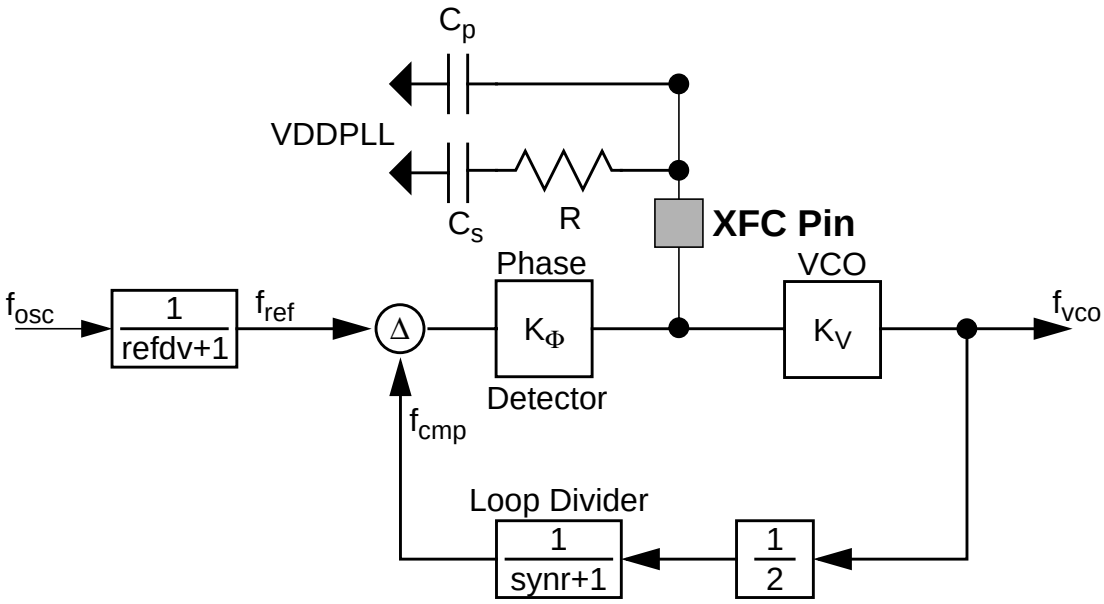


Figure A-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-16**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

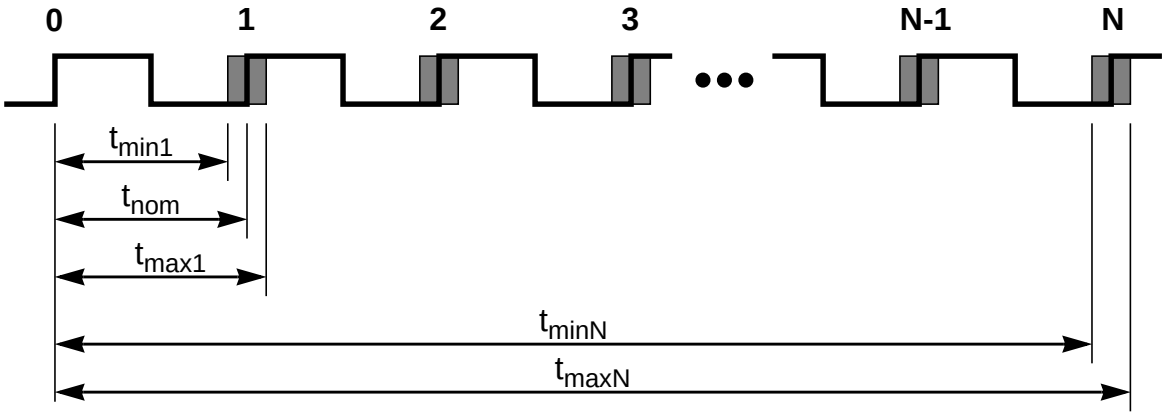


Figure A-3 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

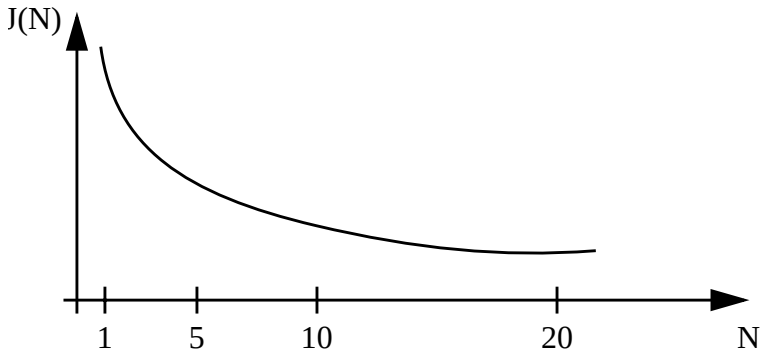


Figure A-4 Maximum bus clock jitter approximation