



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	91
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12dt12f1mpve

2.3.21	PH7 / KWH7 — Port H I/O Pin 7	59
2.3.22	PH6 / KWH6 — Port H I/O Pin 6	60
2.3.23	PH5 / KWH5 — Port H I/O Pin 5	60
2.3.24	PH4 / KWH4 — Port H I/O Pin 2	60
2.3.25	PH3 / KWH3 — Port H I/O Pin 3	60
2.3.26	PH2 / KWH2 — Port H I/O Pin 2	60
2.3.27	PH1 / KWH1 — Port H I/O Pin 1	60
2.3.28	PH0 / KWH0 — Port H I/O Pin 0	60
2.3.29	PJ7 / KWJ7 / SCL / TXCAN0 — PORT J I/O Pin 7	60
2.3.30	PJ6 / KWJ6 / SDA / RXCAN0 — PORT J I/O Pin 6	61
2.3.31	PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]	61
2.3.32	PK7 / ECS / ROMCTL — Port K I/O Pin 7	61
2.3.33	PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]	61
2.3.34	PM7 — Port M I/O Pin 7	61
2.3.35	PM6 — Port M I/O Pin 6	61
2.3.36	PM5 / TXCAN0 / SCK0 — Port M I/O Pin 5	61
2.3.37	PM4 / RXCAN0 / MOSI0 — Port M I/O Pin 4	61
2.3.38	PM3 / TXCAN0 / SS0 — Port M I/O Pin 3	62
2.3.39	PM2 / RXCAN0 / MISO0 — Port M I/O Pin 2	62
2.3.40	PM1 / TXCAN0 / TXB — Port M I/O Pin 1	62
2.3.41	PM0 / RXCAN0 / RXB — Port M I/O Pin 0	62
2.3.42	PP7 / KWP7 / PWM7 — Port P I/O Pin 7	62
2.3.43	PP6 / KWP6 / PWM6 — Port P I/O Pin 6	62
2.3.44	PP5 / KWP5 / PWM5 — Port P I/O Pin 5	62
2.3.45	PP4 / KWP4 / PWM4 — Port P I/O Pin 4	62
2.3.46	PP3 / KWP3 / PWM3 — Port P I/O Pin 3	63
2.3.47	PP2 / KWP2 / PWM2 — Port P I/O Pin 2	63
2.3.48	PP1 / KWP1 / PWM1 — Port P I/O Pin 1	63
2.3.49	PP0 / KWP0 / PWM0 — Port P I/O Pin 0	63
2.3.50	PS7 / SS0 — Port S I/O Pin 7	63
2.3.51	PS6 / SCK0 — Port S I/O Pin 6	63
2.3.52	PS5 / MOSI0 — Port S I/O Pin 5	63
2.3.53	PS4 / MISO0 — Port S I/O Pin 4	63
2.3.54	PS3 / TXD1 — Port S I/O Pin 3	63
2.3.55	PS2 / RXD1 — Port S I/O Pin 2	64
2.3.56	PS1 / TXD0 — Port S I/O Pin 1	64

List of Figures

Figure 0-1	Order Partnumber Example	15
Figure 1-1	MC9S12DJ64 Block Diagram	23
Figure 1-2	MC9S12DJ64 Memory Map out of Reset	27
Figure 1-3	MC9S12D32 Memory Map out of Reset	29
Figure 2-1	Pin Assignments in 112-pin LQFP for MC9S12DJ64	52
Figure 2-2	Pin Assignments in 80-pin QFP for MC9S12DJ64 and MC9S12D32	53
Figure 2-3	PLL Loop Filter Connections	56
Figure 2-4	Colpitts Oscillator Connections (PE7=1)	58
Figure 2-5	Pierce Oscillator Connections (PE7=0)	58
Figure 2-6	External Clock Connections (PE7=0)	58
Figure 3-1	Clock Connections	67
Figure 22-1	Recommended PCB Layout 112LQFP Colpitts Oscillator	82
Figure 22-2	Recommended PCB Layout for 80QFP Colpitts Oscillator	83
Figure 22-3	Recommended PCB Layout for 112LQFP Pierce Oscillator	84
Figure 22-4	Recommended PCB Layout for 80QFP Pierce Oscillator	85
Figure A-1	ATD Accuracy Definitions	100
Figure A-2	Basic PLL functional diagram	109
Figure A-3	Jitter Definitions	111
Figure A-4	Maximum bus clock jitter approximation	111
Figure A-5	SPI Master Timing (CPHA = 0)	115
Figure A-6	SPI Master Timing (CPHA =1)	116
Figure A-7	SPI Slave Timing (CPHA = 0)	117
Figure A-8	SPI Slave Timing (CPHA =1)	117
Figure A-9	General External Bus Timing	120
Figure B-1	112-pin LQFP mechanical dimensions (case no. 987)	124
Figure B-2	80-pin QFP Mechanical Dimensions (case no. 841B)	125

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DJ64 device.

Figure 1-1 MC9S12DJ64 Block Diagram

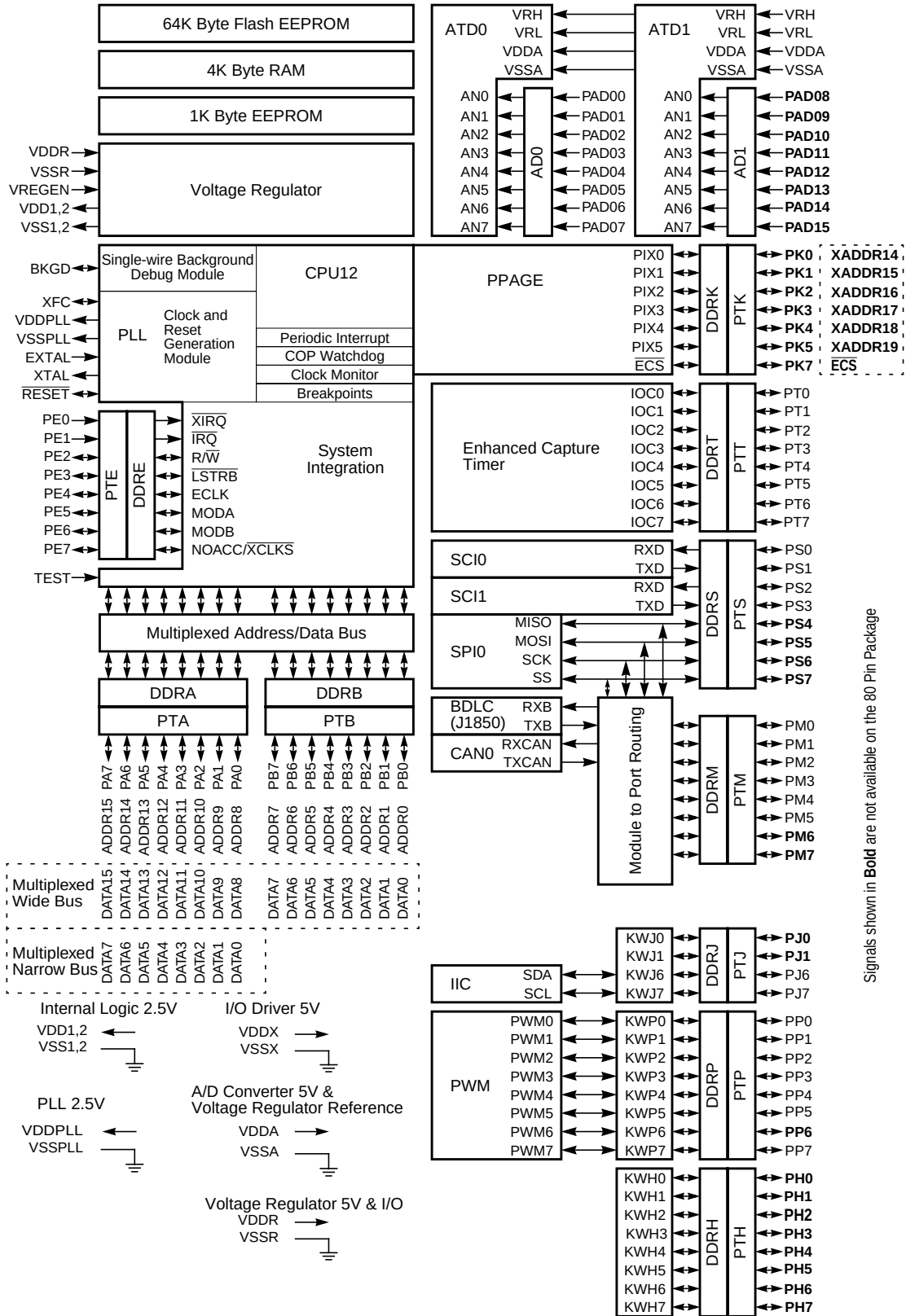


Table 1-2 Device Memory Map for MC9S12D32

Address	Module	Size (Bytes)
\$0000 - \$000F	HCS12 Multiplexed External Bus Interface	16
\$0010 - \$0014	HCS12 Module Mapping Control	5
\$0015 - \$0016	HCS12 Interrupt	2
\$0017 - \$0019	Reserved	3
\$001A - \$001B	Device ID register (PARTID)	2
\$001C - \$001D	HCS12 Module Mapping Control	2
\$001E	HCS12 Multiplexed External Bus Interface	1
\$001F	HCS12 Interrupt	1
\$0020 - \$0027	Reserved	8
\$0028 - \$002F	HCS12 Breakpoint Module	8
\$0030 - \$0031	HCS12 Module Mapping Control	2
\$0032 - \$0033	HCS12 Multiplexed External Bus Interface	2
\$0034 - \$003F	Clock and Reset Generator (PLL, RTI, COP)	12
\$0040 - \$007F	Enhanced Capture Timer 16-bit 8 channels	64
\$0080 - \$009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
\$00A0 - \$00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
\$00C8 - \$00CF	Serial Communications Interface 0 (SCI0)	8
\$00D0 - \$00D7	Serial Communications Interface 0 (SCI1)	8
\$00D8 - \$00DF	Serial Peripheral Interface (SPI0)	8
\$00E0 - \$00E7	Inter IC Bus	8
\$00E8 - \$00EF	Byte Data Link Controller (BDLC)	8
\$00F0 - \$00FF	Reserved	16
\$0100 - \$010F	Flash Control Register	16
\$0110 - \$011B	EEPROM Control Register	12
\$011C - \$011F	Reserved	4
\$0120 - \$013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
\$0140 - \$017F	Freescale Scalable Can (CAN0)	
\$0180 - \$023F	Reserved	192
\$0240 - \$027F	Port Integration Module (PIM)	64
\$0280 - \$03FF	Reserved	384
\$0000 - \$07FF	EEPROM array 1k Array mapped twice in the address space	2048
\$0000 - \$0FFF	RAM array, lower half (\$0000-\$07FF not usable)	4096
\$4000 - \$7FFF	16k Fixed Flash EEPROM array (same as array from \$8000 - \$BFFF when ROMHM=0)	16384
\$8000 - \$FFFF	32K Fixed Flash EEPROM array	32768

64

1.5.1 Detailed Register Map

\$0000 - \$000F

MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
\$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
\$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
\$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
\$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
\$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
\$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
\$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0010 - \$0014

MMC map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
\$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								

\$0040 - \$007F**ECT (Enhanced Capture Timer 16 Bit 8 Channels)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$004A	TCTL3	Read: Write:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
\$004B	TCTL4	Read: Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
\$004C	TIE	Read: Write:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
\$004D	TSCR2	Read: Write:	TOI	0	0	0	TCRE	PR2	PR1	PR0
\$004E	TFLG1	Read: Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
\$004F	TFLG2	Read: Write:	TOF	0	0	0	0	0	0	0
\$0050	TC0 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$0051	TC0 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0052	TC1 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$0053	TC1 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0054	TC2 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$0055	TC2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0056	TC3 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$0057	TC3 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0058	TC4 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$0059	TC4 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$005A	TC5 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$005B	TC5 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$005C	TC6 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$005D	TC6 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$005E	TC7 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
\$005F	TC7 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
\$0060	PACTL	Read: Write:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
\$0061	PAFLG	Read: Write:	0	0	0	0	0	0	PAOVF	PAIF
\$0062	PACN3 (hi)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

\$00E8 - \$00EF**BDLC (Bytelevel Data Link Controller J1850)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00E8	DLCBCR1	Read:	IMSG	CLKS	0	0	0	0	IE	WCM
		Write:								
\$00E9	DLCBSVR	Read:	0	0	I3	I2	I1	I0	0	0
		Write:								
\$00EA	DLCBCR2	Read:	SMRST	DLOOP	RX4XE	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
		Write:								
\$00EB	DLCBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
\$00EC	DLCBARD	Read:	0	RXPOL	0	0	BO3	BO2	BO1	BO0
		Write:								
\$00ED	DLCBRSR	Read:	0	0	R5	R4	R3	R2	R1	R0
		Write:								
\$00EE	DLCSCR	Read:	0	0	0	BDLCE	0	0	0	0
		Write:								
\$00EF	DLCBSTAT	Read:	0	0	0	0	0	0	0	IDLE
		Write:								

\$00F0 - \$00FF**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00F0 - \$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0100 - \$010F**Flash Control Register (fts64k)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
\$0101	FSEC	Read:	KEYEN	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
\$0102	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
		Write:								
\$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
\$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
\$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
\$0107	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0108	FADDRHI	Read:	Bit 14	Bit 14	13	12	11	10	9	Bit 8
		Write:								
\$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 RESET — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This input only pin is reserved for test.

NOTE: The TEST pin must be tied to VSS in all applications.

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

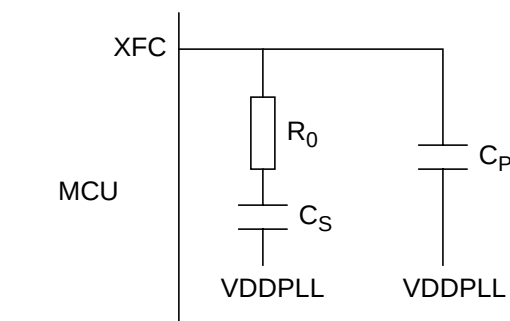


Figure 2-3 PLL Loop Filter Connections

2.3.6 BKGD / TAGHI / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/TAGHI/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the

Mnemonic	Pin Number	Nominal Voltage	Description
	112-pin QFP		
VDDPLL	43	2.5V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	45	0V	
VREGEN	97	5.0V	Internal Voltage Regulator enable/disable

2.4.1 VDDX, VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDX and VSSX are the supplies for Ports J, K, M, P, T and S.

2.4.2 VDDR, VSSR — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

VDDR and VSSR are the supplies for Ports A, B, E and H.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Internal Logic Power Supply Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

NOTE: No load allowed except for bypass capacitors.

2.4.4 VDDA, VSSA — Power Supply Pins for ATD0/ATD1 and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the two analog to digital converters. It also provides the reference for the internal voltage regulator. This allows the supply voltage to ATD0/ATD1 and the reference voltage to be bypassed independently.

NOTE: *For devices assembled in 80-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to **Table 2-1** for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Table 22-1 Suggested External Component Values

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	100 .. 220nF
C2	VDD2 filter cap	ceramic X7R	100 .. 220nF
C3	VDDA filter cap	ceramic X7R	100nF
C4	VDDR filter cap	X7R/tantalum	>=100nF
C5	VDDPLL filter cap	ceramic X7R	100nF
C6	VDDX filter cap	X7R/tantalum	>=100nF
C7	OSC load cap		
C8	OSC load cap		
C9 / C _S	PLL loop filter cap	See PLL specification chapter	
C10 / C _P	PLL loop filter cap		
C11 / C _{DC}	DC cutoff cap	Colpitts mode only, if recommended by quartz manufacturer	
R1	PLL loop filter res	See PLL specification chapter	
R2 / R _B	PLL loop filter res	Pierce mode only	
R3 / R _S	PLL loop filter res		
Q1	Quartz		

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins(C1 - C6).
- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	- 1 1	- 1 1	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	- 3 3	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	T	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	T	Machine Model (MM)	V_{MM}	200	-	V
3	T	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	T	Latch-up Current at $T_A = 125^\circ\text{C}$ positive negative	I_{LAT}	+100 -100	-	mA
5	T	Latch-up Current at $T_A = 27^\circ\text{C}$ positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reference Potential Low High	V_{RL} V_{RH}	V_{SSA} $V_{DDA}/2$		$V_{DDA}/2$ V_{DDA}	V V
2	C	Differential Reference Voltage ¹	$V_{RH}-V_{RL}$	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 7		28 14	Cycles μs
5	D	ATD 8-Bit Conversion Period Clock Cycles ² Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 6		26 13	Cycles μs
6	D	Recovery Time ($V_{DDA}=5.0$ Volts)	t_{REC}			20	μs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

Conditions are shown in Table A-4 unless otherwise noted $V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV $f_{ATDCLK} = 2.0MHz$							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	-1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	-2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error ¹	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB		20		mV
6	P	8-Bit Differential Nonlinearity	DNL	-0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	-1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error ¹	AE	-1.5	±1.0	1.5	Counts

NOTES:

1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^n DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

A.4 Voltage Regulator

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits. No external DC load is allowed.

Table A-13 Voltage Regulator Recommended Load Capacitances

Rating	Symbol	Min	Typ	Max	Unit
Load Capacitance on VDD1, 2	C_{LVDD}		220		nF
Load Capacitance on VDDPLL	$C_{LVDDfcPLL}$		220		nF

A.7 SPI

A.7.1 Master Mode

Figure A-5 and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-18**.

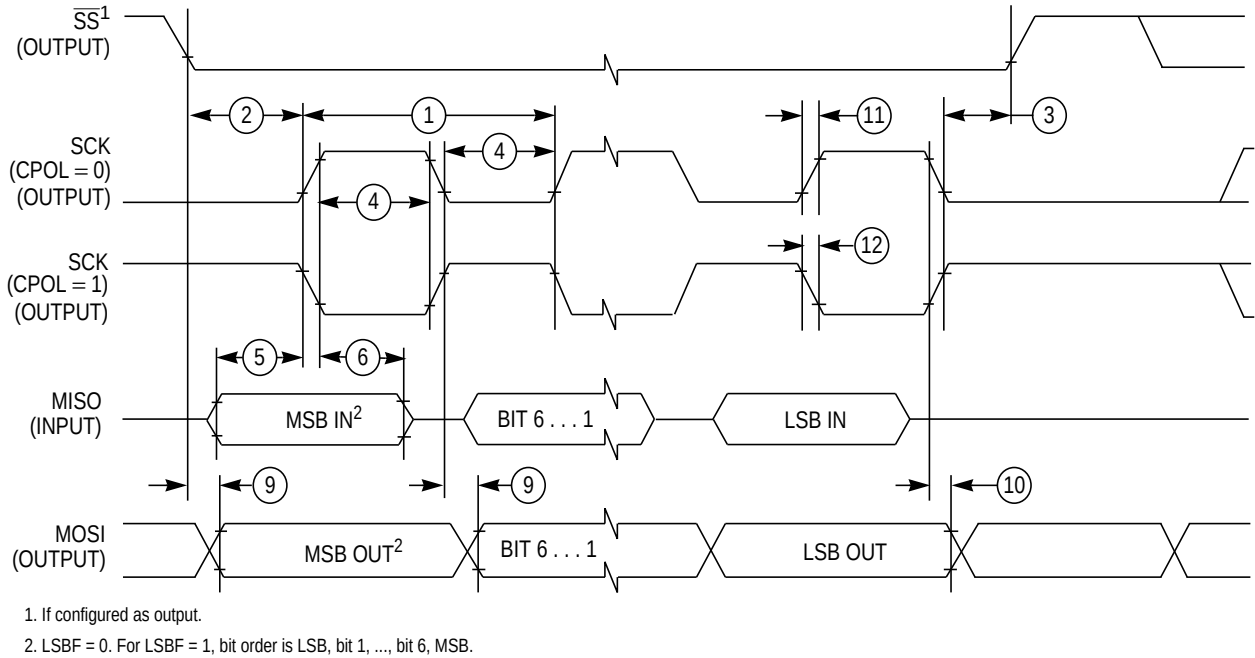


Figure A-5 SPI Master Timing (CPHA = 0)

A.7.2 Slave Mode

Figure A-7 and **Figure A-8** illustrate the slave mode timing. Timing values are shown in **Table A-19**.

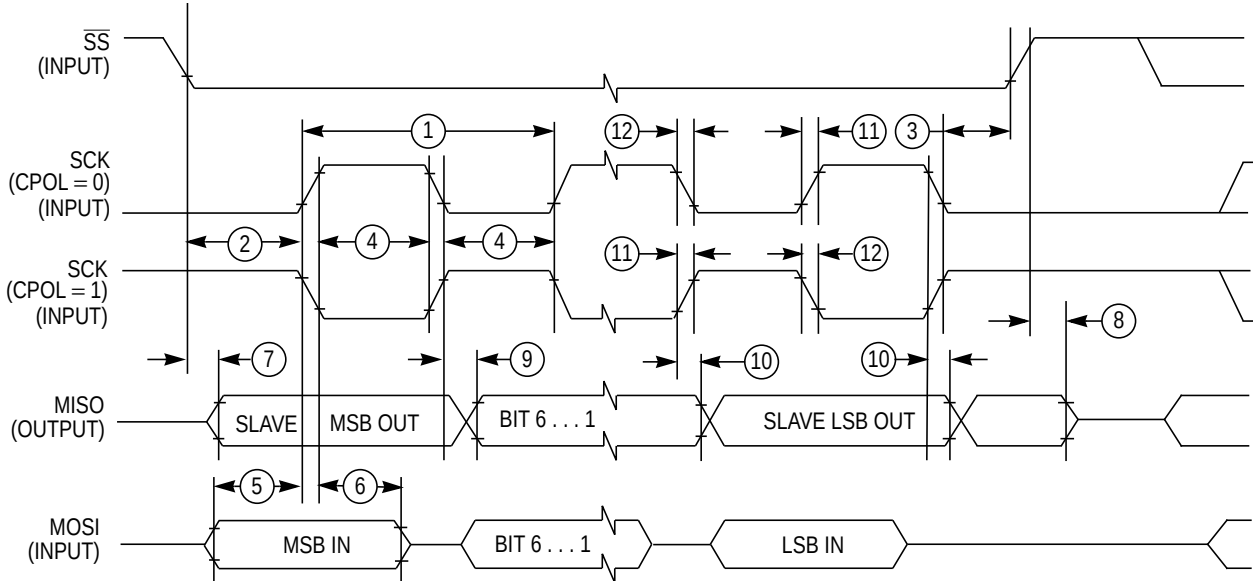


Figure A-7 SPI Slave Timing (CPHA = 0)

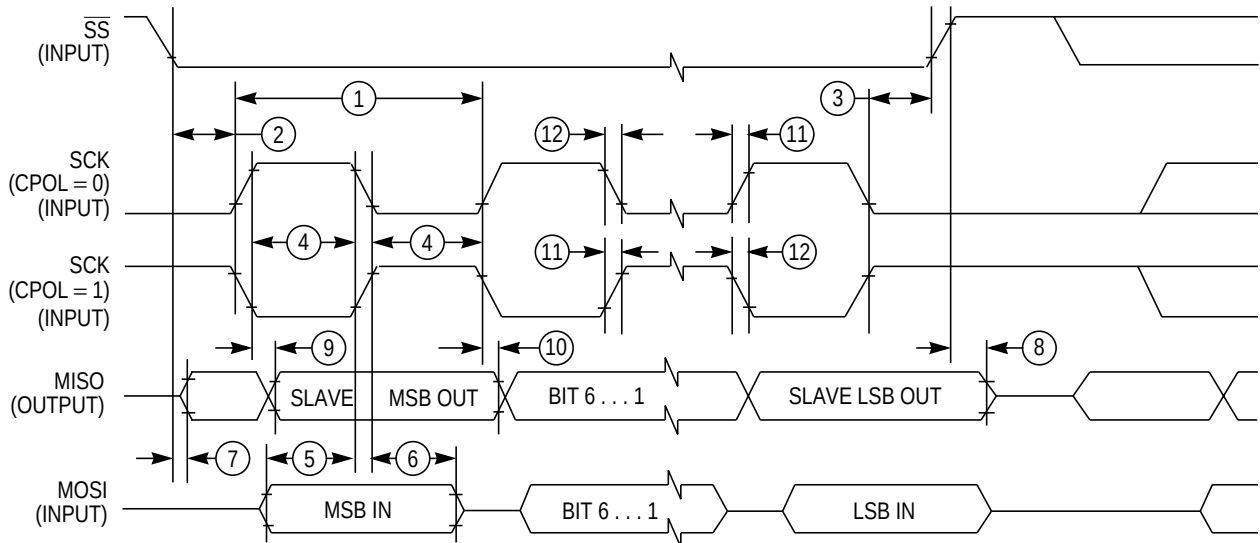


Figure A-8 SPI Slave Timing (CPHA = 1)

**FINAL PAGE OF
128
PAGES**