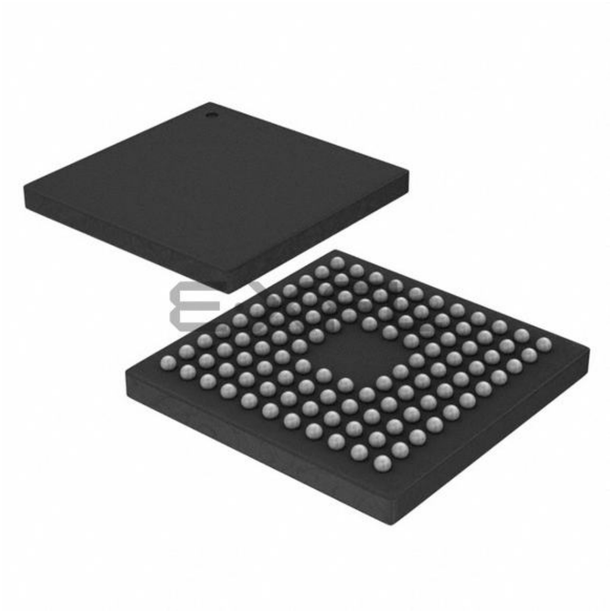
Silicon Labs - EFM32GG290F1024G-E-BGA112 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	90
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg290f1024g-e-bga112

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32GG290 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32GG290F512G-E-BGA112	512	128	48	1.98 - 3.8	-40 - 85	BGA112
EFM32GG290F1024G-E-BGA112	1024	128	48	1.98 - 3.8	-40 - 85	BGA112

Adding the suffix 'R' to the part number (e.g. EFM32GG290F512G-E-BGA112R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

2.1.12 Inter-Integrated Circuit Interface (I2C)

The I^{2}C module provides an interface between the MCU and a serial I^{2}C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^{2}C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.13 Universal Synchronous/Asynchronous Receiver/Transmitter (US-ART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.14 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.15 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.16 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM}, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.17 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.18 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage	EM0	1.74		1.96	V
		EM2	1.74		1.98	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.57		1.70	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{PERASE}	Page erase time	LPERASE == 0	20	20.4	20.8	ms
		LPERASE == 1	40	40.4	40.8	ms
t_{DERASE}	Device erase time				161.6	ms
I_{ERASE}	Erase current	LPERASE == 0			14[1]	mA
		LPERASE == 1			7[1]	mA
I_{WRITE}	Write current	LPWRITE == 0			14[1]	mA
		LPWRITE == 1			7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

[1] Measured at 25°C

3.8 General Purpose Input Output

Table 3.7. GPIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IOIL}	Input low voltage				$0.30V_{DD}$	V
V_{IOIH}	Input high voltage		$0.70V_{DD}$			V
V_{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.80V_{DD}$		V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.90V_{DD}$		V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.85V_{DD}$		V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.90V_{DD}$		V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75V_{DD}$			V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85V_{DD}$			V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60V_{DD}$			V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1] See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

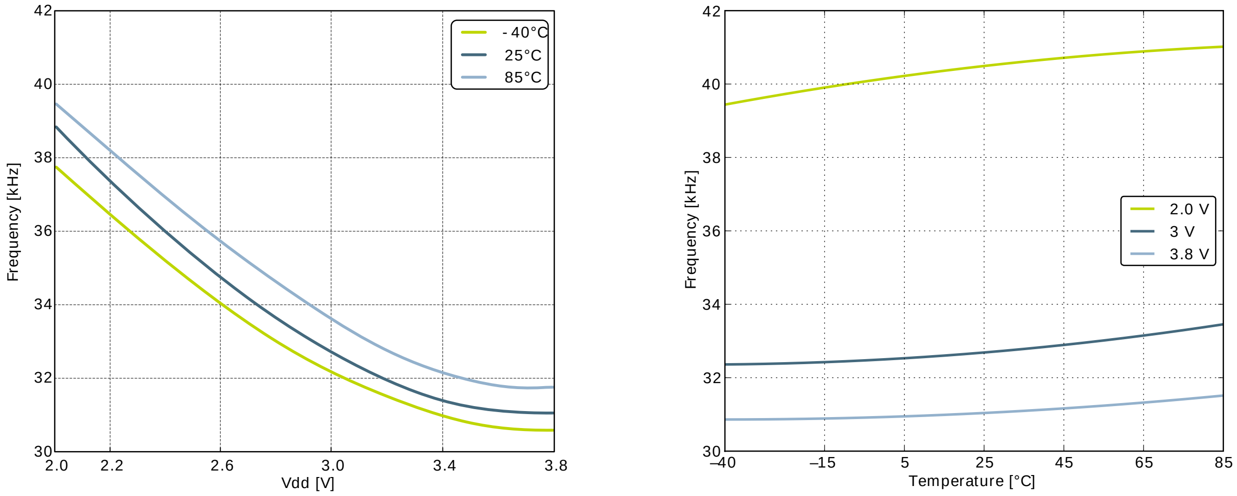
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25°C		31.29	32.768	34.28	kHz
t_{LFRCO}	Startup time not including software calibration			150		µs
I_{LFRCO}	Current consumption			300	900	nA
$TUNESTEP_{LFRCO}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

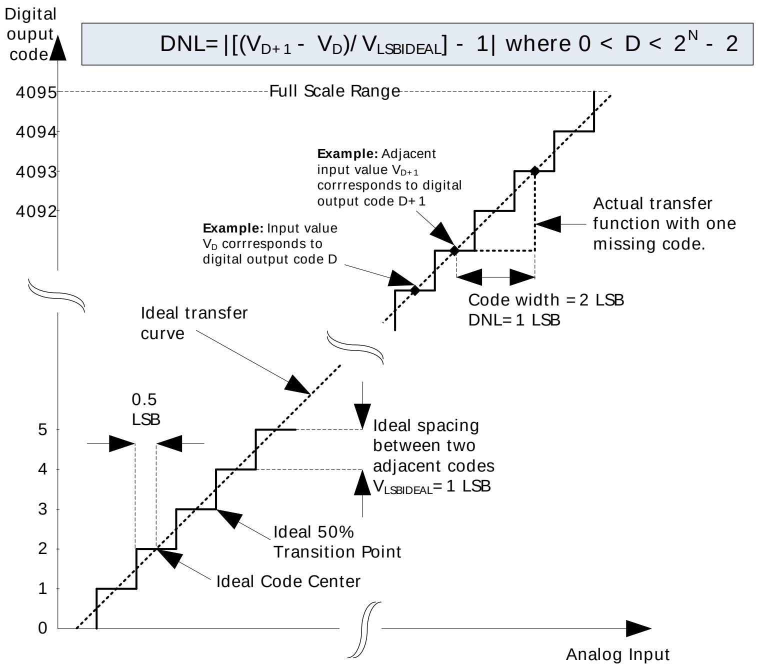


3.9.4 HFRCO

Table 3.11. HFRCO

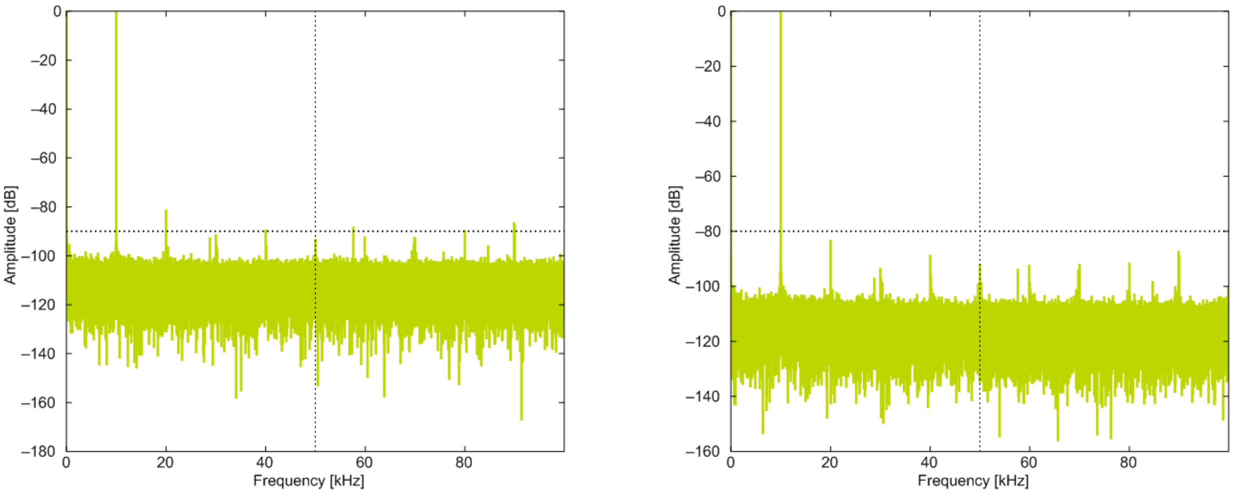
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48[1]	6.60[1]	6.72[1]	MHz
		1 MHz frequency band	1.15[2]	1.20[2]	1.25[2]	MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz		0.6		Cycles
	Settling time after band switch			25		Cycles

Figure 3.18. Differential Non-Linearity (DNL)



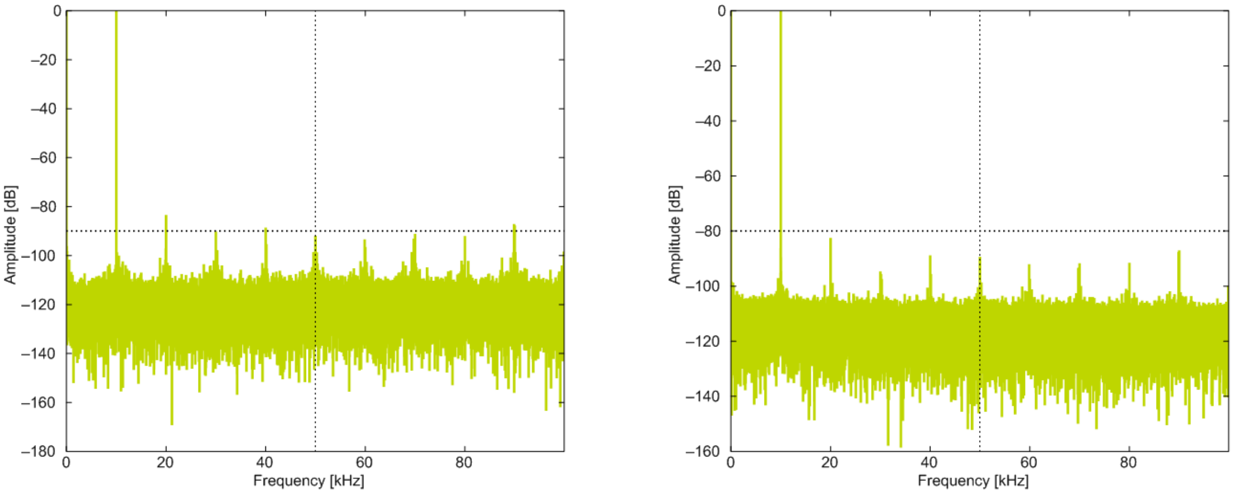
3.10.1 Typical performance

Figure 3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



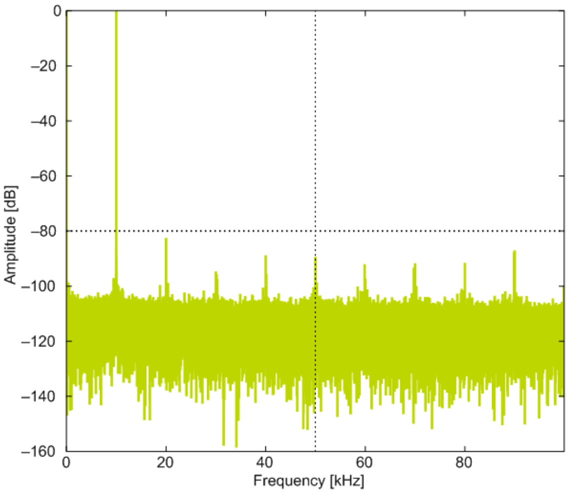
1.25V Reference

2.5V Reference



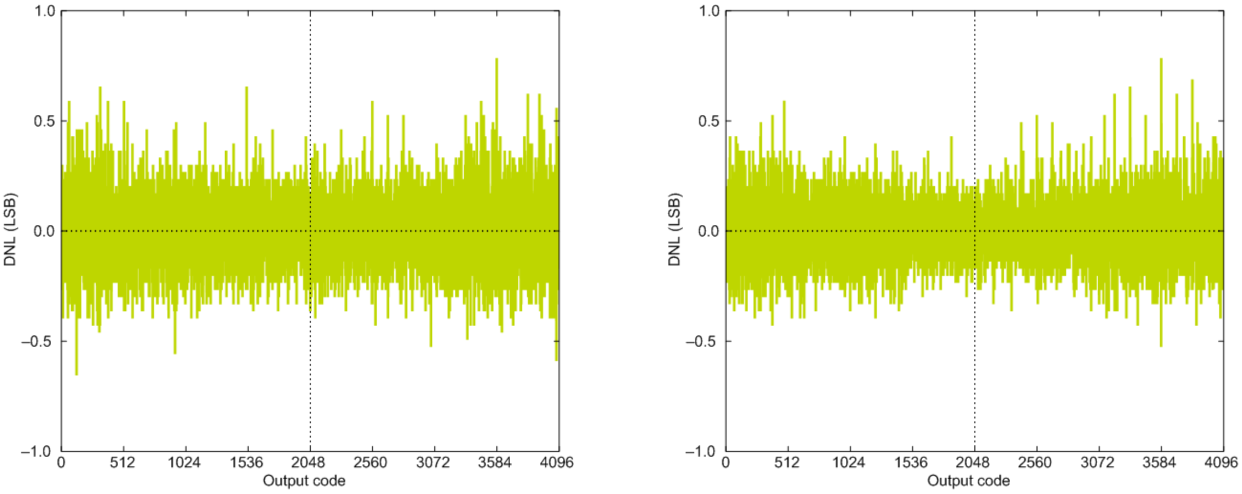
2XVDDVSS Reference

5VDIFF Reference



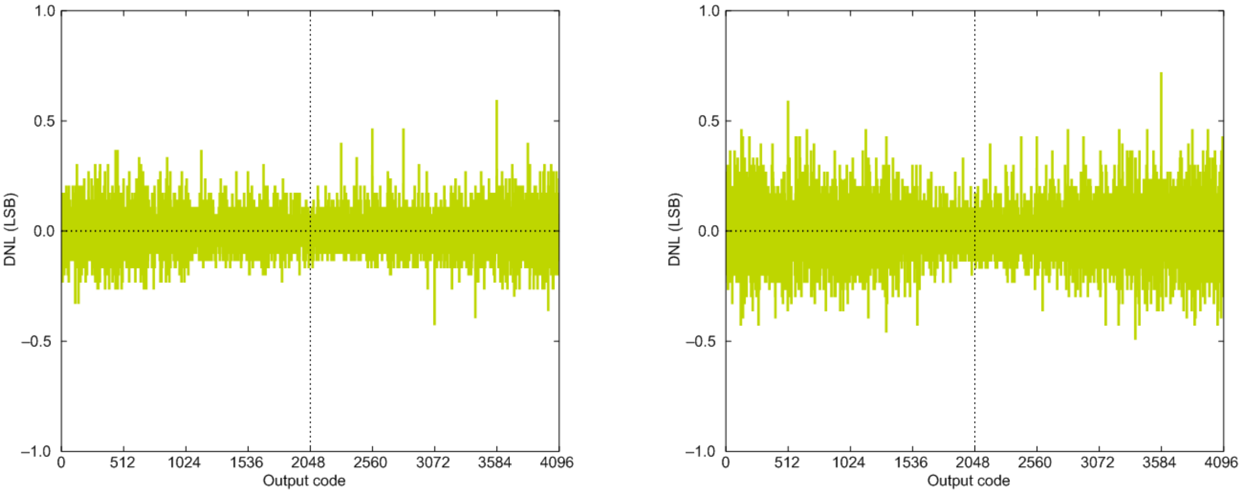
VDD Reference

Figure 3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C



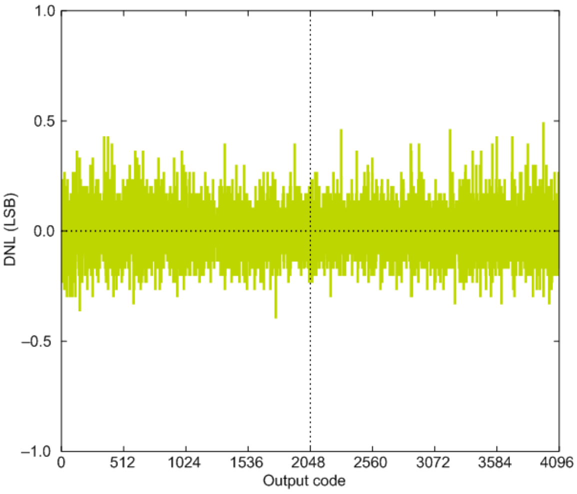
1.25V Reference

2.5V Reference



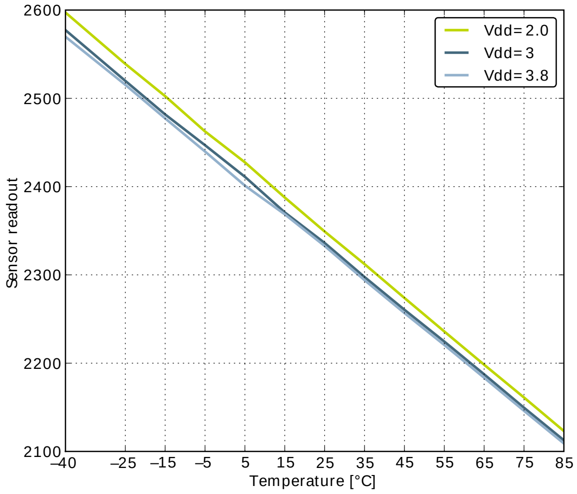
2XVDDVSS Reference

5VDIFF Reference



VDD Reference

Figure 3.24. ADC Temperature sensor readout



3.11 Digital Analog Converter (DAC)

Table 3.15. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12 bit		400[1]	600[1]	µA
		100 kSamples/s, 12 bit		200[1]	260[1]	µA
		1 kSamples/s 12 bit NORMAL		17[1]	25[1]	µA
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cyckles per conversion			2		
$t_{DACCONV}$	Conversion time		2			µs
$t_{DACSETTLE}$	Settling time			5		µs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB

Figure 3.27. OPAMP Negative Power Supply Rejection Ratio

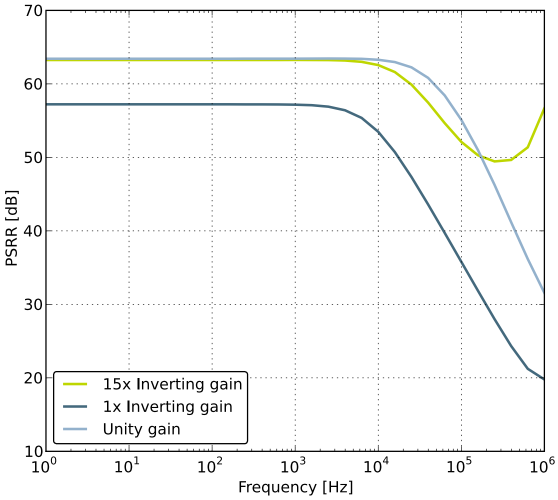


Figure 3.28. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

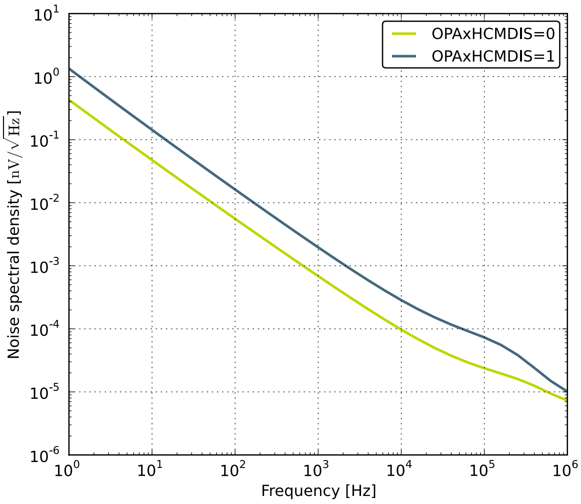


Figure 3.29. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)

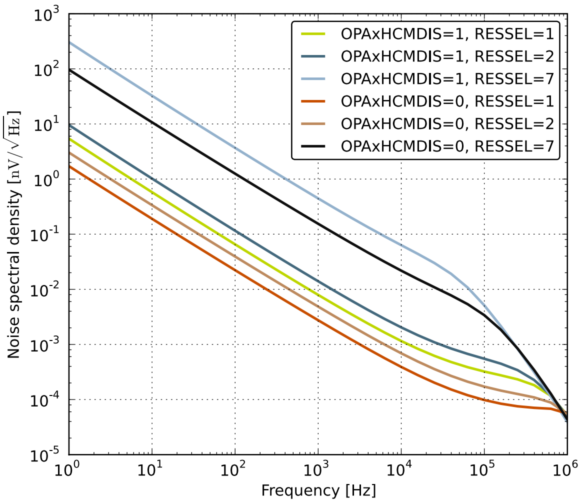
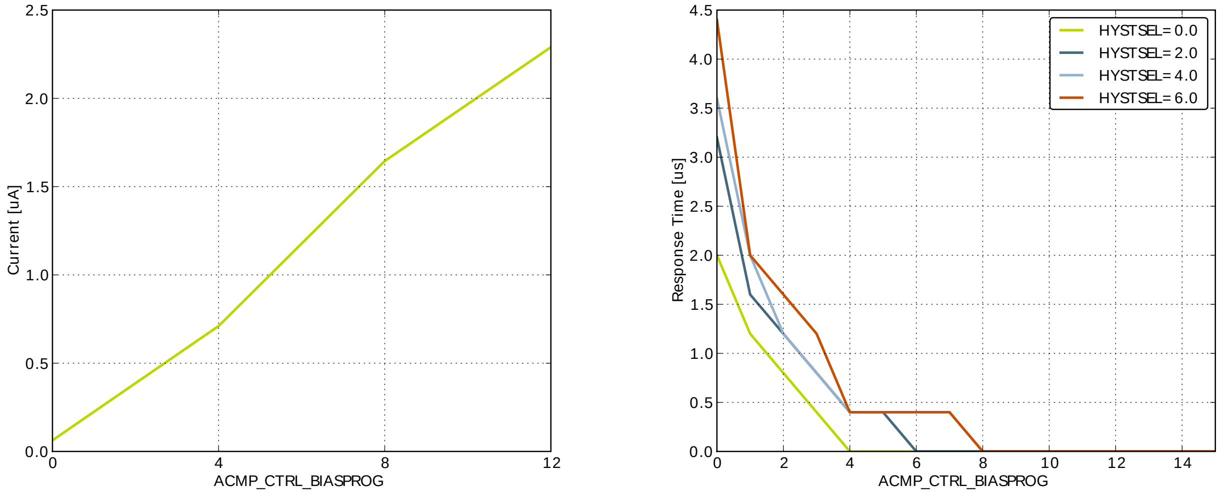
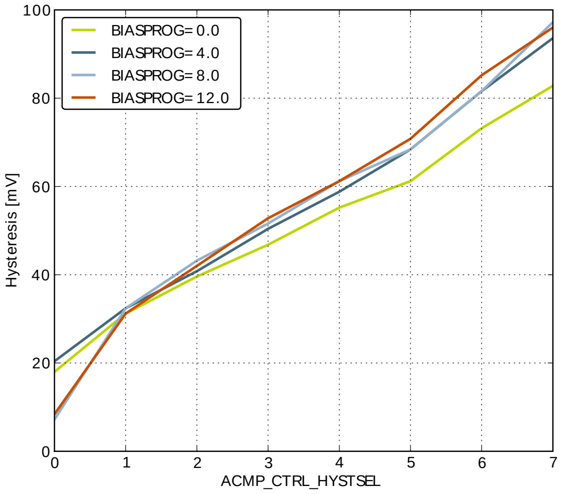


Figure 3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4

Response time



Hysteresis

Figure 3.34. EBI Read Enable Related Timing Requirements

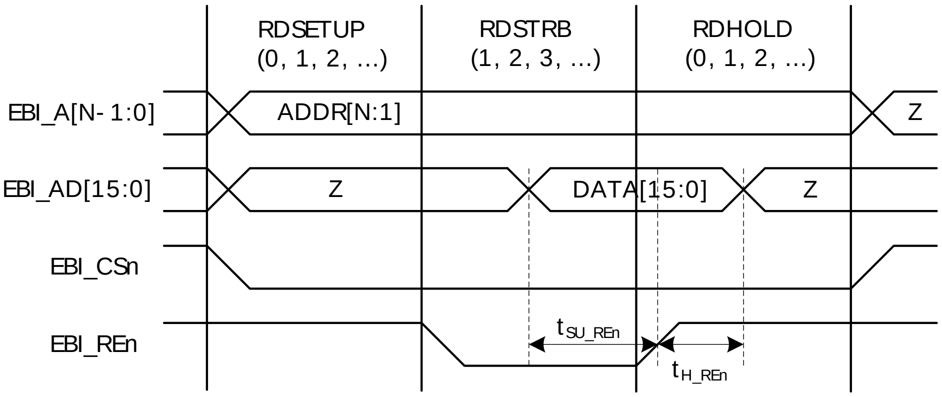


Table 3.22. EBI Read Enable Related Timing Requirements

Symbol	Parameter	Min	Typ	Max	Unit
t_{SU_REn} [1 2 3 4]	Setup time, from EBI_AD valid to trailing EBI_REn edge	37			ns
t_{H_Ren} [1 2 3 4]	Hold time, from trailing EBI_REn edge to EBI_AD invalid	-1			ns

[1] Applies for all addressing modes (figure only shows D16A8).

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

Figure 3.35. EBI Ready/Wait Related Timing Requirements

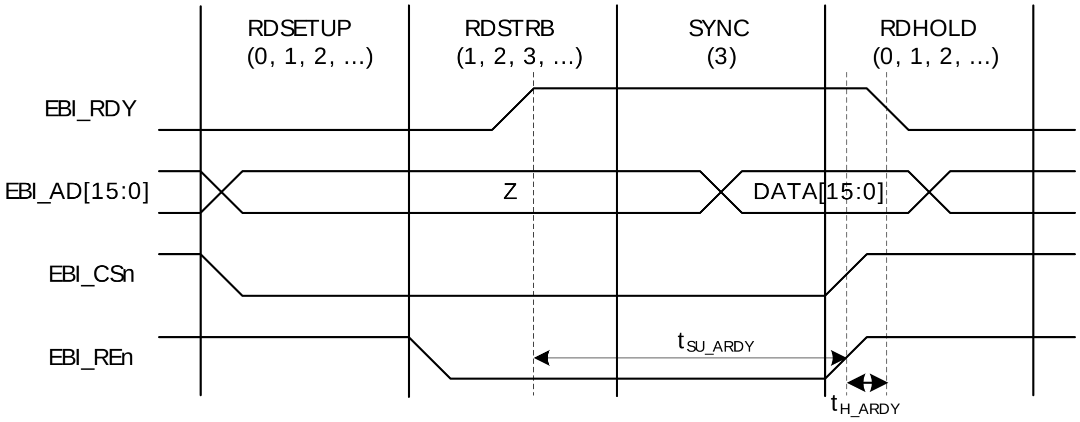


Table 3.23. EBI Ready/Wait Related Timing Requirements

Symbol	Parameter	Min	Typ	Max	Unit
t_{SU_ARDY} [1 2 3 4]	Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	37 + (3 * $t_{HFCORECLK}$)			ns

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG290* is shown in Table 4.3 (p. 63). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32GG290* is shown in Figure 4.2 (p. 64) .

Figure 5.3. BGA112 PCB Stencil Design

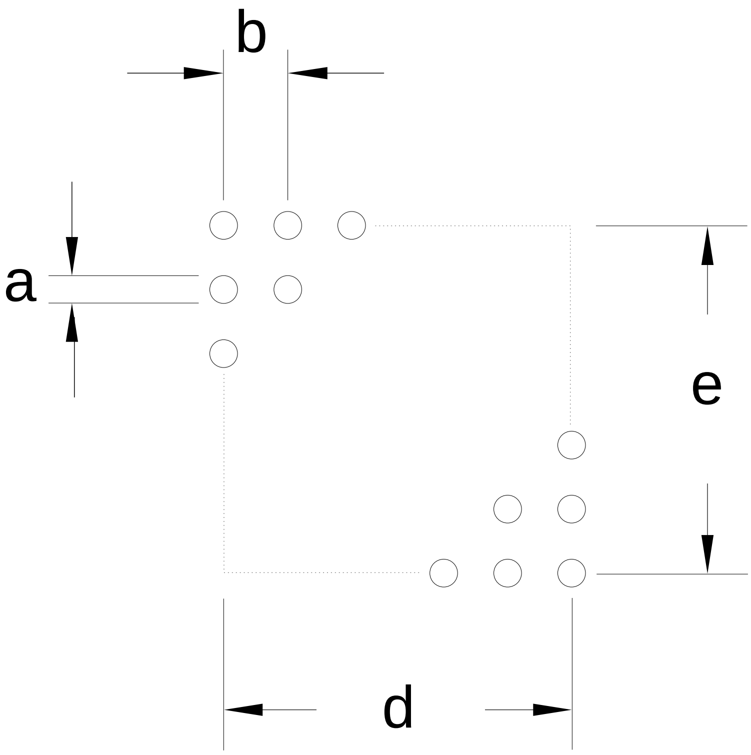


Table 5.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.33
b	0.80
d	8.00
e	8.00

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 64) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

Updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.98

May 25th, 2012

Corrected BGA solder balls material description.

Corrected EM3 current consumption in the Electrical Characteristics section.

7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected BGA112 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected BGA112 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.10 Revision 0.91

March 21th, 2011

Added new alternative locations for EBI and SWO.

Corrected slew rate data for Opamps.

7.11 Revision 0.90

February 4th, 2011

Initial preliminary release.

A Disclaimer and Trademarks

A.1 Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

A.2 Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world’s most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

B Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
http://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

List of Figures

2.1. Block Diagram 3
2.2. *EFM32GG290* Memory Map with largest RAM and Flash sizes 9
3.1. EM2 current consumption. RTC prescaled to 1 Hz, 32.768 kHz LFRCO. 12
3.2. EM3 current consumption. 12
3.3. EM4 current consumption. 13
3.4. Typical Low-Level Output Current, 2V Supply Voltage 17
3.5. Typical High-Level Output Current, 2V Supply Voltage 18
3.6. Typical Low-Level Output Current, 3V Supply Voltage 19
3.7. Typical High-Level Output Current, 3V Supply Voltage 20
3.8. Typical Low-Level Output Current, 3.8V Supply Voltage 21
3.9. Typical High-Level Output Current, 3.8V Supply Voltage 22
3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage 24
3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature 25
3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature 25
3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature 26
3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature 26
3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature 26
3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature 27
3.17. Integral Non-Linearity (INL) 32
3.18. Differential Non-Linearity (DNL) 33
3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C 34
3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C 35
3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C 36
3.22. ADC Absolute Offset, Common Mode = Vdd /2 37
3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V 37
3.24. ADC Temperature sensor readout 38
3.25. OPAMP Common Mode Rejection Ratio 41
3.26. OPAMP Positive Power Supply Rejection Ratio 41
3.27. OPAMP Negative Power Supply Rejection Ratio 42
3.28. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V 42
3.29. OPAMP Voltage Noise Spectral Density (Non-Unity Gain) 42
3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1 44
3.31. EBI Write Enable Timing 45
3.32. EBI Address Latch Enable Related Output Timing 46
3.33. EBI Read Enable Related Output Timing 47
3.34. EBI Read Enable Related Timing Requirements 48
3.35. EBI Ready/Wait Related Timing Requirements 48
3.36. SPI Master Timing 50
3.37. SPI Slave Timing 51
4.1. *EFM32GG290* Pinout (top view, not to scale) 53
4.2. Opamp Pinout 64
4.3. BGA112 64
5.1. BGA112 PCB Land Pattern 66
5.2. BGA112 PCB Solder Mask 67
5.3. BGA112 PCB Stencil Design 68
6.1. Example Chip Marking (top view) 69