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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22g18a-aut

2. Configuration Summary

	SAM L22N	SAM L22J	SAM L22G
Pins	100	64	48 (QFN and TQFP) 49 (WLCSP)
General Purpose I/O-pins (GPIOs)[1]	82	50	36
Flash	256/128/64KB	256/128/64KB	256/128/64KB
Flash RWW section	8/4/2KB	8/4/2KB	8/4/2KB
System SRAM	32/16/8KB	32/16/8KB	32/16/8KB
Segment LCD (SLCD) Pins[1]	48 selectable from 52	31	23
Timer Counter (TC) instances	4	4	4
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	1	1	1
Waveform output channels per TCC	4	4	4
DMA channels	16	16	16
USB interface	1	1	1
AES engine	1	1	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
True Random Generator (TRNG)	1	1	1
Serial Communication Interface (SERCOM) instances	6	4[2]	4[2]
Analog-to-Digital Converter (ADC) channels	20	16	10
Two Analog Comparators (AC) with number of external input channels	4	4	2
Tamper Input Pins	5	3	2

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML22J18A-MUT			QFN64	

3.3. SAM L22G

Table 3-3. SAM L22G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML22G16A-MUT			QFN48	
ATSAML22G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML22G17A-MUT			QFN48	
ATSAML22G17A-UUT			WLCSP49	
ATSAML22G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML22G18A-MUT			QFN48	
ATSAML22G18A-UUT			WLCSP49	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

Table 3-4. SAM L22 Device Identification Values

DSU DID.DEVSEL	Device
0x0	L22N18
0x1	L22N17
0x2	L22N16
0x3-0x4	Reserved
0x5	L22J18
0x6	L22J17
0x7	L22J16
0x8-0x9	Reserved
0xA	L22G18
0xB	L22G17
0xC	L22G16
0xD-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

5. Pinout

5.1. SAM L22G

Figure 5-1. 48-Pin QFN, TQFP

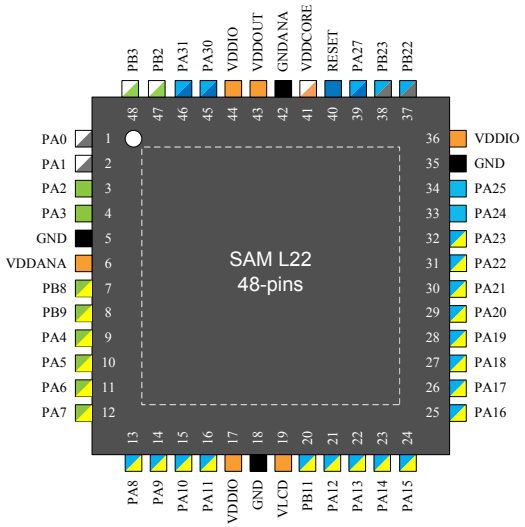
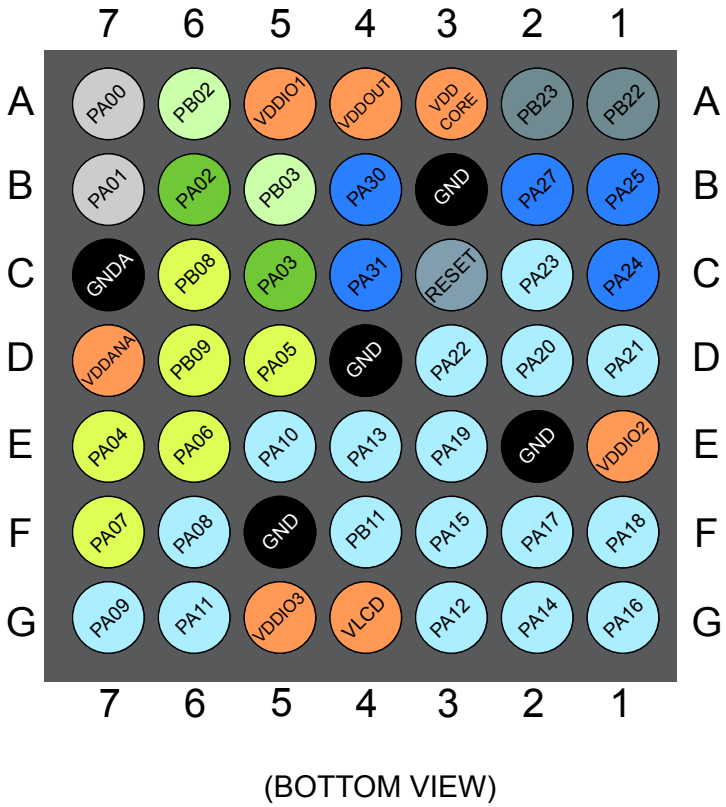


Figure 5-2. 49-Pin WLCSP



(BOTTOM VIEW)

Signal Name	Function	Type	Active Level
32KHz Oscillators Control - OSC32KCTRL			
XIN32	32KHz Crystal or external clock Input	Analog/Digital	
XOUT32	32KHz Crystal Output	Analog	
Timer Counter - TCx			
WO[1:0]	Waveform Outputs	Digital	
Timer Counter - TCCx			
WO[7:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[7:0]	PTC Input/Output	Analog	
Y[23:0]	PTC Input/Output	Analog	
X[31:24]	PTC Output	Analog	
General Purpose I/O - PORT			
PA25 - PA00	Parallel I/O Controller I/O Port A	Digital	
PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB09 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB25 - PB11	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	
PC03 - PC00	Parallel I/O Controller I/O Port C	Digital	
PC07 - PC05	Parallel I/O Controller I/O Port C	Digital	
PC17 - PC12	Parallel I/O Controller I/O Port C	Digital	
PC28 - PC24	Parallel I/O Controller I/O Port C	Digital	
General Purpose input - PORT			
PC11 - PC08	Parallel I/O Controller input Port C	Digital	
PC21 - PC18	Parallel I/O Controller input Port C	Digital	
Segment LCD			
SLCD51 - SLCD00	Segment LCD	Analog	
VLCD	Bias Voltage	Analog	
Universal Serial Bus - USB			
DP	DP for USB	Digital	
DM	DM for USB	Digital	

7. I/O Multiplexing and Considerations

7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned a different peripheral functions. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral function A to I is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) of the PORT.

This table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 7-1. PORT Function Multiplexing

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
Battery backup	1	1	1	PA00	EIC/EXTINT[0]							SERCOM1/ PAD[0]					
	2	2	2	PA01	EIC/EXTINT[1]							SERCOM1/ PAD[1]					
			3	PC00	EIC/EXTINT[8]		ADC/ AIN[16]								RTC/IN[3]		
			4	PC01	EIC/EXTINT[9]		ADC/ AIN[17]								RTC/IN[4]		
			5	PC02	EIC/EXTINT[10]		ADC/ AIN[18]		PTC/ XY[6]								
			6	PC03	EIC/EXTINT[11]		ADC/ AIN[19]		PTC/ XY[7]								
	3	3	7	PA02	EIC/EXTINT[2]	ADC/ VREFB	ADC/ AIN[0]	AC/ AIN[0]	PTC/ XY[8]						RTC/IN[2]		
	4	4	8	PA03	EIC/EXTINT[3]	ADC/ VREFA	ADC/ AIN[1]	AC/ AIN[1]	PTC/ XY[9]								
		5	9	PB04	EIC/EXTINT[4]		ADC/ AIN[12]	AC/ AIN[2]	PTC/ XY[10]								
		6	10	PB05	EIC/EXTINT[5]		ADC/ AIN[13]	AC/ AIN[3]	PTC/ XY[11]								
		9	13	PB06	EIC/EXTINT[6]		ADC/ AIN[14]		PTC/ XY[12]	SLCD/ LP[0]							CCL/IN[6]
		10	14	PB07	EIC/EXTINT[7]		ADC/ AIN[15]		PTC/ XY[13]	SLCD/ LP[1]							CCL/IN[7]
	7	11	15	PB08	EIC/EXTINT[8]		ADC/ AIN[2]		PTC/ XY[14]	SLCD/ LP[2]		SERCOM3/ PAD[0]	TC/0/ WO[0]				CCL/IN[8]
	8	12	16	PB09	EIC/EXTINT[9]		ADC/ AIN[3]		PTC/ XY[15]	SLCD/ LP[3]		SERCOM3/ PAD[1]	TC/0/ WO[1]				CCL/ OUT[2]
	9	13	17	PA04	EIC/EXTINT[4]		ADC/ AIN[4]		PTC/ X[24]	SLCD/ LP[4]		SERCOM0/ PAD[0]	TCC/ WO[0]				CCL/IN[0]
	10	14	18	PA05	EIC/EXTINT[5]		ADC/ AIN[5]		PTC/ X[25]	SLCD/ LP[5]		SERCOM0/ PAD[1]	TCC/ WO[1]				CCL/IN[1]
	11	15	19	PA06	EIC/EXTINT[6]		ADC/ AIN[6]		PTC/ X[26]	SLCD/ LP[6]		SERCOM0/ PAD[2]					CCL/IN[2]
	12	16	20	PA07	EIC/EXTINT[7]		ADC/ AIN[7]		PTC/ X[27]	SLCD/ LP[7]		SERCOM0/ PAD[3]					CCL/ OUT[0]
			21	PC05	EIC/EXTINT[13]				PTC/ XY[4]	SLCD/ LP[8]							
			22	PC06	EIC/EXTINT[14]				PTC/ XY[5]	SLCD/ LP[9]							
			23	PC07	EIC/EXTINT[15]					SLCD/ LP[10]							
	13	17	26	PA08	EIC/NMI				PTC/ XY[3]	SLCD/ LP[11]	SERCOM0/ PAD[0]	SERCOM4/ PAD[0]	TCC/ WO[0]				CCL/IN[3]
	14	18	27	PA09	EIC/EXTINT[9]				PTC/ XY[2]	SLCD/ LP[12]	SERCOM0/ PAD[1]	SERCOM4/ PAD[1]	TCC/ WO[1]				CCL/IN[4]
	15	19	28	PA10	EIC/EXTINT[10]				PTC/ XY[1]	SLCD/ LP[13]	SERCOM0/ PAD[2]	SERCOM4/ PAD[2]		TCC/ WO[2]		GCLK/ IO[4]	CCL/IN[5]
	16	20	29	PA11	EIC/EXTINT[11]				PTC/ XY[0]	SLCD/ LP[14]	SERCOM0/ PAD[3]	SERCOM4/ PAD[3]		TCC/ WO[3]			CCL/ OUT[1]

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
digital: input only			30	PC08	EIC/EXTINT[0]					SLCD/ LP[15]							
			31	PC09	EIC/EXTINT[1]					SLCD/ LP[16]							
			32	PC10	EIC/EXTINT[2]					SLCD/ LP[17]	SERCOM1/ PAD[2]						
			33	PC11	EIC/EXTINT[3]					SLCD/ LP[18]	SERCOM1/ PAD[3]						
			34	PC12	EIC/EXTINT[4]					SLCD/ LP[19]	SERCOM1/ PAD[0]						
			35	PC13	EIC/EXTINT[5]					SLCD/ LP[20]	SERCOM1/ PAD[1]						
	19	23	38	VLCD													
	20	24	39	PB11	EIC/EXTINT[11]					SLCD/ LP[21]		SERCOM3/ PAD[3]	TC/1/ WO[1]	TCC/ WO[5]			CCL/ OUT[1]
I2C: full Fm+. Limited currents for Sm, Fm		25	40	PB12	EIC/EXTINT[12]					SLCD/ LP[22]	SERCOM3/ PAD[0]		TC/0/ WO[0]	TCC/ WO[6]			
		26	41	PB13	EIC/EXTINT[13]					SLCD/ LP[23]	SERCOM3/ PAD[1]		TC/0/ WO[1]	TCC/ WO[7]			
		27	42	PB14	EIC/EXTINT[14]					SLCD/ LP[24]	SERCOM3/ PAD[2]		TC/1/ WO[0]			GCLK/ IO[0]	CCL/IN[9]
		28	43	PB15	EIC/EXTINT[15]					SLCD/ LP[25]	SERCOM3/ PAD[3]		TC/1/ WO[1]			GCLK/ IO[1]	CCL/ IN[10]
			44	PC14	EIC/EXTINT[6]					SLCD/ LP[26]							
			45	PC15	EIC/EXTINT[7]					SLCD/ LP[27]							
I2C: Sm, Fm, Fm+	21	29	46	PA12	EIC/EXTINT[12]					SLCD/ LP[28]	SERCOM4/ PAD[0]	SERCOM3/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
	22	30	47	PA13	EIC/EXTINT[13]					SLCD/ LP[29]	SERCOM4/ PAD[1]	SERCOM3/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
	23	31	48	PA14	EIC/EXTINT[14]					SLCD/ LP[30]	SERCOM4/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[4]		GCLK/ IO[0]	
	24	32	49	PA15	EIC/EXTINT[15]					SLCD/ LP[31]	SERCOM4/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[5]		GCLK/ IO[1]	
	25	35	52	PA16	EIC/EXTINT[0]				PTC/ X[28]	SLCD/ LP[32]	SERCOM1/ PAD[0]	SERCOM2/ PAD[0]		TCC/ WO[6]		GCLK/ IO[2]	CCL/IN[0]
	26	36	53	PA17	EIC/EXTINT[1]				PTC/ X[29]	SLCD/ LP[33]	SERCOM1/ PAD[1]	SERCOM2/ PAD[1]		TCC/ WO[7]		GCLK/ IO[3]	CCL/IN[1]
	27	37	54	PA18	EIC/EXTINT[2]				PTC/ X[30]	SLCD/ LP[34]	SERCOM1/ PAD[2]	SERCOM2/ PAD[2]		TCC/ WO[2]		AC/ CMP[0]	CCL/IN[2]
	28	38	55	PA19	EIC/EXTINT[3]				PTC/ X[31]	SLCD/ LP[35]	SERCOM1/ PAD[3]	SERCOM2/ PAD[3]		TCC/ WO[3]		AC/ CMP[1]	CCL/ OUT[0]
			56	PC16	EIC/EXTINT[8]					SLCD/ LP[36]							
			57	PC17	EIC/EXTINT[9]					SLCD/ LP[37]							
digital: input only			58	PC18	EIC/EXTINT[10]					SLCD/ LP[38]							
			59	PC19	EIC/EXTINT[11]					SLCD/ LP[39]							
			60	PC20	EIC/EXTINT[12]					SLCD/ LP[40]							CCL/IN[9]
			61	PC21	EIC/EXTINT[13]					SLCD/ LP[41]							CCL/ IN[10]
		39	64	PB16	EIC/EXTINT[0]					SLCD/ LP[42]	SERCOM5/ PAD[0]		TC/2/ WO[0]	TCC/ WO[4]		GCLK/ IO[2]	CCL/IN[11]
		40	65	PB17	EIC/EXTINT[1]					SLCD/ LP[43]	SERCOM5/ PAD[1]		TC/2/ WO[1]	TCC/ WO[5]		GCLK/ IO[3]	CCL/ OUT[3]
			66	PB18	EIC/EXTINT[2]					SLCD/ LP[44]	SERCOM5/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[0]			
			67	PB19	EIC/EXTINT[3]					SLCD/ LP[45]	SERCOM5/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[1]			
			68	PB20	EIC/EXTINT[4]					SLCD/ LP[46]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]		TCC/ WO[2]			
			69	PB21	EIC/EXTINT[5]					SLCD/ LP[47]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]		TCC/ WO[3]			
	29	41	70	PA20	EIC/EXTINT[4]				PTC/ XY[16]	SLCD/ LP[48]	SERCOM0/ PAD[0]	SERCOM2/ PAD[2]	TC/3/ WO[0]	TCC/ WO[6]		GCLK/ IO[4]	
	30	42	71	PA21	EIC/EXTINT[5]				PTC/ XY[17]	SLCD/ LP[49]	SERCOM0/ PAD[1]	SERCOM2/ PAD[3]	TC/3/ WO[1]	TCC/ WO[7]			
I2C: Sm, Fm, Fm+	31	43	72	PA22	EIC/EXTINT[6]				PTC/ XY[18]	SLCD/ LP[50]	SERCOM0/ PAD[2]	SERCOM2/ PAD[0]	TC/0/ WO[0]	TCC/ WO[4]			CCL/IN[6]
	32	44	73	PA23	EIC/EXTINT[7]				PTC/ XY[19]	SLCD/ LP[51]	SERCOM0/ PAD[3]	SERCOM2/ PAD[1]	TC/0/ WO[1]	TCC/ WO[5]	USB/SOF_1KHZ		CCL/IN[7]
	33	45	74	PA24	EIC/EXTINT[12]						SERCOM2/ PAD[2]	SERCOM5/ PAD[0]	TC/1/ WO[0]	TCC/ WO[0]	USB/DM		CCL/IN[8]
	34	46	75	PA25	EIC/EXTINT[13]						SERCOM2/ PAD[3]	SERCOM5/ PAD[1]	TC/1/ WO[1]	TCC/ WO[1]	USB/DP		CCL/ OUT[2]
	37	49	78	PB22	EIC/EXTINT[6]						SERCOM0/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]	TCC/ WO[2]	USB/SOF_1KHZ	GCLK/ IO[0]	CCL/IN[0]

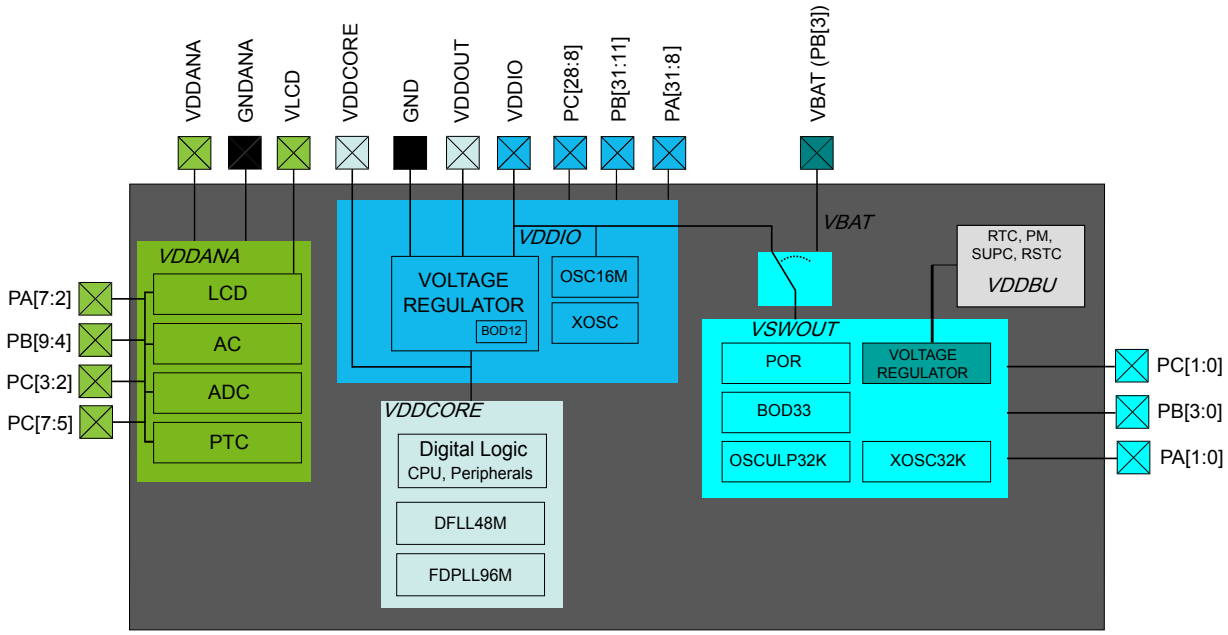
7.2.4. GPIO Pin Clusters

Table 7-6. GPIO Clusters

Package	Cluster	GPIO	Supplies Pin connected to the cluster	
100 pins	1	PA02, PA03, PB04, PB05, PC02, PC03	V_{DDANA} pin12	GNDANA pin11
	2	PA04, PA05, PA06, PA07, PB06, PB07, PB08, PB09, PC05, PC06, PC07	V_{DDANA} pin12, V_{DDANA} pin25	GNDANA pin11, GNDANA pin24
	3	PA08, PA09, PA10, PA11, PC08, PC09, PC10, PC11, PC12, PC13	V_{DDIO} pin36	GND pin37
	4	PA12, PA13, PA14, PA15, PB11, PB12, PB13, PB14, PB15, PC14, PC15	V_{DDIO} pin36, V_{DDIO} pin51	GND pin37, GND pin50
	5	PA16, PA17, PA18, PA19, PC16, PC17, PC18, PC19, PC20, PC21	V_{DDIO} pin51, V_{DDIO} pin63	GND pin50, GND pin62
	6	PA20, PA21, PA22, PA23, PA24, PA25, PB16, PB17, PB18, PB19, PB20, PB21	V_{DDIO} pin63, V_{DDIO} pin77	GND pin62, GND pin76
	7	PA27, PB22, PB23, PB24, PB25, PC24, PC25, PC26, PC27, PC28	V_{DDIO} pin77, V_{DDIO} pin92	GND pin76, GND pin90
	8	PA00, PA01, PA30, PA31, PB00, PB01, PB02, PB03, PB30, PB31, PC00, PC01	V_{DDIO} pin92	GND pin90
64 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB04, PB05, PB06, PB07, PB08, PB09	V_{DDANA} pin8	GNDANA pin7
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin21	GND pin22
	3	PA12, PA13, PA14, PA15, PB11, PB12, PB13, PB14, PB15	V_{DDIO} pin21, V_{DDIO} pin34	GND pin22, GND pin33
	4	PA16, PA17, PA18, PA19, PA20, PA21, PA22, PA23, PA24, PA25, PB16, PB17	V_{DDIO} pin34, V_{DDIO} pin48	GND pin33, GND pin47
	5	PA27, PB22, PB23	V_{DDIO} pin48, V_{DDIO} pin56	GND pin47, GND pin54
	6	PA00, PA01, PA30, PA31, PB00, PB01, PB02, PB03, PB30, PB31	V_{DDIO} pin56	GND pin54
48 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB08, PB09	V_{DDANA} pin6	GNDANA pin5
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin17	GND pin18
	3	PA12, PA13, PA14, PA15, PA16, PA17, PA18, PA19, PA20, PA21, PA22, PA23, PA24, PA25, PB11	V_{DDIO} pin17, V_{DDIO} pin36	GND pin18, GND pin35
	4	PA27, PB22, PB23	V_{DDIO} pin36, V_{DDIO} pin44	GND pin35, GND pin42
	5	PA00, PA01, PA30, PA31, PB02, PB03	V_{DDIO} pin44	GND pin42
49 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB08, PB09	V_{DDANA} pin D7	GNDANA pin C7
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin G5	GND pin F5
	3	PA12, PA13, PA14, PA15, PA16, PA17, PA18, PA19, PB11	V_{DDIO} pin G5, V_{DDIO} pin E1	GND pin F5, GND pin E2
	4	PA20, PA21, PA22, PA23, PA24, PA25	V_{DDIO} pin E1, V_{DDIO} pin A5	GND pin E2, GND pin D4
	4	PA27, PB22, PB23	V_{DDIO} pin E1, V_{DDIO} pin A5	GND pin D4, GND pin B3
	5	PA00, PA01, PA30, PA31, PB02, PB03	V_{DDIO} pin A5	GND pin B3

8. Power Supply and Start-Up Considerations

8.1. Power Domain Overview



The Atmel SAM L22 power domains are not independent of each other:

- VDDCORE and VDDIO share GND, whereas VDDANA refers to GNDANA.
- VDDCORE serves as the internal voltage regulator output.
- VSWOUT and VDDBU are internal power domains.

8.2. Power Supply Considerations

8.2.1. Power Supplies

The Atmel SAM L22 has several different power supply pins:

- VDDIO powers I/O lines and OSC16M, XOSC, the internal regulator for VDDCORE and the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDANA powers I/O lines and the ADC, AC, LCD, and PTC. Voltage is 1.62V to 3.63V
- VLCD has two alternative functions:
  - Output of the LCD voltage pump when VLCD is generated internally. Output voltage is 2.5V to 3.5V.
  - Supply input for the bias generator when VLCD is provided externally by the application. Input voltage is 2.4 to 3.6V.
- VBAT powers the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDCORE serves as the internal voltage regulator output. It powers the core, memories, peripherals, DFLL48M and FDPLL96M. Voltage is 0.9V to 1.2V typical.
- The Automatic Power Switch is a configurable switch that selects between VDDIO and VBAT as supply for the internal output VSWOUT, see the figure in Power Domain Overview.

The same voltage must be applied to both VDDIO and VDDANA. This common voltage is referred to as VDD in the datasheet.

The ground pins, GND, are common to VDDCORE, and VDDIO. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

8.2.2. Voltage Regulator

The SAM L22 internal Voltage Regulator has four different modes:

- Linear mode : This is the default mode when CPU and peripherals are running. It does not require an external inductor.
- Switching mode. This is the most efficient mode when the CPU and peripherals are running. This mode can be selected by software on the fly.
- Low Power (LP) mode. This is the default mode used when the chip is in standby mode.
- Shutdown mode. When the chip is in backup mode, the internal regulator is off.

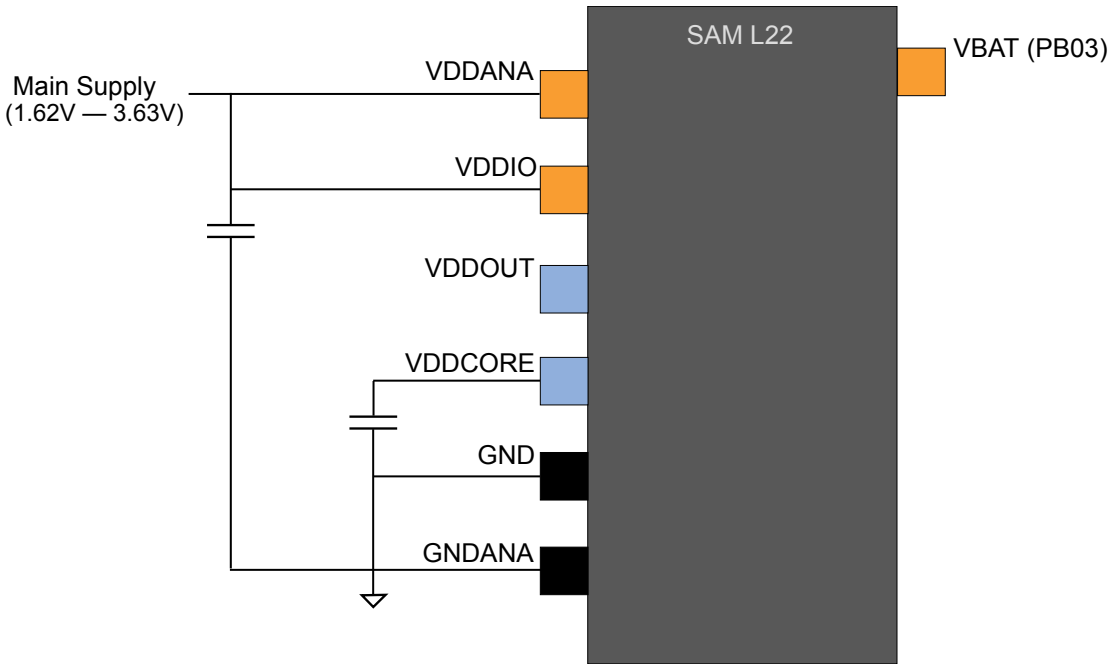
Note that the Voltage Regulator modes are controlled by the Power Manager.

8.2.3. Typical Powering Schematic

The SAM L22 uses a single supply from 1.62V to 3.63V.

The following figure shows the recommended power supply connection.

Figure 8-1. Power Supply Connection for Linear Mode Only



8.4.4. Brown-Out Detector on VDDCORE

Once the device has started up, BOD12 monitors the internal VDDCORE.

8.5. Performance Level Overview

By default, the device will start in Performance Level 0. This PL0 is aiming for the lowest power consumption by limiting logic speeds and the CPU frequency. As a consequence, all GCLK will have limited capabilities, and some peripherals and clock sources will not work or with limited capabilities:

List of peripherals/clock sources not available in PL0:

- USB (limited by logic frequency)
- DFLL48M

List of peripherals/clock sources with limited capabilities in PL0:

- All AHB/APB peripherals are limited by CPU frequency
- DPLL96M: may be able to generate 48MHz internally, but the output cannot be used by logic
- GCLK: the maximum frequency is by factor 4 compared to PL2
- SW interface: the maximum frequency is by factor 4 compared to PL2
- TC: the maximum frequency is by factor 4 compared to PL2
- TCC:the maximum frequency is by factor 4 compared to PL2
- SERCOM: the maximum frequency is by factor 4 compared to PL2

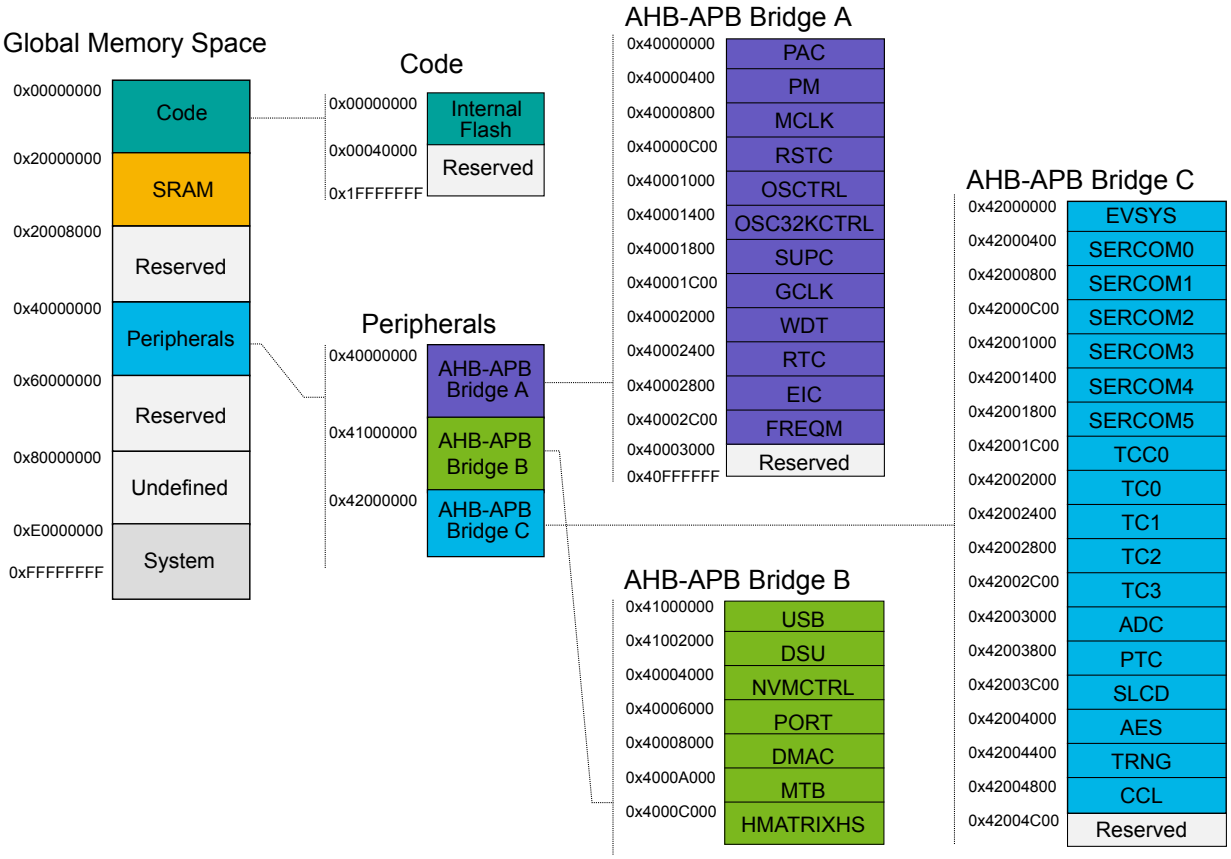
List of peripherals/clock sources with full capabilities in PL0:

- AC
- ADC
- EIC
- OSC16M
- PTC
- All 32KHz clock sources and peripherals

Full functionality and capability will be ensured in PL2. When transitioning between performance levels, the Supply Controller (SUPC) will provide a configurable smooth voltage scaling transition.

9. Product Mapping

Figure 9-1. Atmel SAM L22 Product Mapping



10. Memories

10.1. Embedded Memories

- Internal high-speed Flash with Read-While-Write (RWW) capability on a section of the array
- Internal high-speed RAM, single-cycle access at full speed

10.2. Physical Memory Map

The high-speed bus is implemented as a bus matrix. All high-speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follows:

Table 10-1. SAM L22 Physical Memory Map

Memory	Start address	Size [KB]		
		SAML22x18(1)	SAML22x17(1)	SAML22x16(1)
Embedded Flash	0x00000000	256	128	64
Embedded RWW section	0x00400000	8	4	2
Embedded SRAM	0x20000000	32	16	8
Peripheral Bridge A	0x40000000	64	64	64
Peripheral Bridge B	0x41000000	64	64	64
Peripheral Bridge C	0x42000000	64	64	64
IOBUS	0x60000000	0.5	0.5	0.5

Note: 1. x = G, J, or E.

Table 10-2. Flash Memory Parameters

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	256	4096	64
SAML22x17(1)	128	2048	64
SAML22x16(1)	64	1024	64

Note: 1. x = G, J, or E.

Table 10-3. RWW Section Parameters(1)

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	8	128	64
SAML22x17(1)	4	64	64
SAML22x16(1)	2	32	64

Note: 1. x = G, J, or E.

10.3. NVM User Row Mapping

The Non Volatile Memory (NVM) User Row contains calibration data that are automatically read at device power-on.

The NVM User Row can be read at address 0x00804000.

To write the NVM User Row refer to the documentation of the NVMCTRL - Non-Volatile Memory Controller.

Note: When writing to the User Row, the new values do not get loaded by the other peripherals on the device until a device Reset occurs.

Table 10-4. NVM User Row Mapping

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	0x7	NVMCTRL
3	Reserved	—	0x1	—
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	0x7	NVMCTRL
7	Reserved	—	0x1	—
13:8	BOD33 Level	BOD33 threshold level at power-on.	0x06	SUPC.BOD33
14	BOD33 Disable	BOD33 Disable at power-on.	0x0	SUPC.BOD33
16:15	BOD33 Action	BOD33 Action at power-on.	0x1	SUPC.BOD33
25:17	Reserved	Factory settings - do not change.	0x08F	-
26	WDT Enable	WDT Enable at power-on.	0x0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power-on.	0x0	WDT.CTRLA
31:28	WDT Period	WDT Period at power-on.	0xB	WDT.CONFIG
35:32	WDT Window	WDT Window mode time-out at power-on.	0xB	WDT.CONFIG
39:36	WDT EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on.	0xB	WDT.EWCTRL
40	WDT WEN	WDT Timer Window Mode Enable at power-on.	0x0	WDT.CTRLA
41	BOD33 Hysteresis	BOD33 Hysteresis configuration at power-on.	0x0	SUPC.BOD33
47:42	Reserved	Factory settings - do not change.	0x3E	—
63:48	LOCK	NVM Region Lock Bits.	0xFFFF	NVMCTRL

11.2. Nested Vector Interrupt Controller

11.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM L22 supports 32 interrupts with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).

11.2.2. Interrupt Line Mapping

Each of the interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a '1' to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing '1' to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 11-3. Interrupt Line Mapping

Peripheral source	NVIC line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32KHz Oscillators Controller PAC - Peripheral Access Controller SUPC - Supply Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Counter	2
EIC – External Interrupt Controller	3
FREQM - Frequency Meter	4
USB - Universal Serial Bus	5
NVMCTRL – Non-Volatile Memory Controller	6
DMAC - Direct Memory Access Controller	7

High-Speed Bus Matrix Slaves	Slave ID
AHB-APB Bridge C	5
SRAM Port 2 - DMAC Data Access	6

11.4.4. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, priority levels can be assigned to the masters for different types of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM, the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in the table below.

Table 11-6. Quality of Service

Value	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be a minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by the port ID. The lowest port ID has the highest static priority. See the tables below for details.

The MTB has a fixed QoS level HIGH (0x3).

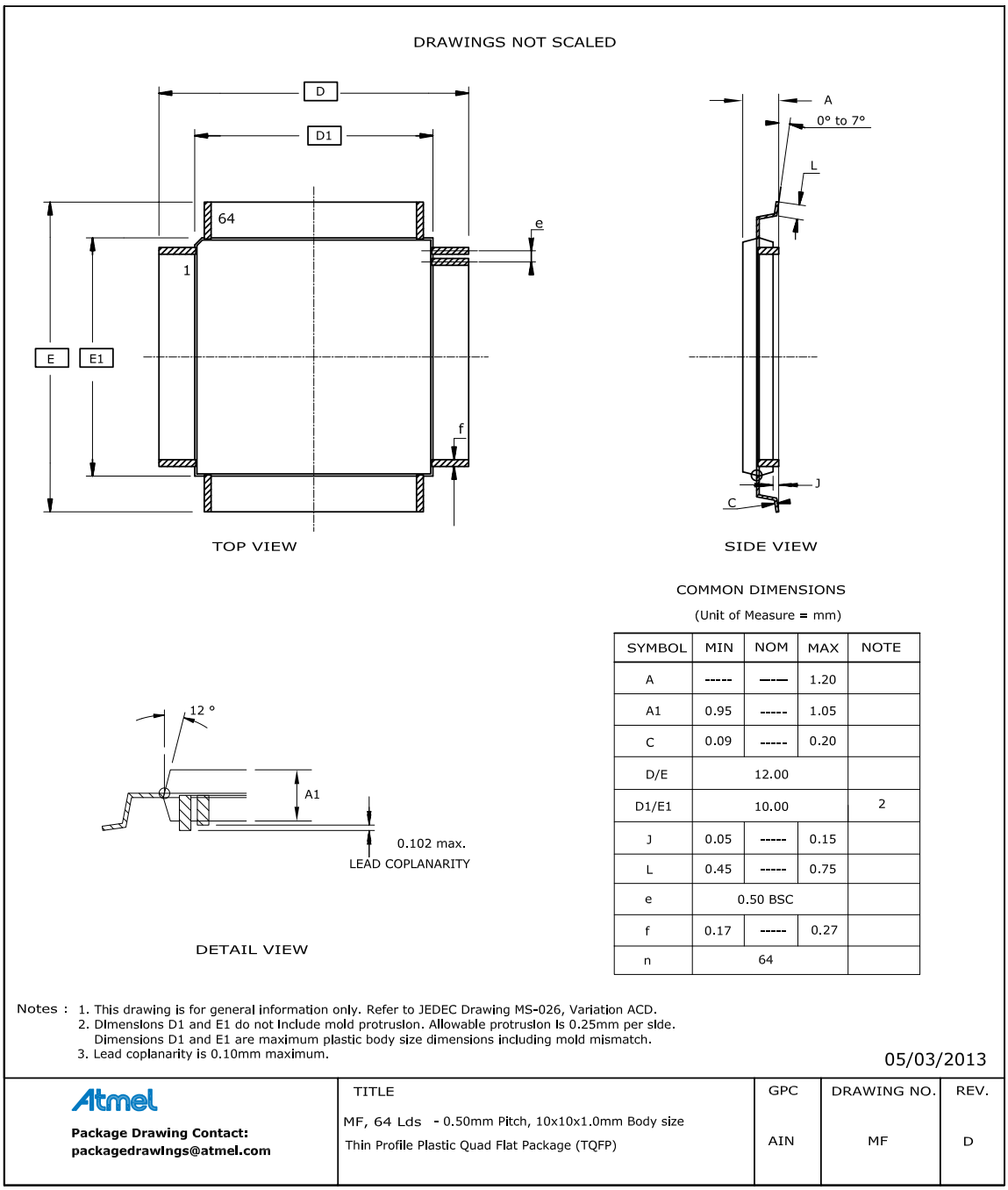
The CPU QoS level can be written/read, using 32-bit access only, at address 0x4100C114, bits [1:0]. Its reset value is 0x3.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

Table 11-7. SRAM Port Connections QoS

SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
CM0+ - Cortex M0+ Processor	0	Bus Matrix	0x4100C114, bits[1:0](1)	0x3
DSU - Device Service Unit	1	Bus Matrix	0x4100201C, bits[1:0](1)	0x2
DMAC - Direct Memory Access Controller - Data Access	2	Bus Matrix	IP-QOSCTRL.DQOS	0x2

12.2.2. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AIN	MF	D

Table 12-5. Device and Package Maximum Weight

300	mg

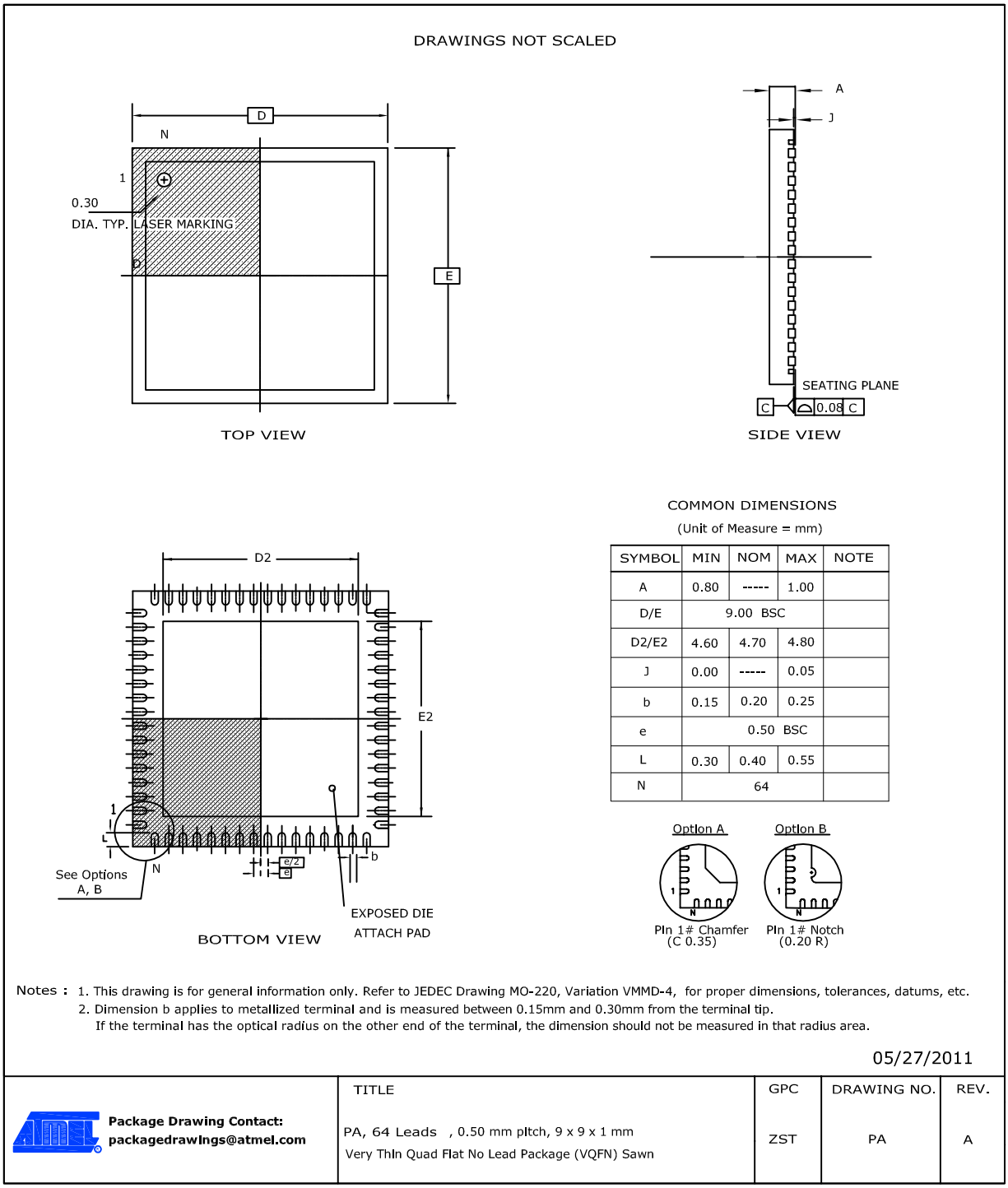
Table 12-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-7. Package Reference

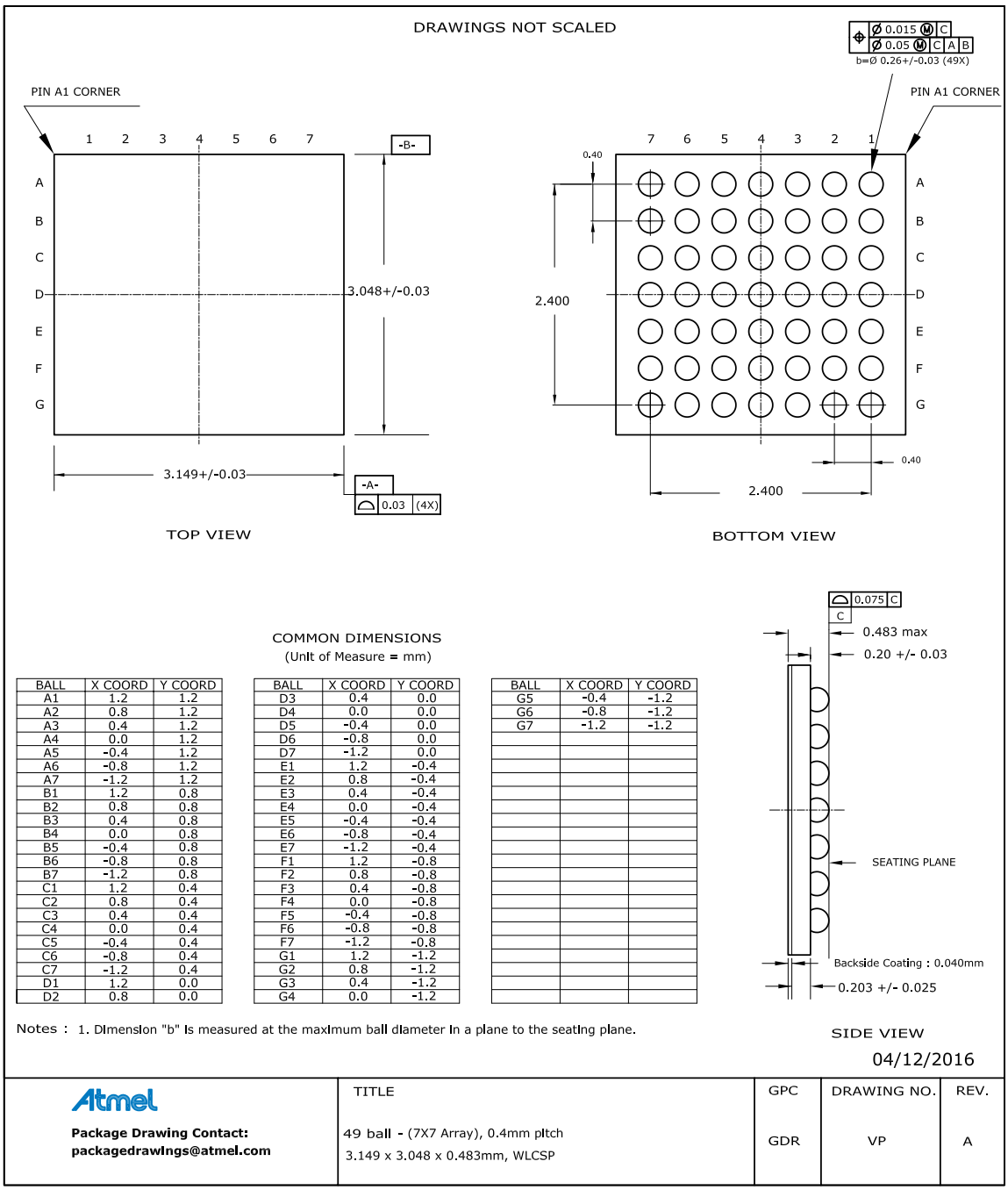
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.3. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

12.2.4. 49-Ball WLCSP



BALL	X COORD	Y COORD
A1	1.2	1.2
A2	0.8	1.2
A3	0.4	1.2
A4	0.0	1.2
A5	-0.4	1.2
A6	-0.8	1.2
A7	-1.2	1.2
B1	1.2	0.8
B2	0.8	0.8
B3	0.4	0.8
B4	0.0	0.8
B5	-0.4	0.8
B6	-0.8	0.8
B7	-1.2	0.8
C1	1.2	0.4
C2	0.8	0.4
C3	0.4	0.4
C4	0.0	0.4
C5	-0.4	0.4
C6	-0.8	0.4
C7	-1.2	0.4
D1	1.2	0.0
D2	0.8	0.0

BALL	X COORD	Y COORD
D3	0.4	0.0
D4	0.0	0.0
D5	-0.4	0.0
D6	-0.8	0.0
D7	-1.2	0.0
E1	1.2	-0.4
E2	0.8	-0.4
E3	0.4	-0.4
E4	0.0	-0.4
E5	-0.4	-0.4
E6	-0.8	-0.4
E7	-1.2	-0.4
F1	1.2	-0.8
F2	0.8	-0.8
F3	0.4	-0.8
F4	0.0	-0.8
F5	-0.4	-0.8
F6	-0.8	-0.8
F7	-1.2	-0.8
G1	1.2	-1.2
G2	0.8	-1.2
G3	0.4	-1.2
G4	0.0	-1.2

BALL	X COORD	Y COORD
G5	-0.4	-1.2
G6	-0.8	-1.2
G7	-1.2	-1.2

Table 12-11. Device and Package Maximum Weight

8.45	mg

Table 12-12. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 12-13. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

12.2.5. 48 pin TQFP

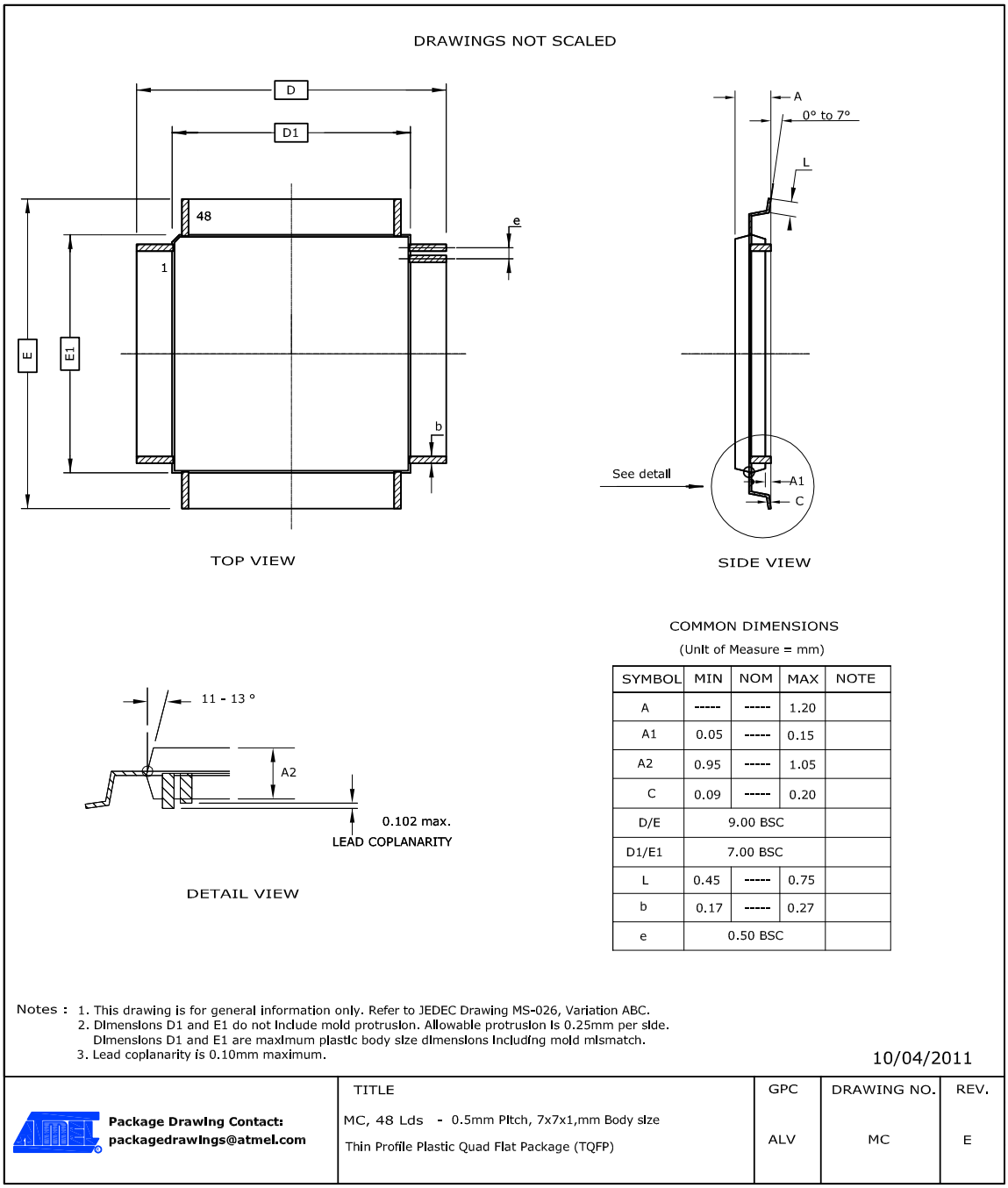


Table 12-14. Device and Package Maximum Weight

140	mg