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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22j17a-aut

- Battery backup support
- Two runtime selectable power/performance levels
- Embedded Buck/LDO regulator supporting on-the-fly selection
- Active mode: <50µA/MHz
- Standby with full retention, RTC and LCD = 3.47µA
  - 2.1µs wake-up time
- Standby with full retention and RTC: 1.87µA
  - 2.1µs wake-up time
- Ultra low power Backup mode with RTC: 490nA
  - 90µs wake-up time

- Peripherals
  - Segment LCD controller
    - Up to 8 (4) common and 40 (44) segment terminals to drive 320 (176) segments
    - Static, ½, 1/3, ¼ bias
    - Internal charge pump able to generate VLCD higher than VDDIO
  - 16-channel Direct Memory Access Controller (DMAC)
  - 8-channel Event System
  - Up to four 16-bit Timer/Counters (TC), each configurable as:
    - 16-bit TC with two compare/capture channels
    - 8-bit TC with two compare/capture channels
    - 32-bit TC with two compare/capture channels, by using two TCs
  - One 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - Frequency Meter
  - 32-bit Real Time Counter (RTC) with clock/calendar function
    - 8x32-bit Backup Register
    - Tamper Detection
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 Device
    - Eight endpoints
    - Crystal less operation
  - Up to six Serial Communication Interfaces (SERCOM), each configurable as:
    - USART with full-duplex and single-wire half-duplex configuration
    - ISO7816
    - I^2C up to 3.4MHz[1]
    - SPI
  - One AES encryption engine

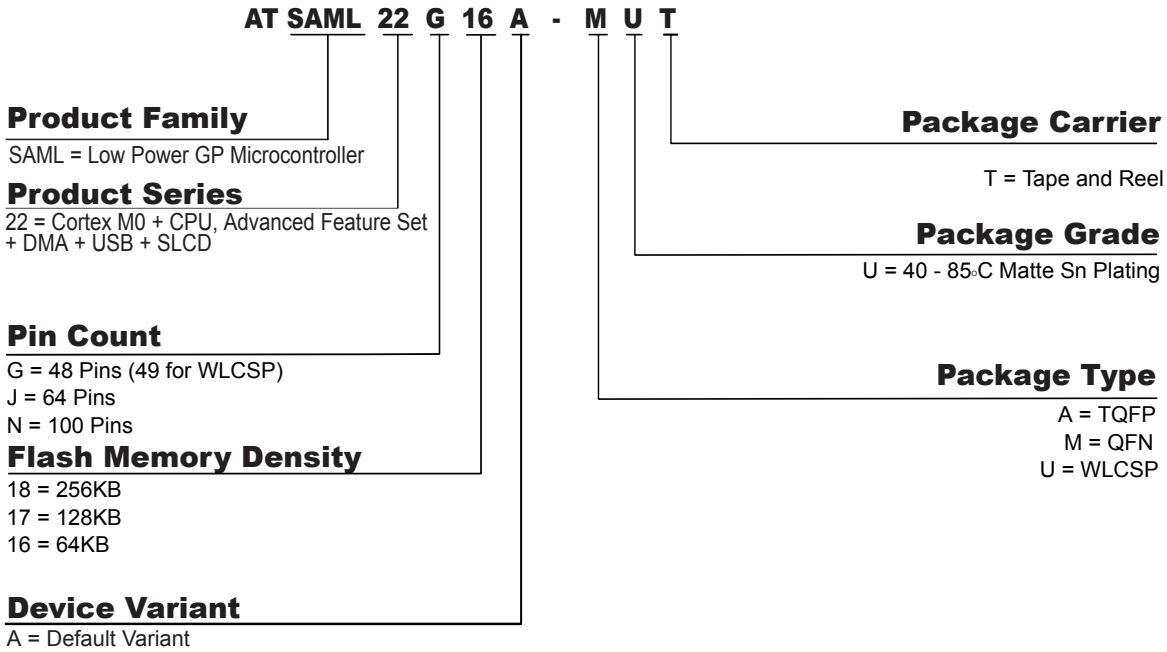
[1] Max 1 high-speed mode and max 3 fast mode I^2C

  - One True Random Generator (TRNG)
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - Up to 256-Channel capacitive touch sensing
      - Maximum Mutual-Cap up to 16x16 channels
      - Maximum Self-Cap up to 24 channels
    - Wake-up on touch in standby mode
- Oscillators
  - 32.768kHz crystal oscillator (XOSC32K)
  - 0.4-32MHz crystal oscillator (XOSC)
  - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
  - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
  - 48MHz Digital Frequency Locked Loop (DFLL48M)
  - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
  - Up to 82 programmable I/O pins
  - Up to 52 segment LCD pins can be used as GPIO/GPI
  - Up to 5 wake-up pins with optional debouncing
  - Up to 5 tamper input pins
  - 1 tamper output pin
- Pin and code compatible with SAM D and SAM L Cortex-M0+ Families[2]
- Packages
  - 100-pin TQFP
  - 64-pin TQFP, QFN
  - 49-pin WLCSP
  - 48-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V

[2] except the VLCD

Table of Contents

3. Ordering Information



Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

3.1. SAM L22N

Table 3-1. SAM L22N Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22N16A-AUT	64K	8K	TQFP100	Tape & Reel
ATSAML22N17A-AUT	128K	16K	TQFP100	Tape & Reel
ATSAML22N18A-AUT	256K	32K	TQFP100	Tape & Reel

3.2. SAM L22J

Table 3-2. SAM L22J Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J16A-AUT	64K	8K	TQFP64	Tape & Reel
ATSAML22J16A-MUT			QFN64	
ATSAML22J17A-AUT	128K	16K	TQFP64	Tape & Reel
ATSAML22J17A-MUT			QFN64	

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML22J18A-MUT			QFN64	

3.3. SAM L22G

Table 3-3. SAM L22G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML22G16A-MUT			QFN48	
ATSAML22G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML22G17A-MUT			QFN48	
ATSAML22G17A-UUT			WLCSP49	
ATSAML22G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML22G18A-MUT			QFN48	
ATSAML22G18A-UUT			WLCSP49	

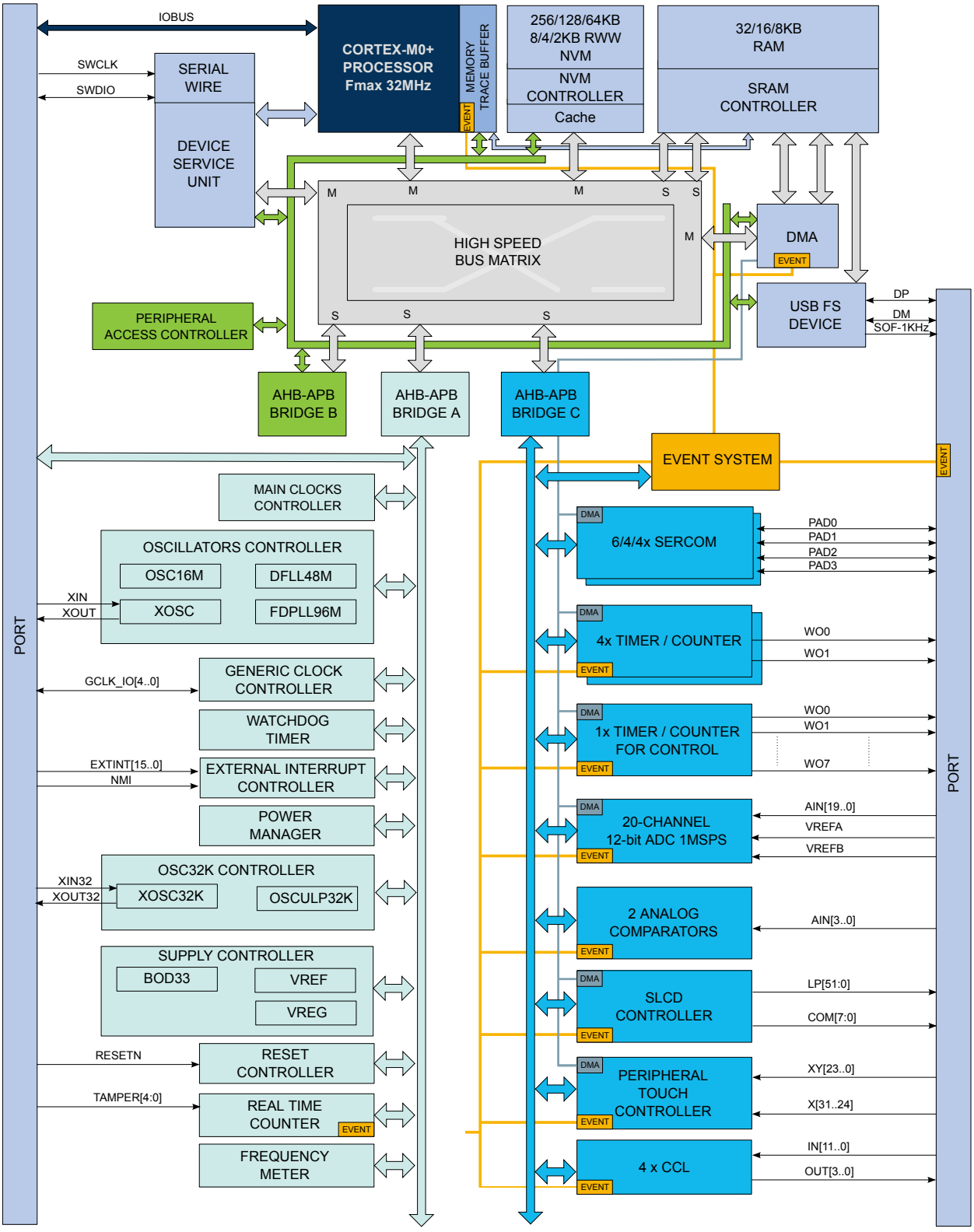
3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

Table 3-4. SAM L22 Device Identification Values

DSU DID.DEVSEL	Device
0x0	L22N18
0x1	L22N17
0x2	L22N16
0x3-0x4	Reserved
0x5	L22J18
0x6	L22J17
0x7	L22J16
0x8-0x9	Reserved
0xA	L22G18
0xB	L22G17
0xC	L22G16
0xD-0xFF	Reserved

4. Block Diagram



Note:

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PB22
		XOUT	PB23
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Table 7-3. XOSC32K Jitter Minimization

Package	Steady Signal Recommended
L22N	PB00, PB01, PB02, PB03, PC00, PC01
L22J	PB00, PB01, PB02, PB03, PA02, PA03
L22G	PB02, PB03, PA02, PA03

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

7.2.3. SERCOM USART and I²C Configurations

The SAM L22 has up to six instances of the serial communication interface (SERCOM) peripheral. The following table lists the supported communication protocols for each SERCOM instance.

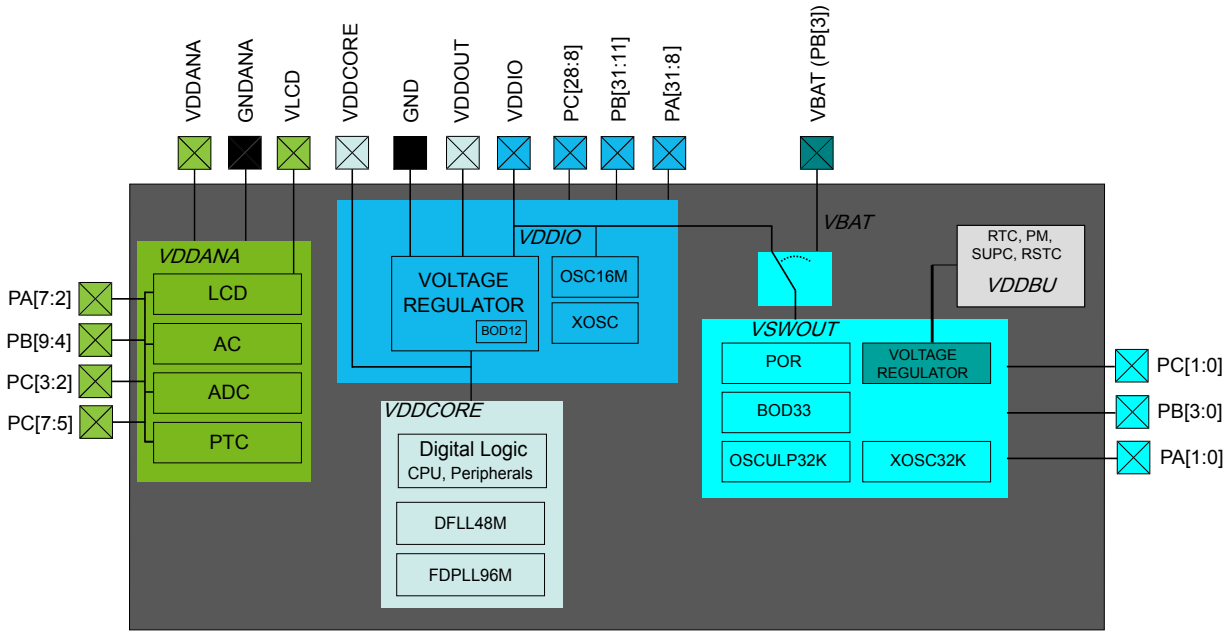
Table 7-5. SERCOM USART and I²C Protocols

	SERCOM Instance					
Protocol	SERCOM0	SERCOM1	SERCOM2	SERCOM3	SERCOM4	SERCOM5
I²C	no	yes	yes	yes	yes	yes
I²C at 3.4MHz	no	yes	no	no	no	yes
USART including RS485 and ISO 7816	yes	yes	yes	yes	yes	yes
SPI	yes	yes	yes	yes	yes	yes

Note: Not all available I²C pins support I²C mode at 3.4MHz.

8. Power Supply and Start-Up Considerations

8.1. Power Domain Overview



The Atmel SAM L22 power domains are not independent of each other:

- VDDCORE and VDDIO share GND, whereas VDDANA refers to GNDANA.
- VDDCORE serves as the internal voltage regulator output.
- VSWOUT and VDDBU are internal power domains.

8.2. Power Supply Considerations

8.2.1. Power Supplies

The Atmel SAM L22 has several different power supply pins:

- VDDIO powers I/O lines and OSC16M, XOSC, the internal regulator for VDDCORE and the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDANA powers I/O lines and the ADC, AC, LCD, and PTC. Voltage is 1.62V to 3.63V
- VLCD has two alternative functions:
  - Output of the LCD voltage pump when VLCD is generated internally. Output voltage is 2.5V to 3.5V.
  - Supply input for the bias generator when VLCD is provided externally by the application. Input voltage is 2.4 to 3.6V.
- VBAT powers the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDCORE serves as the internal voltage regulator output. It powers the core, memories, peripherals, DFLL48M and FDPLL96M. Voltage is 0.9V to 1.2V typical.
- The Automatic Power Switch is a configurable switch that selects between VDDIO and VBAT as supply for the internal output VSWOUT, see the figure in Power Domain Overview.

10. Memories

10.1. Embedded Memories

- Internal high-speed Flash with Read-While-Write (RWW) capability on a section of the array
- Internal high-speed RAM, single-cycle access at full speed

10.2. Physical Memory Map

The high-speed bus is implemented as a bus matrix. All high-speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follows:

Table 10-1. SAM L22 Physical Memory Map

Memory	Start address	Size [KB]		
		SAML22x18(1)	SAML22x17(1)	SAML22x16(1)
Embedded Flash	0x00000000	256	128	64
Embedded RWW section	0x00400000	8	4	2
Embedded SRAM	0x20000000	32	16	8
Peripheral Bridge A	0x40000000	64	64	64
Peripheral Bridge B	0x41000000	64	64	64
Peripheral Bridge C	0x42000000	64	64	64
IOBUS	0x60000000	0.5	0.5	0.5

Note: 1. x = G, J, or E.

Table 10-2. Flash Memory Parameters

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	256	4096	64
SAML22x17(1)	128	2048	64
SAML22x16(1)	64	1024	64

Note: 1. x = G, J, or E.

Table 10-3. RWW Section Parameters(1)

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	8	128	64
SAML22x17(1)	4	64	64
SAML22x16(1)	2	32	64

Note: 1. x = G, J, or E.

10.3. NVM User Row Mapping

The Non Volatile Memory (NVM) User Row contains calibration data that are automatically read at device power-on.

The NVM User Row can be read at address 0x00804000.

To write the NVM User Row refer to the documentation of the NVMCTRL - Non-Volatile Memory Controller.

Note: When writing to the User Row, the new values do not get loaded by the other peripherals on the device until a device Reset occurs.

Table 10-4. NVM User Row Mapping

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	0x7	NVMCTRL
3	Reserved	—	0x1	—
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	0x7	NVMCTRL
7	Reserved	—	0x1	—
13:8	BOD33 Level	BOD33 threshold level at power-on.	0x06	SUPC.BOD33
14	BOD33 Disable	BOD33 Disable at power-on.	0x0	SUPC.BOD33
16:15	BOD33 Action	BOD33 Action at power-on.	0x1	SUPC.BOD33
25:17	Reserved	Factory settings - do not change.	0x08F	-
26	WDT Enable	WDT Enable at power-on.	0x0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power-on.	0x0	WDT.CTRLA
31:28	WDT Period	WDT Period at power-on.	0xB	WDT.CONFIG
35:32	WDT Window	WDT Window mode time-out at power-on.	0xB	WDT.CONFIG
39:36	WDT EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on.	0xB	WDT.EWCTRL
40	WDT WEN	WDT Timer Window Mode Enable at power-on.	0x0	WDT.CTRLA
41	BOD33 Hysteresis	BOD33 Hysteresis configuration at power-on.	0x0	SUPC.BOD33
47:42	Reserved	Factory settings - do not change.	0x3E	—
63:48	LOCK	NVM Region Lock Bits.	0xFFFF	NVMCTRL

10.4. NVM Software Calibration Area Mapping

The NVM Software Calibration Area contains calibration data that are determined and written during production test. These calibration values should be read by the application software and written back to the corresponding register.

The NVM Software Calibration Area can be read at address 0x00806020.

The NVM Software Calibration Area can not be written.

Table 10-5. NVM Software Calibration Area Mapping

Bit Position	Name	Description
2:0	ADC LINEARITY	ADC Linearity Calibration. Should be written to CALIB register.
5:3	ADC BIASCAL	ADC Bias Calibration. Should be written to CALIB register.
12:6	Reserved	Reserved for future use.
17:13	USB TRANSN	USB TRANSN calibration value. Should be written to the USB PADCAL register.
22:18	USB TRANSP	USB TRANSP calibration value. Should be written to the USB PADCAL register.
25:23	USB TRIM	USB TRIM calibration value. Should be written to the USB PADCAL register.
31:26	DFLL48M COARSE CAL	DFLL48M Coarse calibration value. Should be written to the OSCCTRL DFLLVAL register.

10.5. Serial Number

Each device has a unique 128-bit serial number which is a concatenation of four 32-bit words contained at the following addresses:

Word 0: 0x0080A00C

Word 1: 0x0080A040

Word 2: 0x0080A044

Word 3: 0x0080A048

The uniqueness of the serial number is guaranteed only when using all 128 bits.

11.2. Nested Vector Interrupt Controller

11.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM L22 supports 32 interrupts with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).

11.2.2. Interrupt Line Mapping

Each of the interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a '1' to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing '1' to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 11-3. Interrupt Line Mapping

Peripheral source	NVIC line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32KHz Oscillators Controller PAC - Peripheral Access Controller SUPC - Supply Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Counter	2
EIC – External Interrupt Controller	3
FREQM - Frequency Meter	4
USB - Universal Serial Bus	5
NVMCTRL – Non-Volatile Memory Controller	6
DMAC - Direct Memory Access Controller	7

11.4.3. Configuration

Figure 11-1. Master-Slave Relations High-Speed Bus Matrix

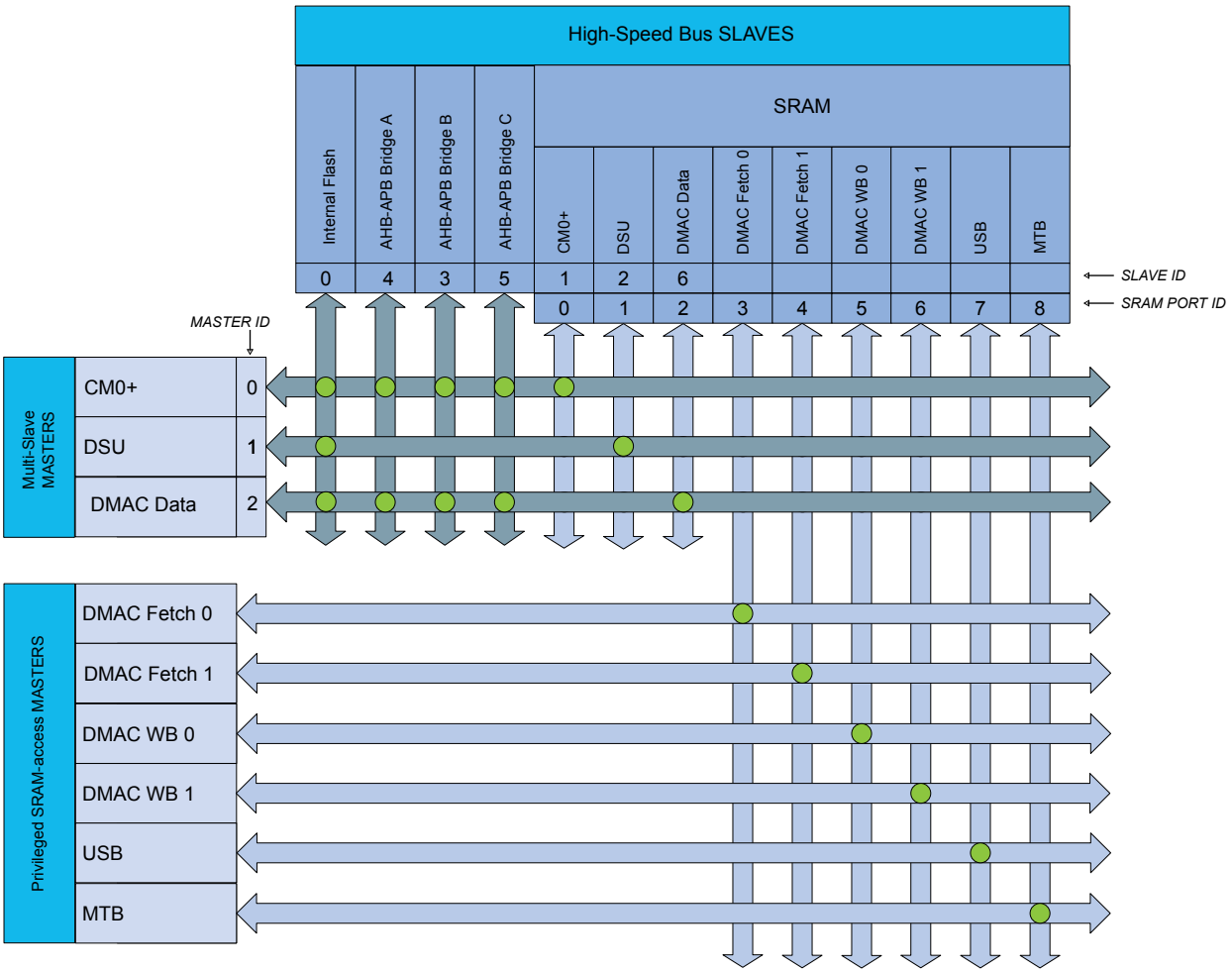


Table 11-4. High Speed Bus Matrix Masters

High-Speed Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1
DMAC - Direct Memory Access Controller / Data Access	2

Table 11-5. High-Speed Bus Matrix Slaves

High-Speed Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
SRAM Port 0 - CM0+ Access	1
SRAM Port 1 - DSU Access	2
AHB-APB Bridge B	3
AHB-APB Bridge A	4

12. Packaging Information

12.1. Thermal Considerations

12.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 12-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
48-pin TQFP	64.2°C/W	12.3°C/W
64-pin TQFP	60.8°C/W	12.0°C/W
100-pin TQFP	58.5°C/W	12.7°C/W
48-pin QFN	32.4°C/W	11.2°C/W
64-pin QFN	32.7°C/W	10.8°C/W
49-pin WLCSP	37.3°C/W	5.8°C/W

Related Links

Junction Temperature on page 42

12.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

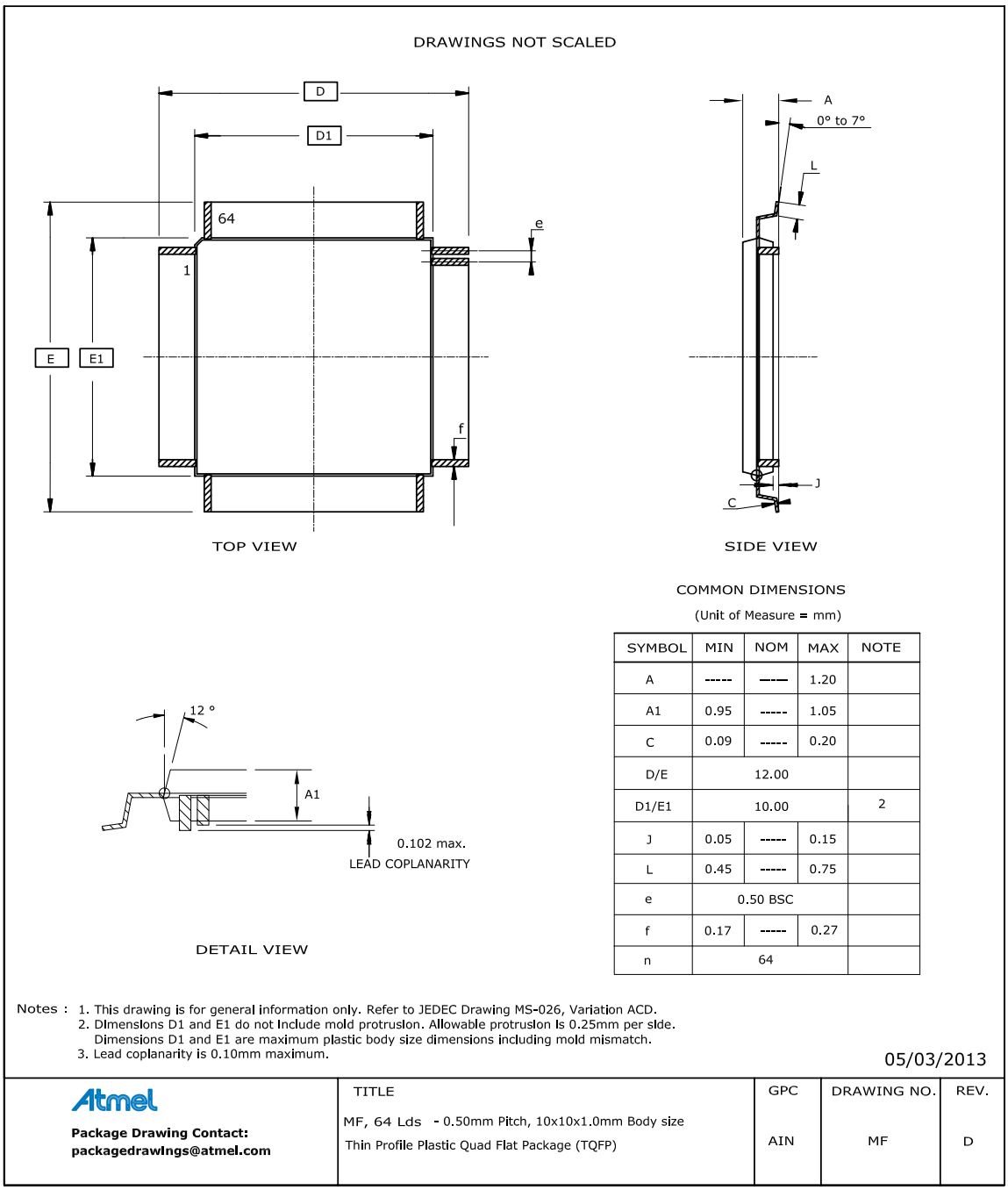
- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Related Links

Thermal Resistance Data on page 42

12.2.2. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AIN	MF	D

Table 12-5. Device and Package Maximum Weight

300	mg

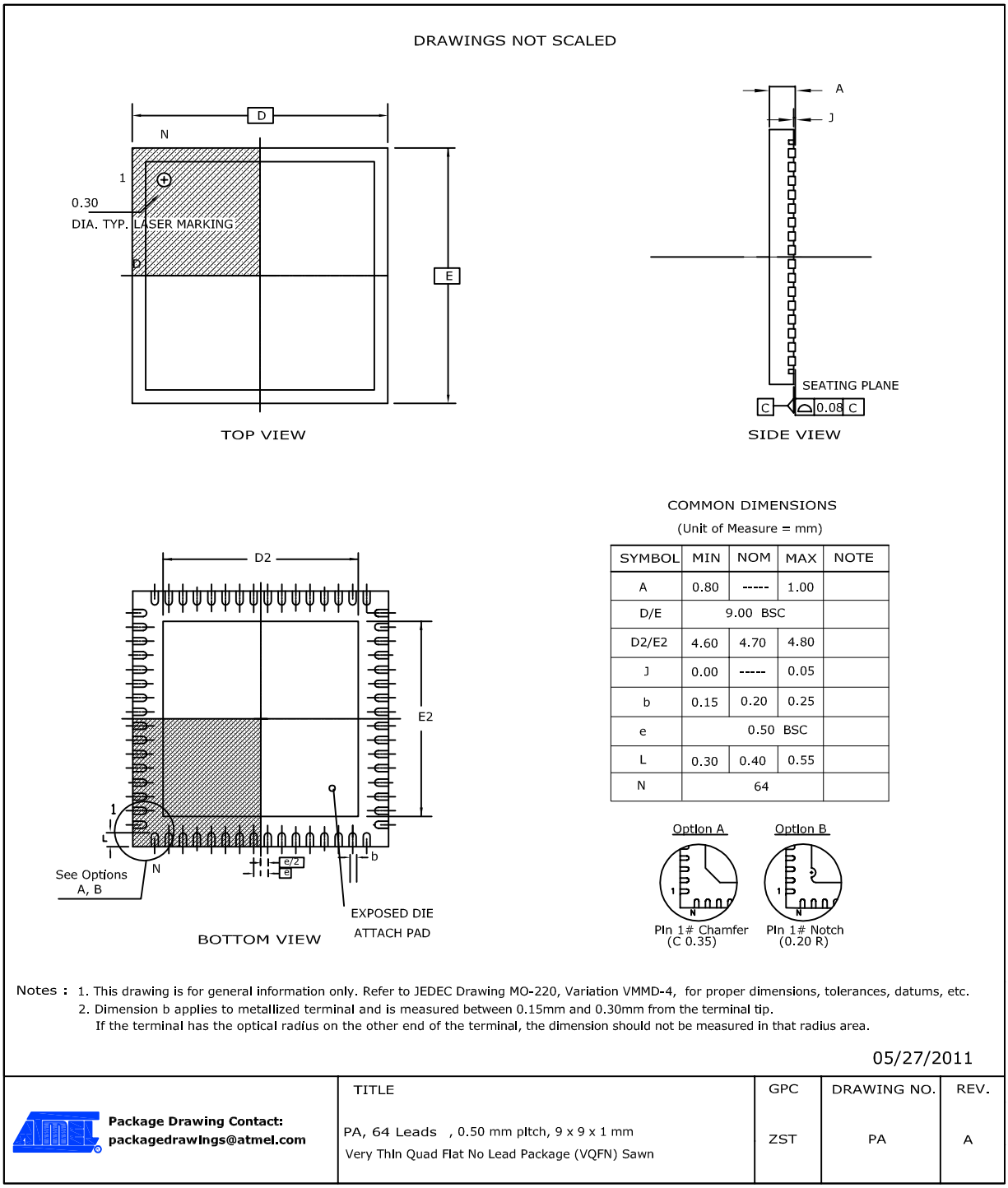
Table 12-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.3. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 12-8. Device and Package Maximum Weight

200	mg

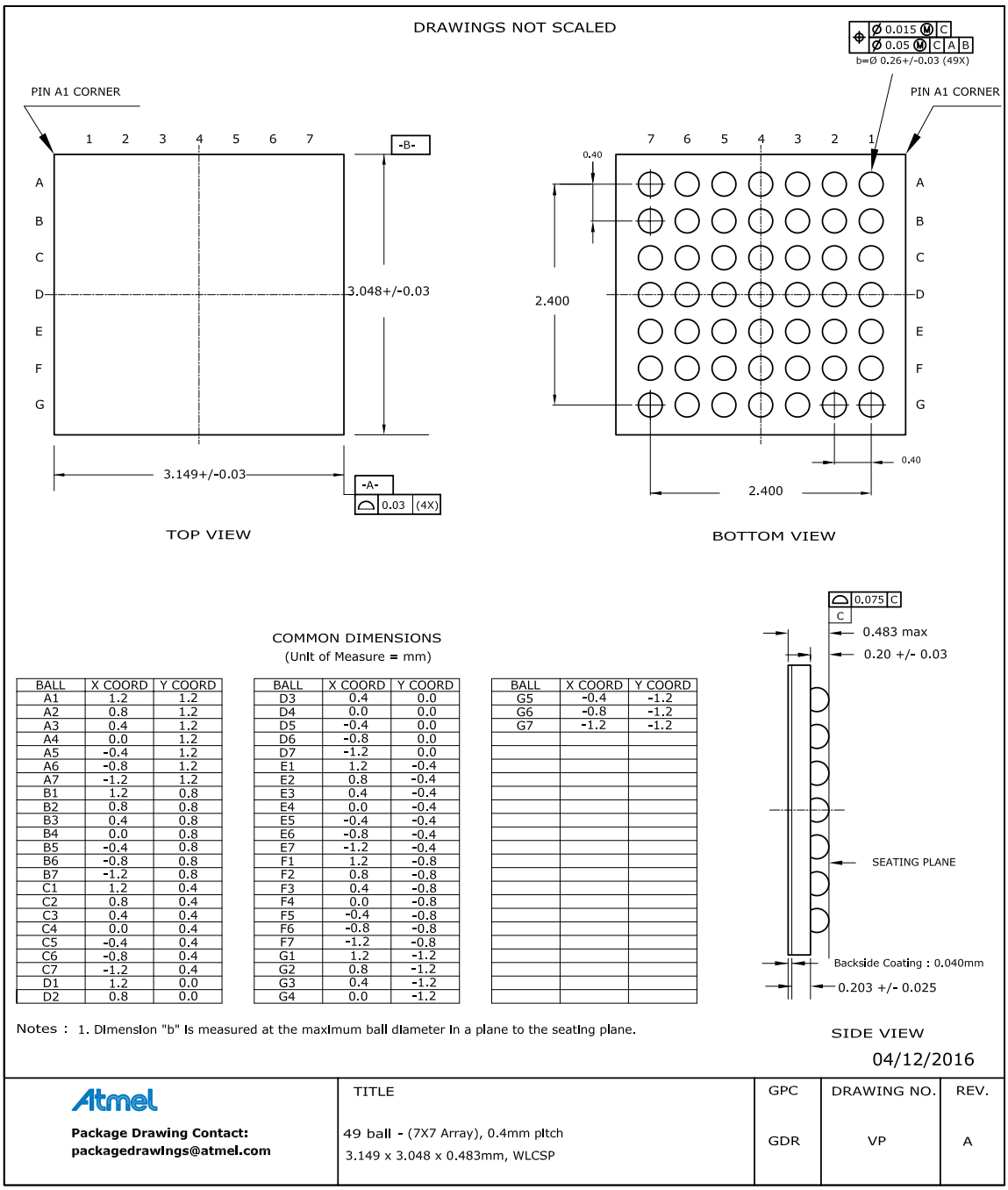
Table 12-9. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 12-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

12.2.4. 49-Ball WLCSP



BALL	X COORD	Y COORD
A1	1.2	1.2
A2	0.8	1.2
A3	0.4	1.2
A4	0.0	1.2
A5	-0.4	1.2
A6	-0.8	1.2
A7	-1.2	1.2
B1	1.2	0.8
B2	0.8	0.8
B3	0.4	0.8
B4	0.0	0.8
B5	-0.4	0.8
B6	-0.8	0.8
B7	-1.2	0.8
C1	1.2	0.4
C2	0.8	0.4
C3	0.4	0.4
C4	0.0	0.4
C5	-0.4	0.4
C6	-0.8	0.4
C7	-1.2	0.4
D1	1.2	0.0
D2	0.8	0.0

BALL	X COORD	Y COORD
D3	0.4	0.0
D4	0.0	0.0
D5	-0.4	0.0
D6	-0.8	0.0
D7	-1.2	0.0
E1	1.2	-0.4
E2	0.8	-0.4
E3	0.4	-0.4
E4	0.0	-0.4
E5	-0.4	-0.4
E6	-0.8	-0.4
E7	-1.2	-0.4
F1	1.2	-0.8
F2	0.8	-0.8
F3	0.4	-0.8
F4	0.0	-0.8
F5	-0.4	-0.8
F6	-0.8	-0.8
F7	-1.2	-0.8
G1	1.2	-1.2
G2	0.8	-1.2
G3	0.4	-1.2
G4	0.0	-1.2

BALL	X COORD	Y COORD
G5	-0.4	-1.2
G6	-0.8	-1.2
G7	-1.2	-1.2

Table 12-11. Device and Package Maximum Weight

8.45	mg

Table 12-12. Package Characteristics

Moisture Sensitivity Level	MSL1

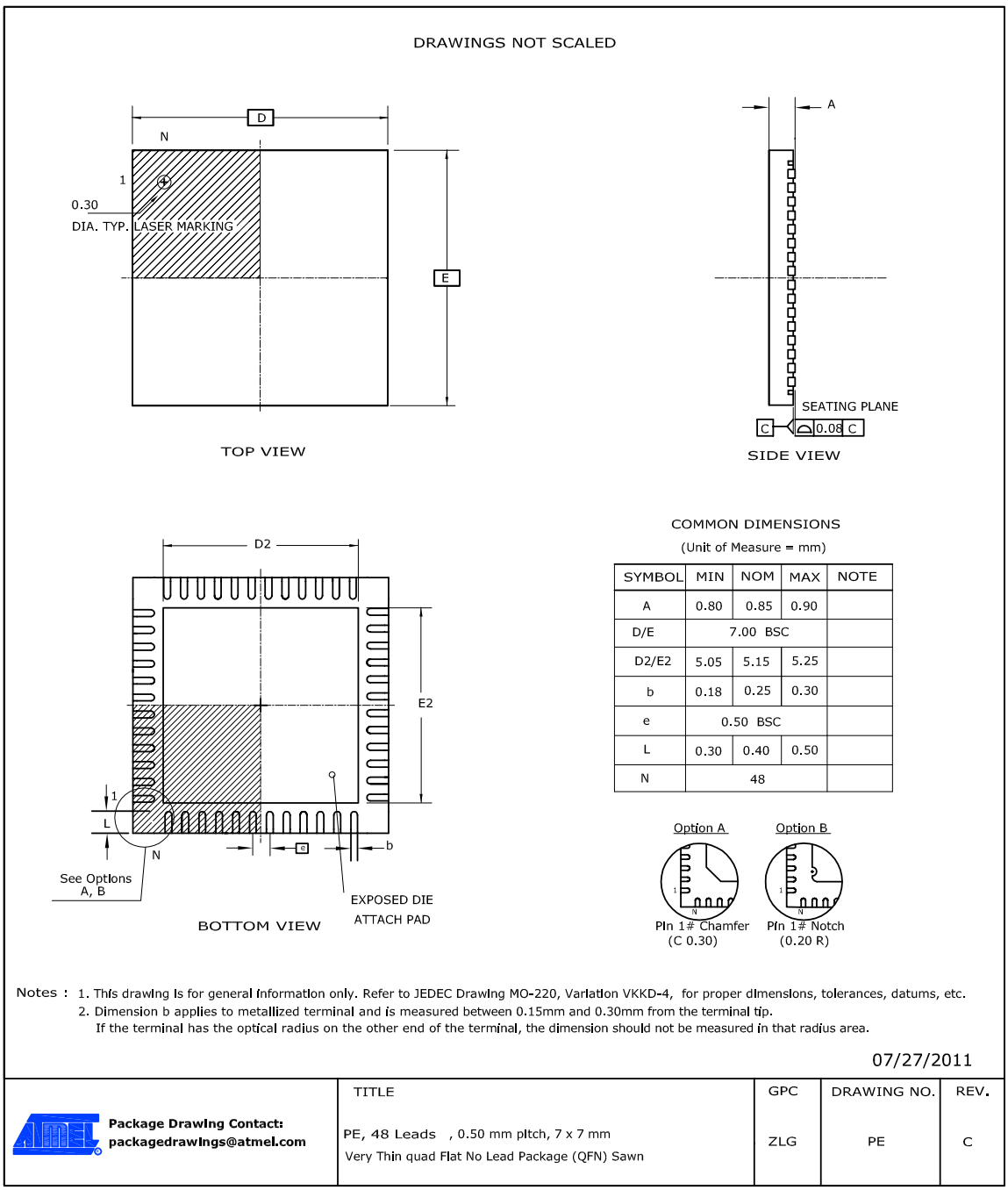
Table 12-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.6. 48 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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