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What is "Embedded - Microcontrollers"?

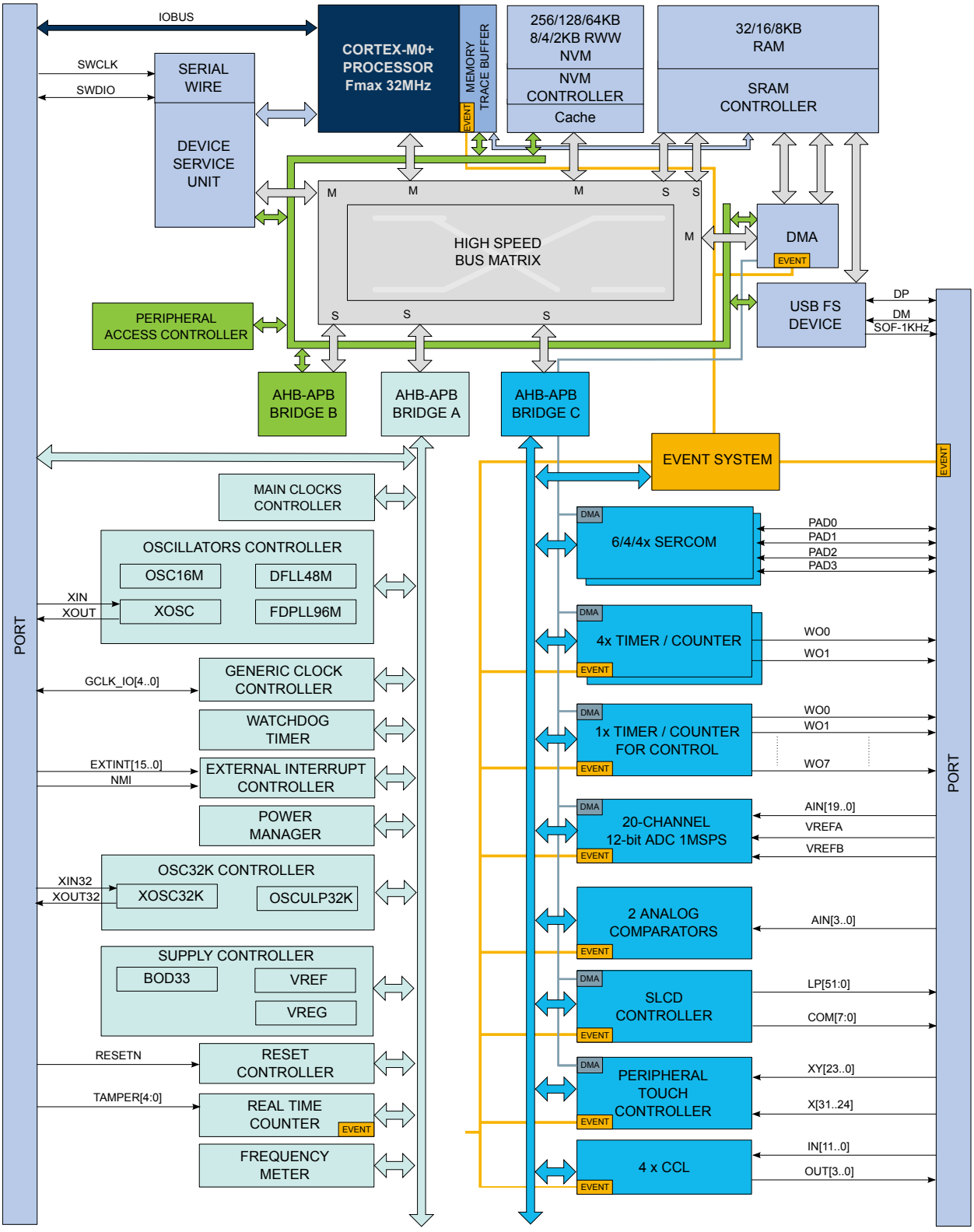
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22j18a-aut

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram



Note:

Signal Name	Function	Type	Active Level
SOF 1kHz	USB Start of Frame	Digital	
Real Timer Clock - RTC			
RTC_IN[4:0]	Tamper or external wake-up pins	Digital	
RTC_OUT	Tamper output	Digital	

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
digital: input only			30	PC08	EIC/EXTINT[0]					SLCD/ LP[15]							
			31	PC09	EIC/EXTINT[1]					SLCD/ LP[16]							
			32	PC10	EIC/EXTINT[2]					SLCD/ LP[17]	SERCOM1/ PAD[2]						
			33	PC11	EIC/EXTINT[3]					SLCD/ LP[18]	SERCOM1/ PAD[3]						
			34	PC12	EIC/EXTINT[4]					SLCD/ LP[19]	SERCOM1/ PAD[0]						
			35	PC13	EIC/EXTINT[5]					SLCD/ LP[20]	SERCOM1/ PAD[1]						
	19	23	38	VLCD													
	20	24	39	PB11	EIC/EXTINT[11]					SLCD/ LP[21]		SERCOM3/ PAD[3]	TC/1/ WO[1]	TCC/ WO[5]			CCL/ OUT[1]
I2C: full Fm+. Limited currents for Sm, Fm		25	40	PB12	EIC/EXTINT[12]					SLCD/ LP[22]	SERCOM3/ PAD[0]		TC/0/ WO[0]	TCC/ WO[6]			
		26	41	PB13	EIC/EXTINT[13]					SLCD/ LP[23]	SERCOM3/ PAD[1]		TC/0/ WO[1]	TCC/ WO[7]			
		27	42	PB14	EIC/EXTINT[14]					SLCD/ LP[24]	SERCOM3/ PAD[2]		TC/1/ WO[0]			GCLK/ IO[0]	CCL/IN[9]
		28	43	PB15	EIC/EXTINT[15]					SLCD/ LP[25]	SERCOM3/ PAD[3]		TC/1/ WO[1]			GCLK/ IO[1]	CCL/ IN[10]
			44	PC14	EIC/EXTINT[6]					SLCD/ LP[26]							
			45	PC15	EIC/EXTINT[7]					SLCD/ LP[27]							
I2C: Sm, Fm, Fm+	21	29	46	PA12	EIC/EXTINT[12]					SLCD/ LP[28]	SERCOM4/ PAD[0]	SERCOM3/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
	22	30	47	PA13	EIC/EXTINT[13]					SLCD/ LP[29]	SERCOM4/ PAD[1]	SERCOM3/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
	23	31	48	PA14	EIC/EXTINT[14]					SLCD/ LP[30]	SERCOM4/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[4]		GCLK/ IO[0]	
	24	32	49	PA15	EIC/EXTINT[15]					SLCD/ LP[31]	SERCOM4/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[5]		GCLK/ IO[1]	
	25	35	52	PA16	EIC/EXTINT[0]				PTC/ X[28]	SLCD/ LP[32]	SERCOM1/ PAD[0]	SERCOM2/ PAD[0]		TCC/ WO[6]		GCLK/ IO[2]	CCL/IN[0]
	26	36	53	PA17	EIC/EXTINT[1]				PTC/ X[29]	SLCD/ LP[33]	SERCOM1/ PAD[1]	SERCOM2/ PAD[1]		TCC/ WO[7]		GCLK/ IO[3]	CCL/IN[1]
	27	37	54	PA18	EIC/EXTINT[2]				PTC/ X[30]	SLCD/ LP[34]	SERCOM1/ PAD[2]	SERCOM2/ PAD[2]		TCC/ WO[2]		AC/ CMP[0]	CCL/IN[2]
	28	38	55	PA19	EIC/EXTINT[3]				PTC/ X[31]	SLCD/ LP[35]	SERCOM1/ PAD[3]	SERCOM2/ PAD[3]		TCC/ WO[3]		AC/ CMP[1]	CCL/ OUT[0]
			56	PC16	EIC/EXTINT[8]					SLCD/ LP[36]							
			57	PC17	EIC/EXTINT[9]					SLCD/ LP[37]							
digital: input only			58	PC18	EIC/EXTINT[10]					SLCD/ LP[38]							
			59	PC19	EIC/EXTINT[11]					SLCD/ LP[39]							
			60	PC20	EIC/EXTINT[12]					SLCD/ LP[40]							CCL/IN[9]
			61	PC21	EIC/EXTINT[13]					SLCD/ LP[41]							CCL/ IN[10]
		39	64	PB16	EIC/EXTINT[0]					SLCD/ LP[42]	SERCOM5/ PAD[0]		TC/2/ WO[0]	TCC/ WO[4]		GCLK/ IO[2]	CCL/IN[11]
		40	65	PB17	EIC/EXTINT[1]					SLCD/ LP[43]	SERCOM5/ PAD[1]		TC/2/ WO[1]	TCC/ WO[5]		GCLK/ IO[3]	CCL/ OUT[3]
			66	PB18	EIC/EXTINT[2]					SLCD/ LP[44]	SERCOM5/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[0]			
			67	PB19	EIC/EXTINT[3]					SLCD/ LP[45]	SERCOM5/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[1]			
			68	PB20	EIC/EXTINT[4]					SLCD/ LP[46]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]		TCC/ WO[2]			
			69	PB21	EIC/EXTINT[5]					SLCD/ LP[47]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]		TCC/ WO[3]			
	29	41	70	PA20	EIC/EXTINT[4]				PTC/ XY[16]	SLCD/ LP[48]	SERCOM0/ PAD[0]	SERCOM2/ PAD[2]	TC/3/ WO[0]	TCC/ WO[6]		GCLK/ IO[4]	
	30	42	71	PA21	EIC/EXTINT[5]				PTC/ XY[17]	SLCD/ LP[49]	SERCOM0/ PAD[1]	SERCOM2/ PAD[3]	TC/3/ WO[1]	TCC/ WO[7]			
I2C: Sm, Fm, Fm+	31	43	72	PA22	EIC/EXTINT[6]				PTC/ XY[18]	SLCD/ LP[50]	SERCOM0/ PAD[2]	SERCOM2/ PAD[0]	TC/0/ WO[0]	TCC/ WO[4]			CCL/IN[6]
	32	44	73	PA23	EIC/EXTINT[7]				PTC/ XY[19]	SLCD/ LP[51]	SERCOM0/ PAD[3]	SERCOM2/ PAD[1]	TC/0/ WO[1]	TCC/ WO[5]	USB/SOF_1KHZ		CCL/IN[7]
	33	45	74	PA24	EIC/EXTINT[12]						SERCOM2/ PAD[2]	SERCOM5/ PAD[0]	TC/1/ WO[0]	TCC/ WO[0]	USB/DM		CCL/IN[8]
	34	46	75	PA25	EIC/EXTINT[13]						SERCOM2/ PAD[3]	SERCOM5/ PAD[1]	TC/1/ WO[1]	TCC/ WO[1]	USB/DP		CCL/ OUT[2]
	37	49	78	PB22	EIC/EXTINT[6]						SERCOM0/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]	TCC/ WO[2]	USB/SOF_1KHZ	GCLK/ IO[0]	CCL/IN[0]

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PB22
		XOUT	PB23
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Table 7-3. XOSC32K Jitter Minimization

Package	Steady Signal Recommended
L22N	PB00, PB01, PB02, PB03, PC00, PC01
L22J	PB00, PB01, PB02, PB03, PA02, PA03
L22G	PB02, PB03, PA02, PA03

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

7.2.3. SERCOM USART and I²C Configurations

The SAM L22 has up to six instances of the serial communication interface (SERCOM) peripheral. The following table lists the supported communication protocols for each SERCOM instance.

Table 7-5. SERCOM USART and I²C Protocols

	SERCOM Instance					
Protocol	SERCOM0	SERCOM1	SERCOM2	SERCOM3	SERCOM4	SERCOM5
I²C	no	yes	yes	yes	yes	yes
I²C at 3.4MHz	no	yes	no	no	no	yes
USART including RS485 and ISO 7816	yes	yes	yes	yes	yes	yes
SPI	yes	yes	yes	yes	yes	yes

Note: Not all available I²C pins support I²C mode at 3.4MHz.

7.2.4. GPIO Pin Clusters

Table 7-6. GPIO Clusters

Package	Cluster	GPIO	Supplies Pin connected to the cluster	
100 pins	1	PA02, PA03, PB04, PB05, PC02, PC03	V_{DDANA} pin12	GNDANA pin11
	2	PA04, PA05, PA06, PA07, PB06, PB07, PB08, PB09, PC05, PC06, PC07	V_{DDANA} pin12, V_{DDANA} pin25	GNDANA pin11, GNDANA pin24
	3	PA08, PA09, PA10, PA11, PC08, PC09, PC10, PC11, PC12, PC13	V_{DDIO} pin36	GND pin37
	4	PA12, PA13, PA14, PA15, PB11, PB12, PB13, PB14, PB15, PC14, PC15	V_{DDIO} pin36, V_{DDIO} pin51	GND pin37, GND pin50
	5	PA16, PA17, PA18, PA19, PC16, PC17, PC18, PC19, PC20, PC21	V_{DDIO} pin51, V_{DDIO} pin63	GND pin50, GND pin62
	6	PA20, PA21, PA22, PA23, PA24, PA25, PB16, PB17, PB18, PB19, PB20, PB21	V_{DDIO} pin63, V_{DDIO} pin77	GND pin62, GND pin76
	7	PA27, PB22, PB23, PB24, PB25, PC24, PC25, PC26, PC27, PC28	V_{DDIO} pin77, V_{DDIO} pin92	GND pin76, GND pin90
	8	PA00, PA01, PA30, PA31, PB00, PB01, PB02, PB03, PB30, PB31, PC00, PC01	V_{DDIO} pin92	GND pin90
64 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB04, PB05, PB06, PB07, PB08, PB09	V_{DDANA} pin8	GNDANA pin7
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin21	GND pin22
	3	PA12, PA13, PA14, PA15, PB11, PB12, PB13, PB14, PB15	V_{DDIO} pin21, V_{DDIO} pin34	GND pin22, GND pin33
	4	PA16, PA17, PA18, PA19, PA20, PA21, PA22, PA23, PA24, PA25, PB16, PB17	V_{DDIO} pin34, V_{DDIO} pin48	GND pin33, GND pin47
	5	PA27, PB22, PB23	V_{DDIO} pin48, V_{DDIO} pin56	GND pin47, GND pin54
	6	PA00, PA01, PA30, PA31, PB00, PB01, PB02, PB03, PB30, PB31	V_{DDIO} pin56	GND pin54
48 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB08, PB09	V_{DDANA} pin6	GNDANA pin5
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin17	GND pin18
	3	PA12, PA13, PA14, PA15, PA16, PA17, PA18, PA19, PA20, PA21, PA22, PA23, PA24, PA25, PB11	V_{DDIO} pin17, V_{DDIO} pin36	GND pin18, GND pin35
	4	PA27, PB22, PB23	V_{DDIO} pin36, V_{DDIO} pin44	GND pin35, GND pin42
	5	PA00, PA01, PA30, PA31, PB02, PB03	V_{DDIO} pin44	GND pin42
49 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB08, PB09	V_{DDANA} pin D7	GNDANA pin C7
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin G5	GND pin F5
	3	PA12, PA13, PA14, PA15, PA16, PA17, PA18, PA19, PB11	V_{DDIO} pin G5, V_{DDIO} pin E1	GND pin F5, GND pin E2
	4	PA20, PA21, PA22, PA23, PA24, PA25	V_{DDIO} pin E1, V_{DDIO} pin A5	GND pin E2, GND pin D4
	4	PA27, PB22, PB23	V_{DDIO} pin E1, V_{DDIO} pin A5	GND pin D4, GND pin B3
	5	PA00, PA01, PA30, PA31, PB02, PB03	V_{DDIO} pin A5	GND pin B3

Figure 8-2. Power Supply Connection for Switching/Linear Mode

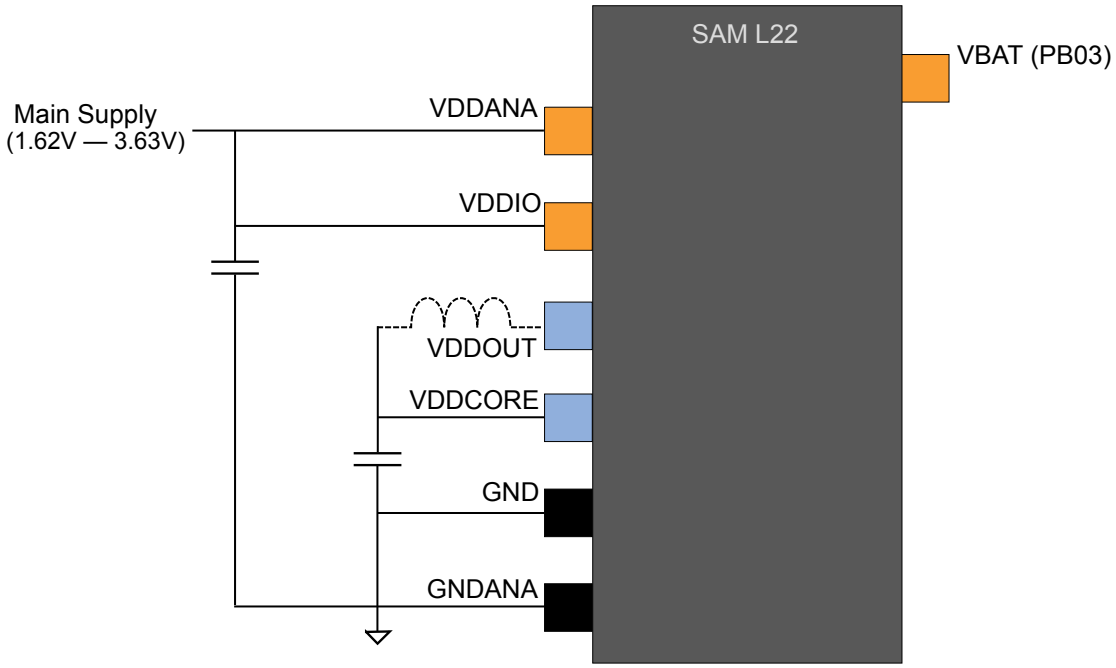
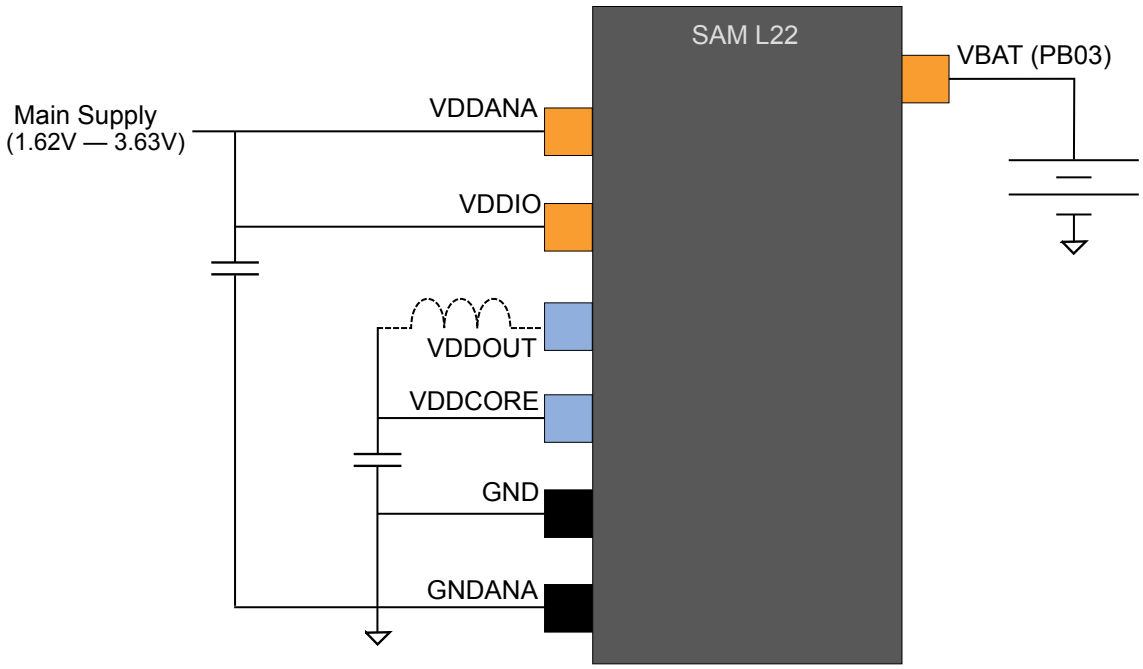


Figure 8-3. Power Supply Connection for Battery Backup



8.2.4. Power-Up Sequence

8.2.4.1. Supply Order

VDDIO and VDDANA must have the same supply sequence. Ideally, they must be connected together.

8.2.4.2. Minimum Rise Rate

One integrated power-on reset (POR) circuits monitoring VDDIO requires a minimum rise rate.

8.2.4.3. Maximum Rise Rate

The rise rate of the power supplies must not exceed the values described in Electrical Characteristics.

8.4.4. Brown-Out Detector on VDDCORE

Once the device has started up, BOD12 monitors the internal VDDCORE.

8.5. Performance Level Overview

By default, the device will start in Performance Level 0. This PL0 is aiming for the lowest power consumption by limiting logic speeds and the CPU frequency. As a consequence, all GCLK will have limited capabilities, and some peripherals and clock sources will not work or with limited capabilities:

List of peripherals/clock sources not available in PL0:

- USB (limited by logic frequency)
- DFLL48M

List of peripherals/clock sources with limited capabilities in PL0:

- All AHB/APB peripherals are limited by CPU frequency
- DPLL96M: may be able to generate 48MHz internally, but the output cannot be used by logic
- GCLK: the maximum frequency is by factor 4 compared to PL2
- SW interface: the maximum frequency is by factor 4 compared to PL2
- TC: the maximum frequency is by factor 4 compared to PL2
- TCC:the maximum frequency is by factor 4 compared to PL2
- SERCOM: the maximum frequency is by factor 4 compared to PL2

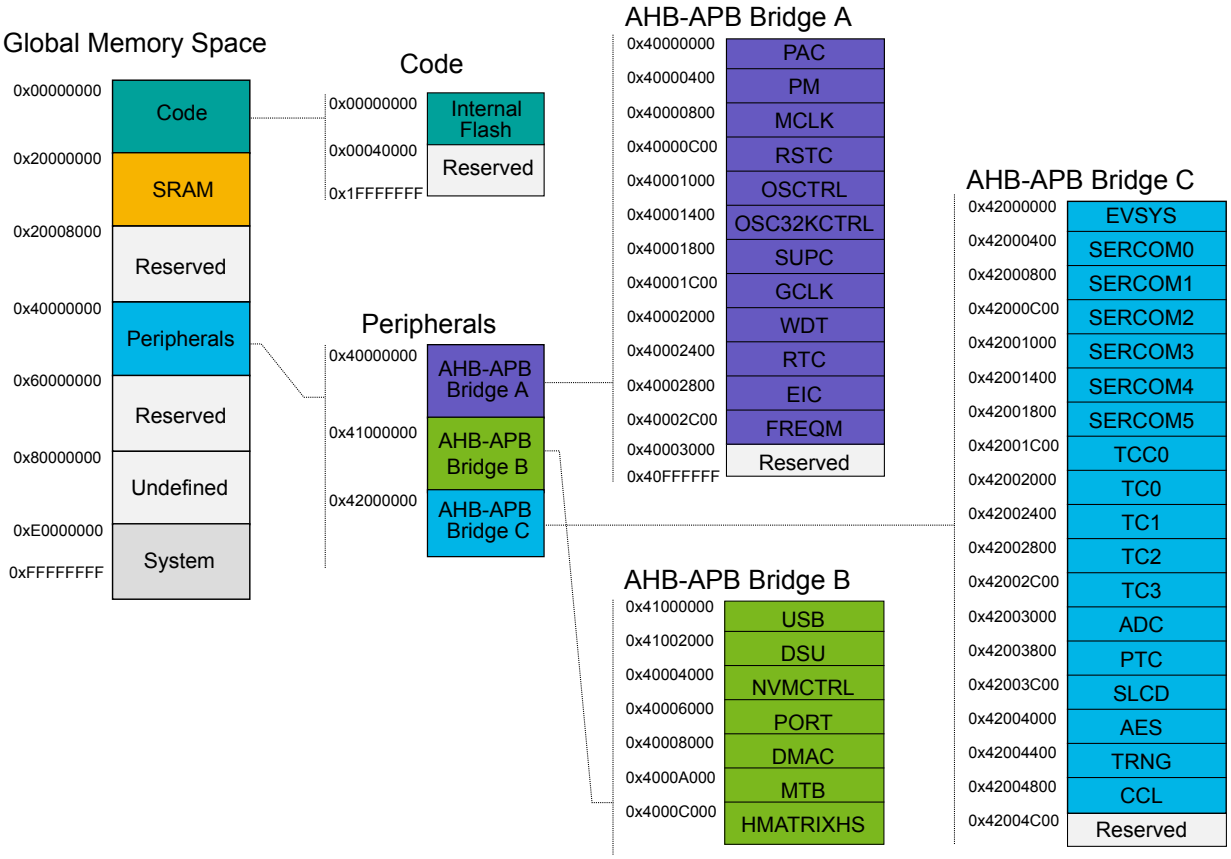
List of peripherals/clock sources with full capabilities in PL0:

- AC
- ADC
- EIC
- OSC16M
- PTC
- All 32KHz clock sources and peripherals

Full functionality and capability will be ensured in PL2. When transitioning between performance levels, the Supply Controller (SUPC) will provide a configurable smooth voltage scaling transition.

9. Product Mapping

Figure 9-1. Atmel SAM L22 Product Mapping



11. Processor and Architecture

11.1. Cortex M0+ Processor

The Atmel SAM L22 implements the ARM ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

11.1.1. Cortex M0+ Configuration

Table 11-1. Cortex M0+ Configuration

Features	Cortex-M0+ options	SAM L22 configuration
Interrupts	External interrupts 0-32	27
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

11.1.2. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

arriving interrupts. Refer to NVIC-Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).

Note: When the CPU frequency is much higher than the APB frequency it is recommended to insert a memory read barrier after each CPU write to registers mapped on the APB. Failing to do so in such conditions may lead to unexpected behavior such as e.g. re-entering a peripheral interrupt handler just after leaving it.

- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section MTB-Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (http://www.arm.com).
- Memory Protection Unit (MPU)
  - The Memory Protection Unit divides the memory map into a number of regions, and defines the location, size, access permissions and memory attributes of each region. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com)

11.1.3. Cortex M0+ Address Map

Table 11-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000	Micro Trace Buffer (MTB)

Related Links

Product Mapping on page 30

11.1.4. I/O Interface

The device allows direct access to PORT registers. Accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, so the Cortex M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O access to be sustained for as long as necessary.

11.2. Nested Vector Interrupt Controller

11.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM L22 supports 32 interrupts with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).

11.2.2. Interrupt Line Mapping

Each of the interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a '1' to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing '1' to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

Table 11-3. Interrupt Line Mapping

Peripheral source	NVIC line
EIC NMI – External Interrupt Controller	NMI
PM – Power Manager MCLK - Main Clock OSCCTRL - Oscillators Controller OSC32KCTRL - 32KHz Oscillators Controller PAC - Peripheral Access Controller SUPC - Supply Controller	0
WDT – Watchdog Timer	1
RTC – Real Time Counter	2
EIC – External Interrupt Controller	3
FREQM - Frequency Meter	4
USB - Universal Serial Bus	5
NVMCTRL – Non-Volatile Memory Controller	6
DMAC - Direct Memory Access Controller	7

branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has four programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit
- MASTER: Contains the main trace enable bit and other trace control fields
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location by a debug agent

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

11.4. High-Speed Bus System

11.4.1. Overview

11.4.2. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

11.4.3. Configuration

Figure 11-1. Master-Slave Relations High-Speed Bus Matrix

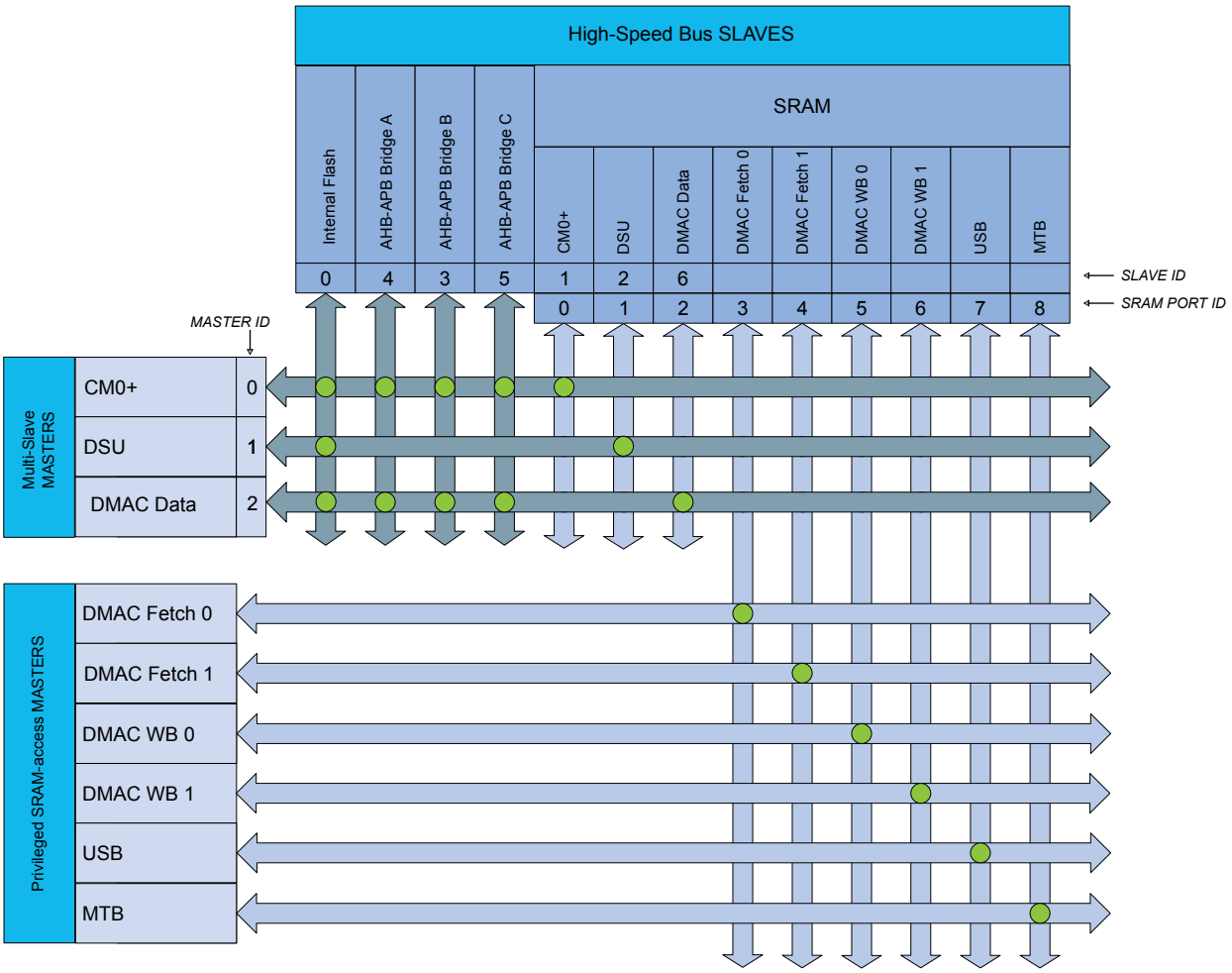


Table 11-4. High Speed Bus Matrix Masters

High-Speed Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1
DMAC - Direct Memory Access Controller / Data Access	2

Table 11-5. High-Speed Bus Matrix Slaves

High-Speed Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
SRAM Port 0 - CM0+ Access	1
SRAM Port 1 - DSU Access	2
AHB-APB Bridge B	3
AHB-APB Bridge A	4

SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
USB - Universal Serial Bus	7	Direct	IP-QOSCTRL	0x3
MTB - Micro Trace Buffer	8	Direct	STATIC-3	0x3

Note: 1. Using 32-bit access only.

12. Packaging Information

12.1. Thermal Considerations

12.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 12-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
48-pin TQFP	64.2°C/W	12.3°C/W
64-pin TQFP	60.8°C/W	12.0°C/W
100-pin TQFP	58.5°C/W	12.7°C/W
48-pin QFN	32.4°C/W	11.2°C/W
64-pin QFN	32.7°C/W	10.8°C/W
49-pin WLCSP	37.3°C/W	5.8°C/W

Related Links

Junction Temperature on page 42

12.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

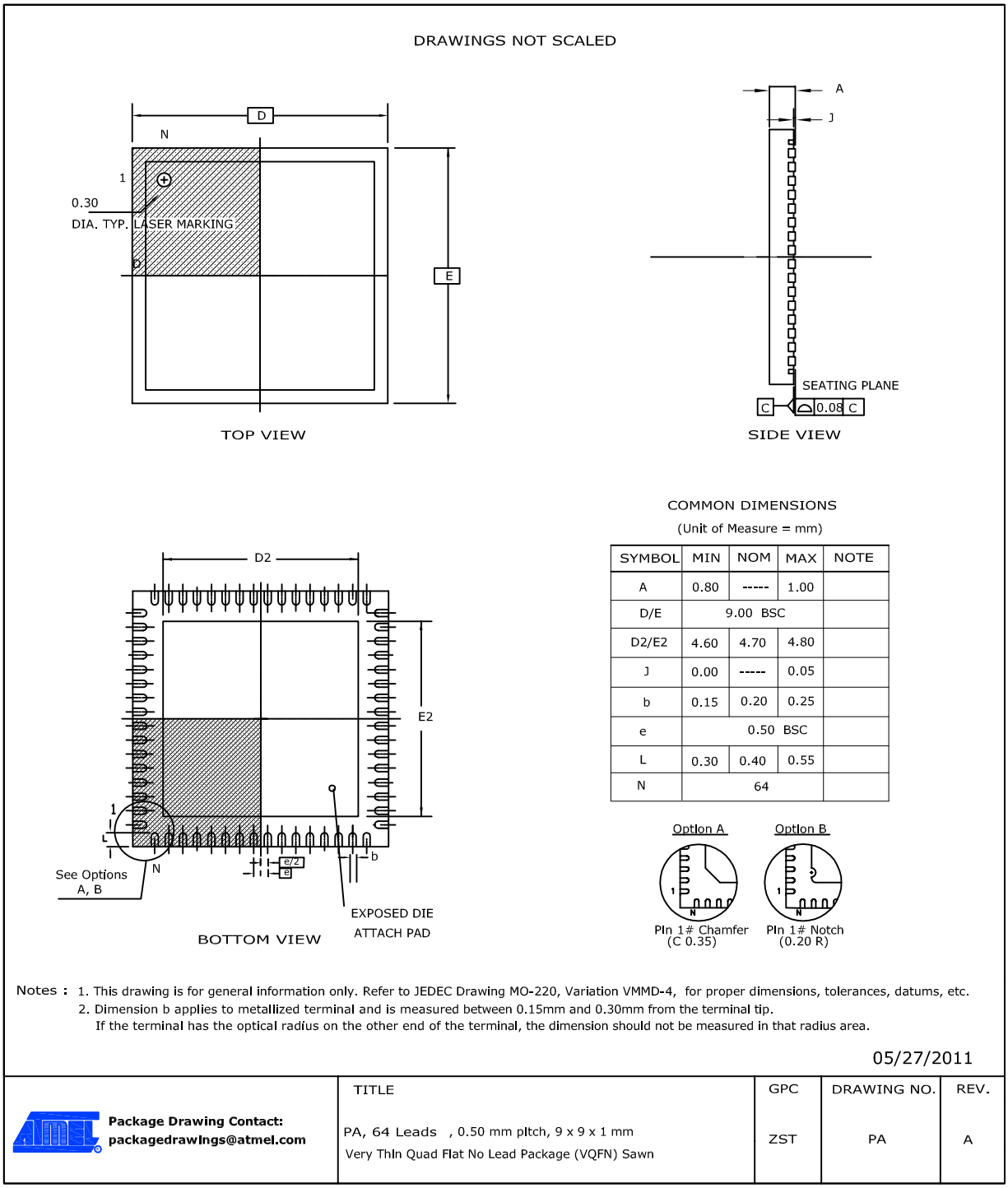
Related Links

Thermal Resistance Data on page 42

Table 12-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.3. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 12-8. Device and Package Maximum Weight

200	mg

Table 12-9. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 12-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

Table 12-13. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

12.2.5. 48 pin TQFP

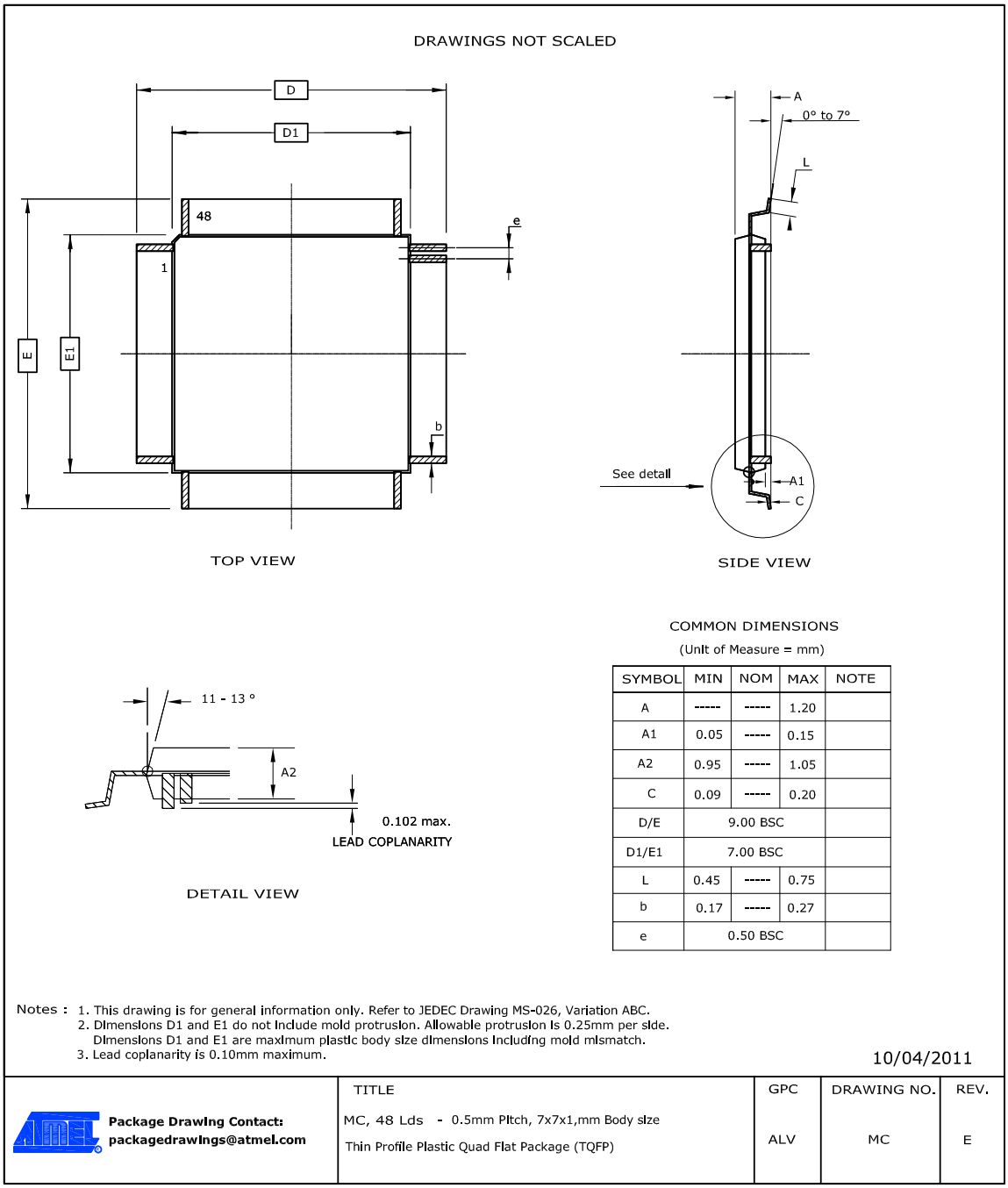


Table 12-14. Device and Package Maximum Weight

140	mg

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