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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22n16a-aut

Table of Contents

2. Configuration Summary

	SAM L22N	SAM L22J	SAM L22G
Pins	100	64	48 (QFN and TQFP) 49 (WLCSP)
General Purpose I/O-pins (GPIOs)[1]	82	50	36
Flash	256/128/64KB	256/128/64KB	256/128/64KB
Flash RWW section	8/4/2KB	8/4/2KB	8/4/2KB
System SRAM	32/16/8KB	32/16/8KB	32/16/8KB
Segment LCD (SLCD) Pins[1]	48 selectable from 52	31	23
Timer Counter (TC) instances	4	4	4
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	1	1	1
Waveform output channels per TCC	4	4	4
DMA channels	16	16	16
USB interface	1	1	1
AES engine	1	1	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
True Random Generator (TRNG)	1	1	1
Serial Communication Interface (SERCOM) instances	6	4[2]	4[2]
Analog-to-Digital Converter (ADC) channels	20	16	10
Two Analog Comparators (AC) with number of external input channels	4	4	2
Tamper Input Pins	5	3	2

	SAM L22N	SAM L22J	SAM L22G
Wake-up Pins with debouncing	5	3	2
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) channels (X- x Y-lines) for mutual capacitance[3]	256 (16x16)	182 (13x14)	132 (11x12)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-lines only)[4]	24	19	15
Maximum CPU frequency	32MHz	32MHz	32MHz
Packages	TQFP	QFN TQFP	QFN TQFP WLCSP
Oscillators			
Event System channels	8	8	8
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Note:

1. L22J, L22G: All SLCD Pins can be configured also as GPIOs. L22N: 44 SLCD Pins can be configured as GPIOs, 8 SLCD Pins can be used as GP input.
2. SAM L22N: SERCOM[5:0]. L22G, L22J: SERCOM[3:0].
3. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines.
4. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML22J18A-MUT			QFN64	

3.3. SAM L22G

Table 3-3. SAM L22G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML22G16A-MUT			QFN48	
ATSAML22G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML22G17A-MUT			QFN48	
ATSAML22G17A-UUT			WLCSP49	
ATSAML22G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML22G18A-MUT			QFN48	
ATSAML22G18A-UUT			WLCSP49	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

Table 3-4. SAM L22 Device Identification Values

DSU DID.DEVSEL	Device
0x0	L22N18
0x1	L22N17
0x2	L22N16
0x3-0x4	Reserved
0x5	L22J18
0x6	L22J17
0x7	L22J16
0x8-0x9	Reserved
0xA	L22G18
0xB	L22G17
0xC	L22G16
0xD-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

1. Some device configurations have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. The number of PTC X and Y signals is configurable.

5. Pinout

5.1. SAM L22G

Figure 5-1. 48-Pin QFN, TQFP

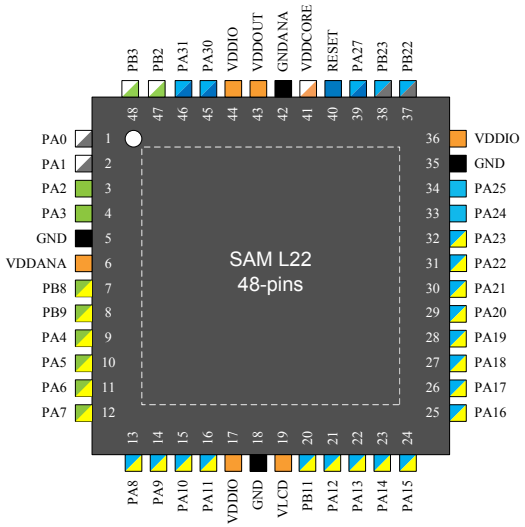
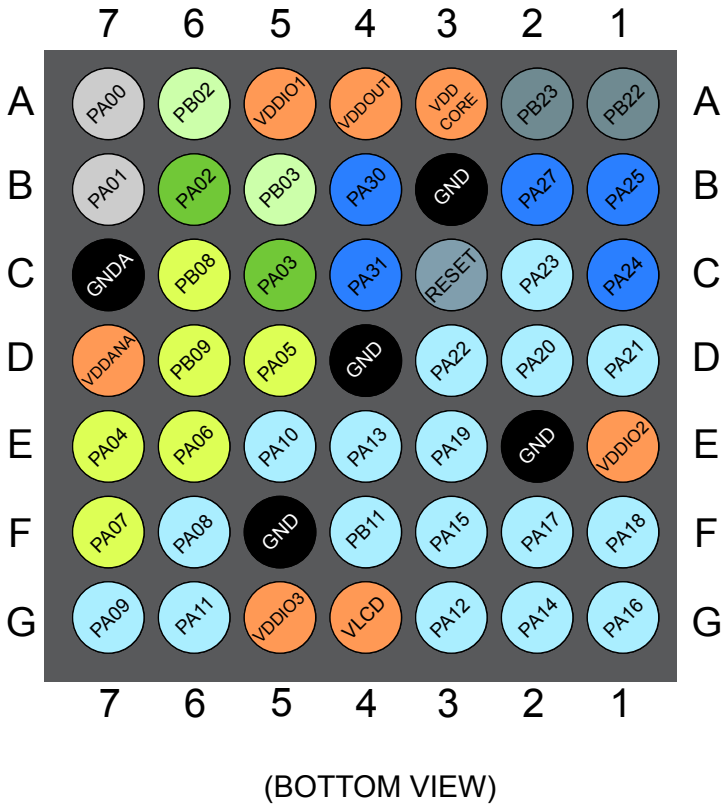


Figure 5-2. 49-Pin WLCSP



(BOTTOM VIEW)

6. Signal Descriptions List

The following table gives details on signal names classified by peripheral.

Table 6-1. Signal Descriptions List

Signal Name	Function	Type	Active Level
Analog Comparators - AC			
AIN[3:0]	AC Analog Inputs	Analog	
CMP[1:0]	AC Analog Output	Analog	
Analog Digital Converter - ADC			
AIN[19:0]	ADC Analog Inputs	Analog	
VREFA	ADC Voltage External Reference A	Analog	
VREFB	ADC Voltage External Reference B	Analog	
External Interrupt Controller - EIC			
EXTINT[15:0]	External Interrupts inputs	Digital	
NMI	External Non-Maskable Interrupt input	Digital	
Generic Clock Generator - GCLK			
GCLK_IO[4:0]	Generic Clock (source clock inputs or generic clock generator output)	Digital	
Custom Control Logic - CCL			
IN[11:0]	Logic Inputs	Digital	
OUT[3:0]	Logic Outputs	Digital	
Supply Controller - SUPC			
VBAT	External battery supply Inputs	Analog	
PSOK	Main Power Supply OK input	Digital	
OUT[1:0]	Logic Outputs	Digital	
Power Manager - PM			
RESETN	Reset input	Digital	Low
Serial Communication Interface - SERCOMx			
PAD[3:0]	SERCOM Inputs/Outputs Pads	Digital	
Oscillators Control - OSCCTRL			
XIN	Crystal or external clock Input	Analog/Digital	
XOUT	Crystal Output	Analog	

Signal Name	Function	Type	Active Level
32KHz Oscillators Control - OSC32KCTRL			
XIN32	32KHz Crystal or external clock Input	Analog/Digital	
XOUT32	32KHz Crystal Output	Analog	
Timer Counter - TCx			
WO[1:0]	Waveform Outputs	Digital	
Timer Counter - TCCx			
WO[7:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[7:0]	PTC Input/Output	Analog	
Y[23:0]	PTC Input/Output	Analog	
X[31:24]	PTC Output	Analog	
General Purpose I/O - PORT			
PA25 - PA00	Parallel I/O Controller I/O Port A	Digital	
PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB09 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB25 - PB11	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	
PC03 - PC00	Parallel I/O Controller I/O Port C	Digital	
PC07 - PC05	Parallel I/O Controller I/O Port C	Digital	
PC17 - PC12	Parallel I/O Controller I/O Port C	Digital	
PC28 - PC24	Parallel I/O Controller I/O Port C	Digital	
General Purpose input - PORT			
PC11 - PC08	Parallel I/O Controller input Port C	Digital	
PC21 - PC18	Parallel I/O Controller input Port C	Digital	
Segment LCD			
SLCD51 - SLCD00	Segment LCD	Analog	
VLCD	Bias Voltage	Analog	
Universal Serial Bus - USB			
DP	DP for USB	Digital	
DM	DM for USB	Digital	

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
digital: input only			30	PC08	EIC/EXTINT[0]					SLCD/ LP[15]							
			31	PC09	EIC/EXTINT[1]					SLCD/ LP[16]							
			32	PC10	EIC/EXTINT[2]					SLCD/ LP[17]	SERCOM1/ PAD[2]						
			33	PC11	EIC/EXTINT[3]					SLCD/ LP[18]	SERCOM1/ PAD[3]						
			34	PC12	EIC/EXTINT[4]					SLCD/ LP[19]	SERCOM1/ PAD[0]						
			35	PC13	EIC/EXTINT[5]					SLCD/ LP[20]	SERCOM1/ PAD[1]						
	19	23	38	VLCD													
	20	24	39	PB11	EIC/EXTINT[11]					SLCD/ LP[21]		SERCOM3/ PAD[3]	TC/1/ WO[1]	TCC/ WO[5]			CCL/ OUT[1]
I2C: full Fm+. Limited currents for Sm, Fm		25	40	PB12	EIC/EXTINT[12]					SLCD/ LP[22]	SERCOM3/ PAD[0]		TC/0/ WO[0]	TCC/ WO[6]			
		26	41	PB13	EIC/EXTINT[13]					SLCD/ LP[23]	SERCOM3/ PAD[1]		TC/0/ WO[1]	TCC/ WO[7]			
		27	42	PB14	EIC/EXTINT[14]					SLCD/ LP[24]	SERCOM3/ PAD[2]		TC/1/ WO[0]			GCLK/ IO[0]	CCL/IN[9]
		28	43	PB15	EIC/EXTINT[15]					SLCD/ LP[25]	SERCOM3/ PAD[3]		TC/1/ WO[1]			GCLK/ IO[1]	CCL/ IN[10]
			44	PC14	EIC/EXTINT[6]					SLCD/ LP[26]							
			45	PC15	EIC/EXTINT[7]					SLCD/ LP[27]							
I2C: Sm, Fm, Fm+	21	29	46	PA12	EIC/EXTINT[12]					SLCD/ LP[28]	SERCOM4/ PAD[0]	SERCOM3/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
	22	30	47	PA13	EIC/EXTINT[13]					SLCD/ LP[29]	SERCOM4/ PAD[1]	SERCOM3/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
	23	31	48	PA14	EIC/EXTINT[14]					SLCD/ LP[30]	SERCOM4/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[4]		GCLK/ IO[0]	
	24	32	49	PA15	EIC/EXTINT[15]					SLCD/ LP[31]	SERCOM4/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[5]		GCLK/ IO[1]	
	25	35	52	PA16	EIC/EXTINT[0]				PTC/ X[28]	SLCD/ LP[32]	SERCOM1/ PAD[0]	SERCOM2/ PAD[0]		TCC/ WO[6]		GCLK/ IO[2]	CCL/IN[0]
	26	36	53	PA17	EIC/EXTINT[1]				PTC/ X[29]	SLCD/ LP[33]	SERCOM1/ PAD[1]	SERCOM2/ PAD[1]		TCC/ WO[7]		GCLK/ IO[3]	CCL/IN[1]
	27	37	54	PA18	EIC/EXTINT[2]				PTC/ X[30]	SLCD/ LP[34]	SERCOM1/ PAD[2]	SERCOM2/ PAD[2]		TCC/ WO[2]		AC/ CMP[0]	CCL/IN[2]
	28	38	55	PA19	EIC/EXTINT[3]				PTC/ X[31]	SLCD/ LP[35]	SERCOM1/ PAD[3]	SERCOM2/ PAD[3]		TCC/ WO[3]		AC/ CMP[1]	CCL/ OUT[0]
			56	PC16	EIC/EXTINT[8]					SLCD/ LP[36]							
			57	PC17	EIC/EXTINT[9]					SLCD/ LP[37]							
digital: input only			58	PC18	EIC/EXTINT[10]					SLCD/ LP[38]							
			59	PC19	EIC/EXTINT[11]					SLCD/ LP[39]							
			60	PC20	EIC/EXTINT[12]					SLCD/ LP[40]							CCL/IN[9]
			61	PC21	EIC/EXTINT[13]					SLCD/ LP[41]							CCL/ IN[10]
		39	64	PB16	EIC/EXTINT[0]					SLCD/ LP[42]	SERCOM5/ PAD[0]		TC/2/ WO[0]	TCC/ WO[4]		GCLK/ IO[2]	CCL/IN[11]
		40	65	PB17	EIC/EXTINT[1]					SLCD/ LP[43]	SERCOM5/ PAD[1]		TC/2/ WO[1]	TCC/ WO[5]		GCLK/ IO[3]	CCL/ OUT[3]
			66	PB18	EIC/EXTINT[2]					SLCD/ LP[44]	SERCOM5/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[0]			
			67	PB19	EIC/EXTINT[3]					SLCD/ LP[45]	SERCOM5/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[1]			
			68	PB20	EIC/EXTINT[4]					SLCD/ LP[46]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]		TCC/ WO[2]			
			69	PB21	EIC/EXTINT[5]					SLCD/ LP[47]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]		TCC/ WO[3]			
	29	41	70	PA20	EIC/EXTINT[4]				PTC/ XY[16]	SLCD/ LP[48]	SERCOM0/ PAD[0]	SERCOM2/ PAD[2]	TC/3/ WO[0]	TCC/ WO[6]		GCLK/ IO[4]	
	30	42	71	PA21	EIC/EXTINT[5]				PTC/ XY[17]	SLCD/ LP[49]	SERCOM0/ PAD[1]	SERCOM2/ PAD[3]	TC/3/ WO[1]	TCC/ WO[7]			
I2C: Sm, Fm, Fm+	31	43	72	PA22	EIC/EXTINT[6]				PTC/ XY[18]	SLCD/ LP[50]	SERCOM0/ PAD[2]	SERCOM2/ PAD[0]	TC/0/ WO[0]	TCC/ WO[4]			CCL/IN[6]
	32	44	73	PA23	EIC/EXTINT[7]				PTC/ XY[19]	SLCD/ LP[51]	SERCOM0/ PAD[3]	SERCOM2/ PAD[1]	TC/0/ WO[1]	TCC/ WO[5]	USB/SOF_1KHZ		CCL/IN[7]
	33	45	74	PA24	EIC/EXTINT[12]						SERCOM2/ PAD[2]	SERCOM5/ PAD[0]	TC/1/ WO[0]	TCC/ WO[0]	USB/DM		CCL/IN[8]
	34	46	75	PA25	EIC/EXTINT[13]						SERCOM2/ PAD[3]	SERCOM5/ PAD[1]	TC/1/ WO[1]	TCC/ WO[1]	USB/DP		CCL/ OUT[2]
	37	49	78	PB22	EIC/EXTINT[6]						SERCOM0/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]	TCC/ WO[2]	USB/SOF_1KHZ	GCLK/ IO[0]	CCL/IN[0]

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PB22
		XOUT	PB23
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Table 7-3. XOSC32K Jitter Minimization

Package	Steady Signal Recommended
L22N	PB00, PB01, PB02, PB03, PC00, PC01
L22J	PB00, PB01, PB02, PB03, PA02, PA03
L22G	PB02, PB03, PA02, PA03

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

7.2.3. SERCOM USART and I²C Configurations

The SAM L22 has up to six instances of the serial communication interface (SERCOM) peripheral. The following table lists the supported communication protocols for each SERCOM instance.

Table 7-5. SERCOM USART and I²C Protocols

	SERCOM Instance					
Protocol	SERCOM0	SERCOM1	SERCOM2	SERCOM3	SERCOM4	SERCOM5
I²C	no	yes	yes	yes	yes	yes
I²C at 3.4MHz	no	yes	no	no	no	yes
USART including RS485 and ISO 7816	yes	yes	yes	yes	yes	yes
SPI	yes	yes	yes	yes	yes	yes

Note: Not all available I²C pins support I²C mode at 3.4MHz.

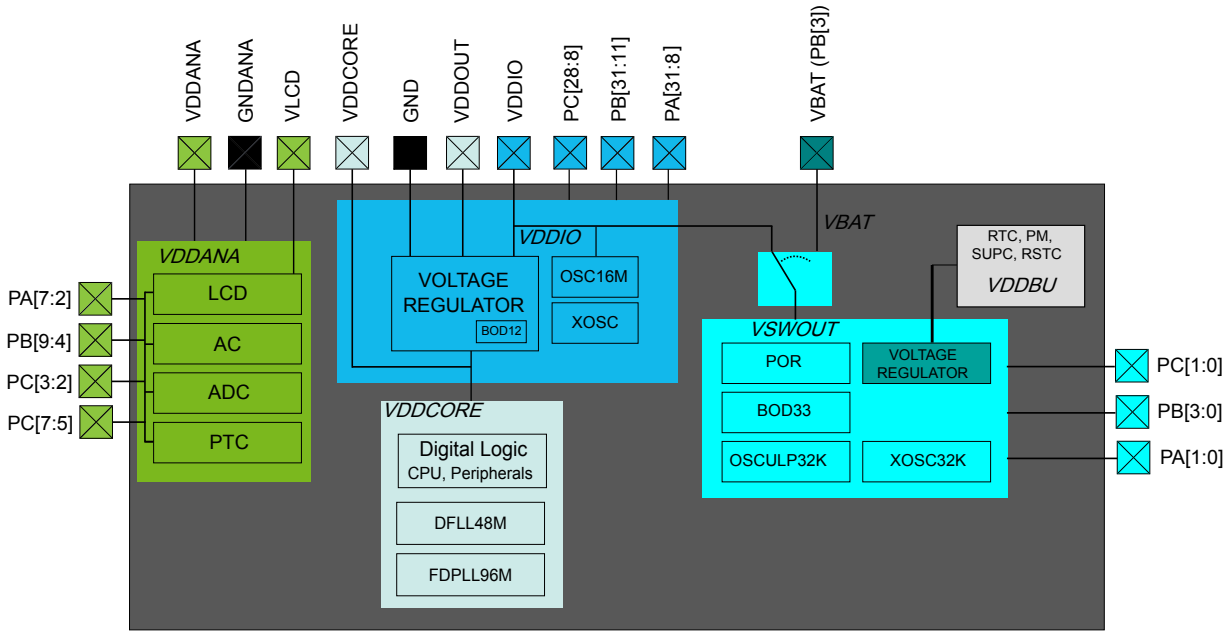
7.2.4. GPIO Pin Clusters

Table 7-6. GPIO Clusters

Package	Cluster	GPIO	Supplies Pin connected to the cluster	
100 pins	1	PA02, PA03, PB04, PB05, PC02, PC03	V_{DDANA} pin12	GNDANA pin11
	2	PA04, PA05, PA06, PA07, PB06, PB07, PB08, PB09, PC05, PC06, PC07	V_{DDANA} pin12, V_{DDANA} pin25	GNDANA pin11, GNDANA pin24
	3	PA08, PA09, PA10, PA11, PC08, PC09, PC10, PC11, PC12, PC13	V_{DDIO} pin36	GND pin37
	4	PA12, PA13, PA14, PA15, PB11, PB12, PB13, PB14, PB15, PC14, PC15	V_{DDIO} pin36, V_{DDIO} pin51	GND pin37, GND pin50
	5	PA16, PA17, PA18, PA19, PC16, PC17, PC18, PC19, PC20, PC21	V_{DDIO} pin51, V_{DDIO} pin63	GND pin50, GND pin62
	6	PA20, PA21, PA22, PA23, PA24, PA25, PB16, PB17, PB18, PB19, PB20, PB21	V_{DDIO} pin63, V_{DDIO} pin77	GND pin62, GND pin76
	7	PA27, PB22, PB23, PB24, PB25, PC24, PC25, PC26, PC27, PC28	V_{DDIO} pin77, V_{DDIO} pin92	GND pin76, GND pin90
	8	PA00, PA01, PA30, PA31, PB00, PB01, PB02, PB03, PB30, PB31, PC00, PC01	V_{DDIO} pin92	GND pin90
64 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB04, PB05, PB06, PB07, PB08, PB09	V_{DDANA} pin8	GNDANA pin7
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin21	GND pin22
	3	PA12, PA13, PA14, PA15, PB11, PB12, PB13, PB14, PB15	V_{DDIO} pin21, V_{DDIO} pin34	GND pin22, GND pin33
	4	PA16, PA17, PA18, PA19, PA20, PA21, PA22, PA23, PA24, PA25, PB16, PB17	V_{DDIO} pin34, V_{DDIO} pin48	GND pin33, GND pin47
	5	PA27, PB22, PB23	V_{DDIO} pin48, V_{DDIO} pin56	GND pin47, GND pin54
	6	PA00, PA01, PA30, PA31, PB00, PB01, PB02, PB03, PB30, PB31	V_{DDIO} pin56	GND pin54
48 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB08, PB09	V_{DDANA} pin6	GNDANA pin5
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin17	GND pin18
	3	PA12, PA13, PA14, PA15, PA16, PA17, PA18, PA19, PA20, PA21, PA22, PA23, PA24, PA25, PB11	V_{DDIO} pin17, V_{DDIO} pin36	GND pin18, GND pin35
	4	PA27, PB22, PB23	V_{DDIO} pin36, V_{DDIO} pin44	GND pin35, GND pin42
	5	PA00, PA01, PA30, PA31, PB02, PB03	V_{DDIO} pin44	GND pin42
49 pins	1	PA02, PA03, PA04, PA05, PA06, PA07, PB08, PB09	V_{DDANA} pin D7	GNDANA pin C7
	2	PA08, PA09, PA10, PA11	V_{DDIO} pin G5	GND pin F5
	3	PA12, PA13, PA14, PA15, PA16, PA17, PA18, PA19, PB11	V_{DDIO} pin G5, V_{DDIO} pin E1	GND pin F5, GND pin E2
	4	PA20, PA21, PA22, PA23, PA24, PA25	V_{DDIO} pin E1, V_{DDIO} pin A5	GND pin E2, GND pin D4
	4	PA27, PB22, PB23	V_{DDIO} pin E1, V_{DDIO} pin A5	GND pin D4, GND pin B3
	5	PA00, PA01, PA30, PA31, PB02, PB03	V_{DDIO} pin A5	GND pin B3

8. Power Supply and Start-Up Considerations

8.1. Power Domain Overview



The Atmel SAM L22 power domains are not independent of each other:

- VDDCORE and VDDIO share GND, whereas VDDANA refers to GNDANA.
- VDDCORE serves as the internal voltage regulator output.
- VSWOUT and VDDBU are internal power domains.

8.2. Power Supply Considerations

8.2.1. Power Supplies

The Atmel SAM L22 has several different power supply pins:

- VDDIO powers I/O lines and OSC16M, XOSC, the internal regulator for VDDCORE and the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDANA powers I/O lines and the ADC, AC, LCD, and PTC. Voltage is 1.62V to 3.63V
- VLCD has two alternative functions:
  - Output of the LCD voltage pump when VLCD is generated internally. Output voltage is 2.5V to 3.5V.
  - Supply input for the bias generator when VLCD is provided externally by the application. Input voltage is 2.4 to 3.6V.
- VBAT powers the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDCORE serves as the internal voltage regulator output. It powers the core, memories, peripherals, DFLL48M and FDPLL96M. Voltage is 0.9V to 1.2V typical.
- The Automatic Power Switch is a configurable switch that selects between VDDIO and VBAT as supply for the internal output VSWOUT, see the figure in Power Domain Overview.

Figure 8-2. Power Supply Connection for Switching/Linear Mode

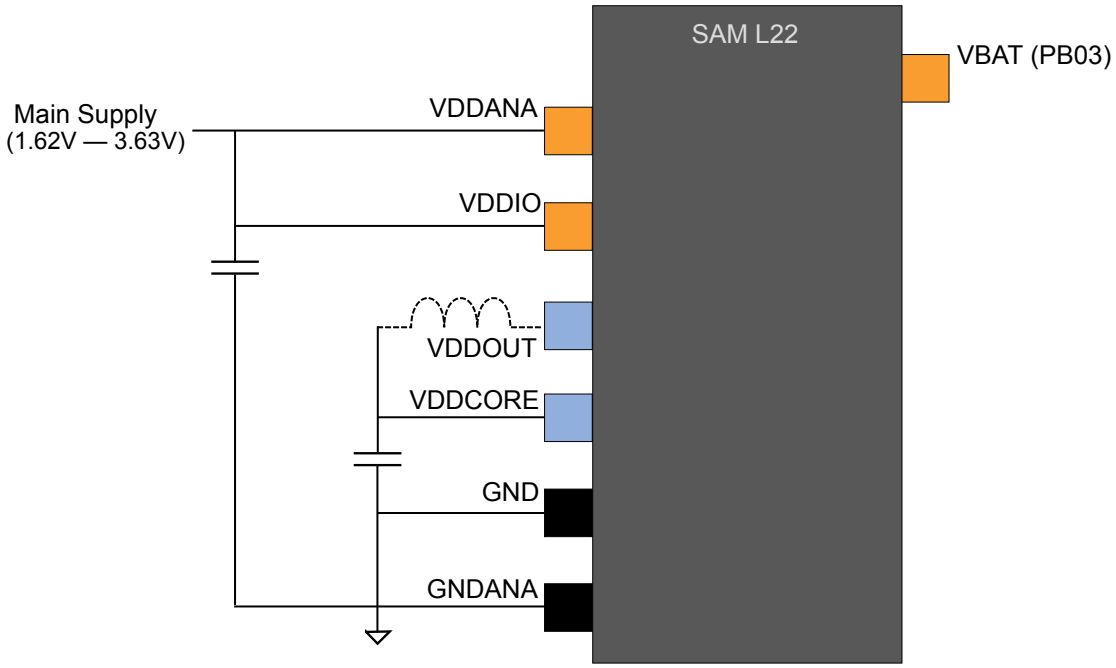
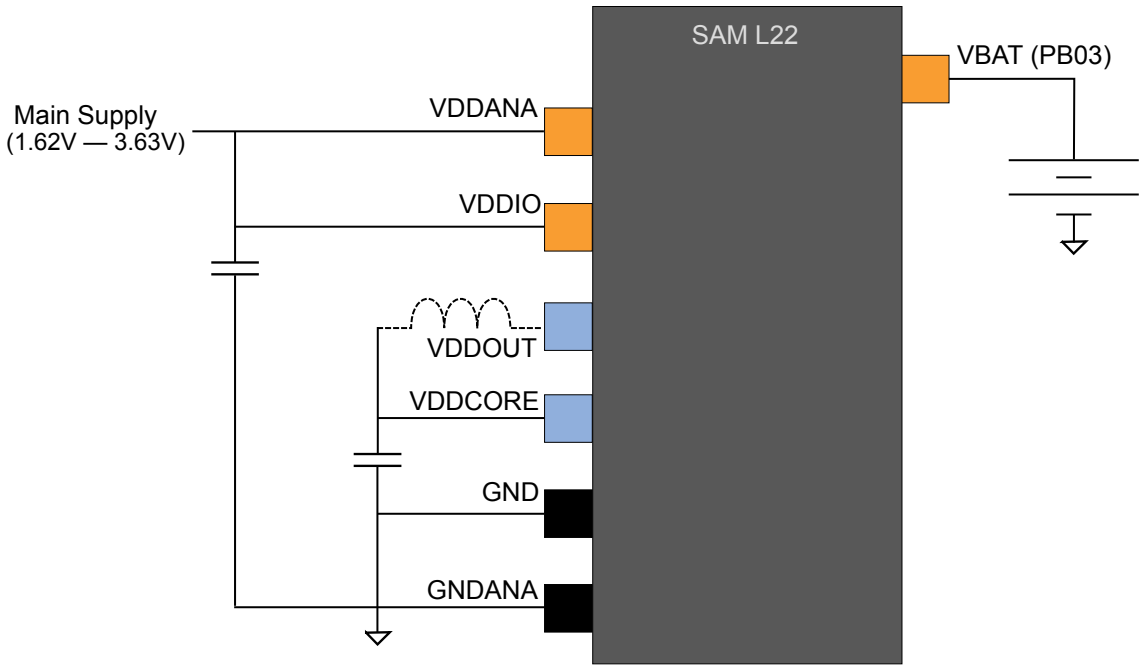


Figure 8-3. Power Supply Connection for Battery Backup



8.2.4. Power-Up Sequence

8.2.4.1. Supply Order

VDDIO and VDDANA must have the same supply sequence. Ideally, they must be connected together.

8.2.4.2. Minimum Rise Rate

One integrated power-on reset (POR) circuits monitoring VDDIO requires a minimum rise rate.

8.2.4.3. Maximum Rise Rate

The rise rate of the power supplies must not exceed the values described in Electrical Characteristics.

8.3. Power-Up

This section summarizes the power-up sequence of the SAM L22. The behavior after power-up is controlled by the Power Manager.

8.3.1. Starting of Internal Regulator

After power-up, the device is set to its initial state and kept in Reset, until the power has stabilized throughout the device. The default performance level after power-up is PL0.

The internal regulator provides the internal VDDCORE corresponding to this performance level. Once the external voltage VDDIO and the internal VDDCORE reach a stable value, the internal Reset is released.

8.3.2. Starting of Clocks

Once the power has stabilized and the internal Reset is released, the device will use a 4MHz clock by default. The clock source for this clock signal is OSC16M, which is enabled and configured at 4MHz after a reset by default. This is also the default time base for Generic Clock Generator 0. In turn, Generator 0 provides the main clock GCLK_MAIN which is used by the Power Manager (PM).

Some synchronous system clocks are active after Start-Up, allowing software execution. Refer to the “Clock Mask Register” section in the PM-Power Manager documentation for the list of clocks that are running by default. Synchronous system clocks that are running receive the 4MHz clock from Generic Clock Generator 0. Other generic clocks are disabled.

8.3.3. I/O Pins

After power-up, the I/O pins are tri-stated except PA30, which is pull-up enabled and configured as input.

8.3.4. Fetching of Initial Instructions

After Reset has been released, the CPU starts fetching PC and SP values from the Reset address, 0x00000000. This points to the first executable address in the internal Flash memory. The code read from the internal Flash can be used to configure the clock system and clock sources. See the related peripheral documentation for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

8.4. Power-On Reset and Brown-Out Detector

The SAM L22 embeds three features to monitor, warn and/or reset the device:

- POR: Power-on Reset on VSWOUT and VDDIO
- BOD33: Brown-out detector on VSWOUT/VBAT
- Brown-out detector internal to the voltage regulator for VDDCORE. BOD12 is calibrated in production and its calibration parameters are stored in the NVM User Row. This data should not be changed if the User Row is written to in order to assure correct behavior.

8.4.1. Power-On Reset on VSWOUT

VSWOUT is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VSWOUT goes below the threshold voltage, the entire chip is reset.

8.4.2. Power-On Reset on VDDIO

VDDIO is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VDDIO goes below the threshold voltage, all I/Os supplied by VDDIO are reset.

8.4.3. Brown-Out Detector on VSWOUT/VBAT

BOD33 monitors VSWOUT or VBAT depending on configuration.

11. Processor and Architecture

11.1. Cortex M0+ Processor

The Atmel SAM L22 implements the ARM ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

11.1.1. Cortex M0+ Configuration

Table 11-1. Cortex M0+ Configuration

Features	Cortex-M0+ options	SAM L22 configuration
Interrupts	External interrupts 0-32	27
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

11.1.2. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

Peripheral source	NVIC line
EVSYS – Event System	8
SERCOM0 – Serial Communication Interface 0	9
SERCOM1 – Serial Communication Interface 1	10
SERCOM2 – Serial Communication Interface 2	11
SERCOM3 – Serial Communication Interface 3	12
SERCOM4 – Serial Communication Interface 4	13
SERCOM5 – Serial Communication Interface 5	14
TCC0 – Timer Counter for Control 0	15
TC0 – Timer Counter 0	16
TC1 – Timer Counter 1	17
TC2 – Timer Counter 2	18
TC3 – Timer Counter 3	19
ADC – Analog-to-Digital Converter	20
AC – Analog Comparator	21
PTC – Peripheral Touch Controller	22
SLCD - Segmented LCD Controller	23
AES - Advanced Encryption Standard module	24
TRNG - True Random Number Generator	25

11.3. Micro Trace Buffer

11.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

11.3.2. Overview

When enabled, the MTB records the changes in program flow that are reported by the Cortex-M0+ processor over the execution trace interface. This interface is shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. The information is stored by the MTB in the SRAM as trace packets. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB stores trace information into the SRAM and gives the processor access to the SRAM simultaneously. The MTB ensures that trace write accesses have priority over processor accesses.

An execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects a non-sequential change of the program pounter (PC) value. A non-sequential PC change can occur during

High-Speed Bus Matrix Slaves	Slave ID
AHB-APB Bridge C	5
SRAM Port 2 - DMAC Data Access	6

11.4.4. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, priority levels can be assigned to the masters for different types of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM, the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in the table below.

Table 11-6. Quality of Service

Value	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be a minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by the port ID. The lowest port ID has the highest static priority. See the tables below for details.

The MTB has a fixed QoS level HIGH (0x3).

The CPU QoS level can be written/read, using 32-bit access only, at address 0x4100C114, bits [1:0]. Its reset value is 0x3.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

Table 11-7. SRAM Port Connections QoS

SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
CM0+ - Cortex M0+ Processor	0	Bus Matrix	0x4100C114, bits[1:0](1)	0x3
DSU - Device Service Unit	1	Bus Matrix	0x4100201C, bits[1:0](1)	0x2
DMAC - Direct Memory Access Controller - Data Access	2	Bus Matrix	IP-QOSCTRL.DQOS	0x2

Table 12-13. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

12.2.5. 48 pin TQFP

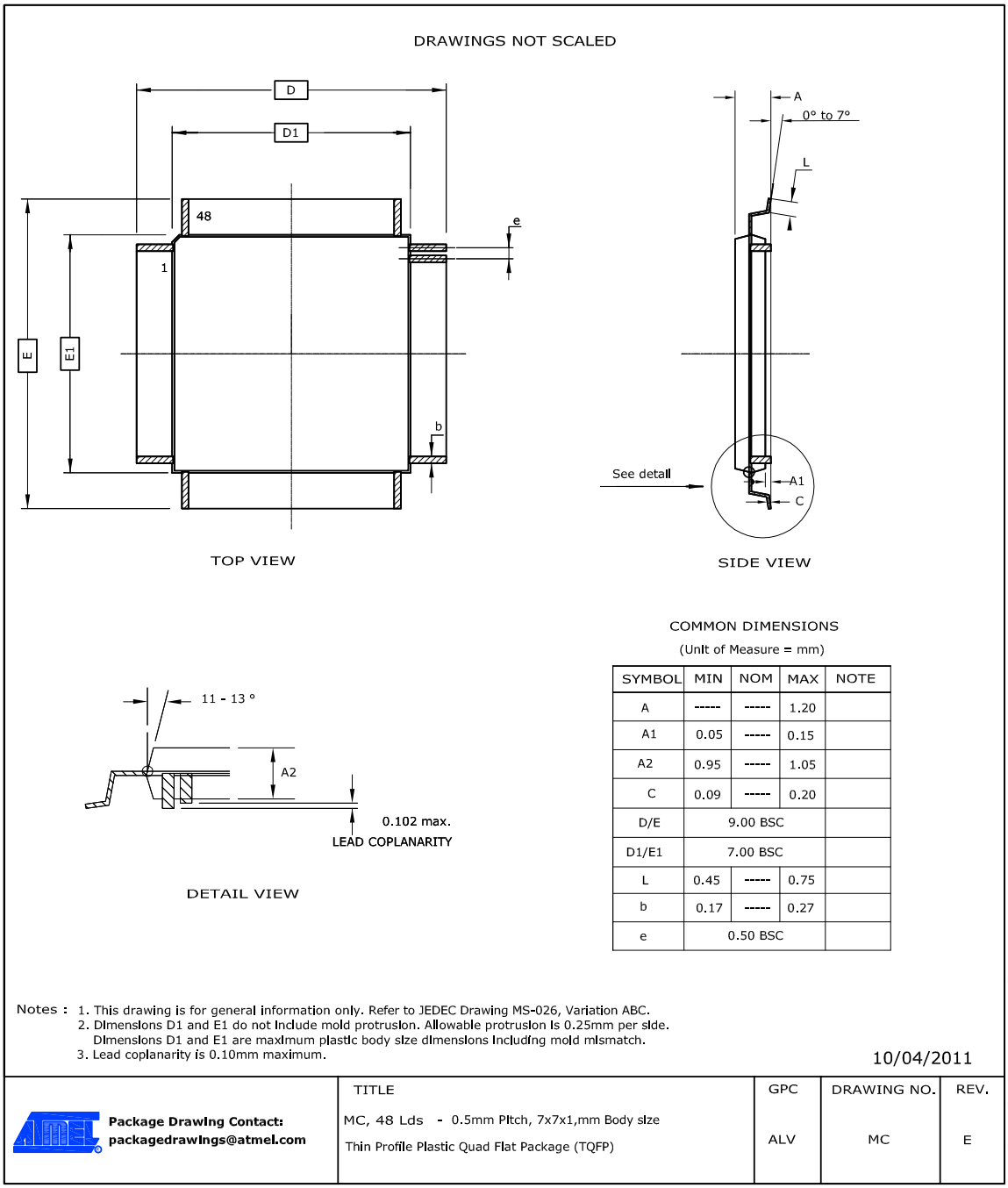


Table 12-14. Device and Package Maximum Weight

140	mg

Table 12-17. Device and Package Maximum Weight

140	mg

Table 12-18. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

12.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 12-20.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.