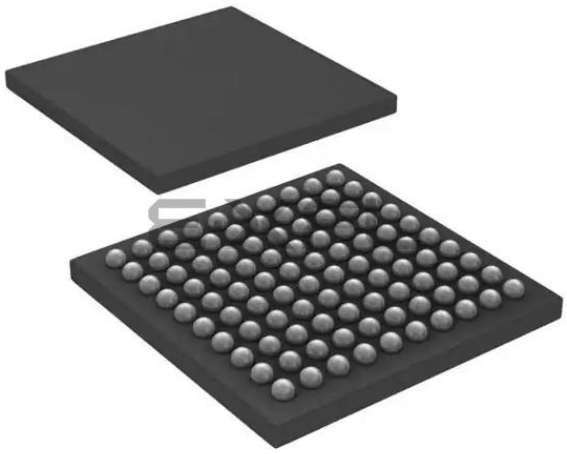

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

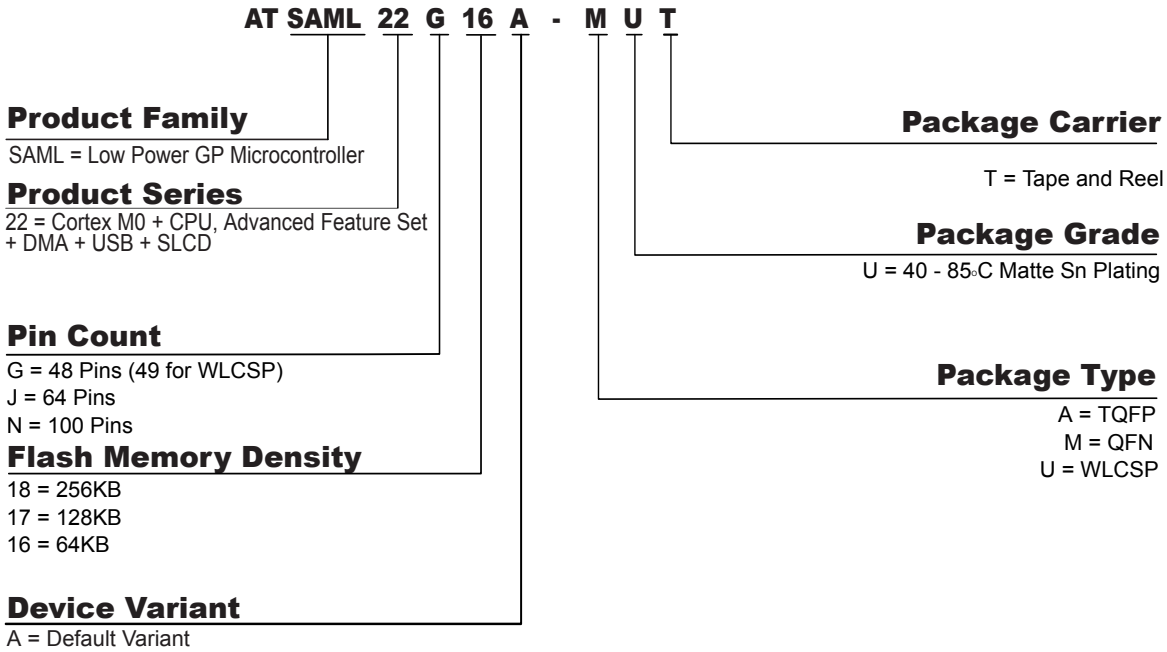
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22n16a-cfut

  - One True Random Generator (TRNG)
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - Up to 256-Channel capacitive touch sensing
      - Maximum Mutual-Cap up to 16x16 channels
      - Maximum Self-Cap up to 24 channels
    - Wake-up on touch in standby mode
- Oscillators
  - 32.768kHz crystal oscillator (XOSC32K)
  - 0.4-32MHz crystal oscillator (XOSC)
  - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
  - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
  - 48MHz Digital Frequency Locked Loop (DFLL48M)
  - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
  - Up to 82 programmable I/O pins
  - Up to 52 segment LCD pins can be used as GPIO/GPI
  - Up to 5 wake-up pins with optional debouncing
  - Up to 5 tamper input pins
  - 1 tamper output pin
- Pin and code compatible with SAM D and SAM L Cortex-M0+ Families[2]
- Packages
  - 100-pin TQFP
  - 64-pin TQFP, QFN
  - 49-pin WLCSP
  - 48-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V

[2] except the VLCD

3. Ordering Information



Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

3.1. SAM L22N

Table 3-1. SAM L22N Ordering Codes

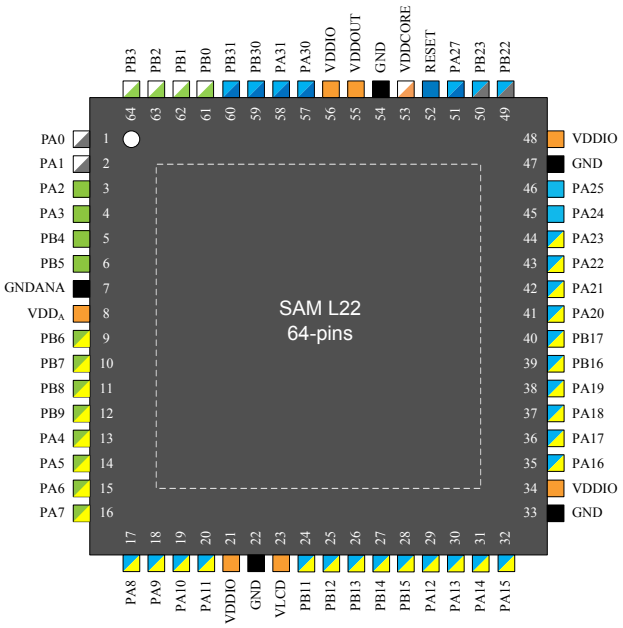
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22N16A-AUT	64K	8K	TQFP100	Tape & Reel
ATSAML22N17A-AUT	128K	16K	TQFP100	Tape & Reel
ATSAML22N18A-AUT	256K	32K	TQFP100	Tape & Reel

3.2. SAM L22J

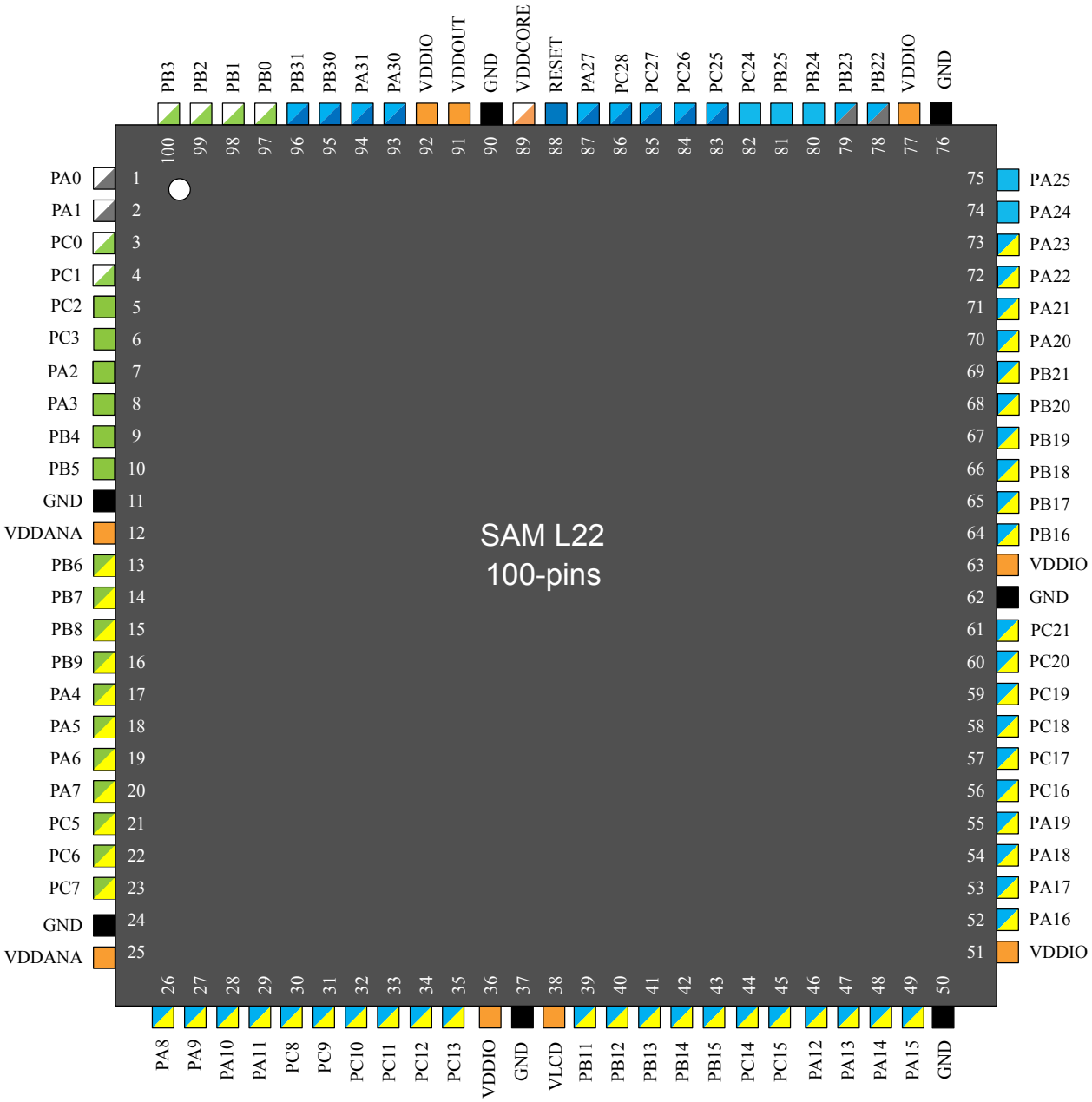
Table 3-2. SAM L22J Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J16A-AUT	64K	8K	TQFP64	Tape & Reel
ATSAML22J16A-MUT			QFN64	
ATSAML22J17A-AUT	128K	16K	TQFP64	Tape & Reel
ATSAML22J17A-MUT			QFN64	

5.2. SAM L22J


SAM L22
64-pins
PB3 64
PB2 63
PB1 62
PB0 61
PB31 60
PB30 59
PA31 58
PA30 57
VDDIO 56
VDDOUT 55
GND 54
VDDCORE 53
RESET 52
PA27 51
PB23 50
PB22 49
PA0 1
PA1 2
PA2 3
PA3 4
PB4 5
PB5 6
GNDANA 7
VDDA 8
PB6 9
PB7 10
PB8 11
PB9 12
PA4 13
PA5 14
PA6 15
PA7 16
48 VDDIO
47 GND
46 PA25
45 PA24
44 PA23
43 PA22
42 PA21
41 PA20
40 PB17
39 PB16
38 PA19
37 PA18
36 PA17
35 PA16
34 VDDIO
33 GND
17 PA8
18 PA9
19 PA10
20 PA11
21 VDDIO
22 GND
23 VLCD
24 PB11
25 PB12
26 PB13
27 PB14
28 PB15
29 PA12
30 PA13
31 PA14
32 PA15

5.3. SAM L22N


SAM L22
100-pins
PB3 100
PB2 99
PB1 98
PB0 97
PB31 96
PB30 95
PA31 94
PA30 93
VDDIO 92
VDDOUT 91
GND 90
VDDCORE 89
RESET 88
PA27 87
PC28 86
PC27 85
PC26 84
PC25 83
PC24 82
PB25 81
PB24 80
PB23 79
PB22 78
VDDIO 77
GND 76
PA0 1
PA1 2
PC0 3
PC1 4
PC2 5
PC3 6
PA2 7
PA3 8
PB4 9
PB5 10
GND 11
VDDANA 12
PB6 13
PB7 14
PB8 15
PB9 16
PA4 17
PA5 18
PA6 19
PA7 20
PC5 21
PC6 22
PC7 23
GND 24
VDDANA 25
75 PA25
74 PA24
73 PA23
72 PA22
71 PA21
70 PA20
69 PB21
68 PB20
67 PB19
66 PB18
65 PB17
64 PB16
63 VDDIO
62 GND
61 PC21
60 PC20
59 PC19
58 PC18
57 PC17
56 PC16
55 PA19
54 PA18
53 PA17
52 PA16
51 VDDIO
26 PA8
27 PA9
28 PA10
29 PA11
30 PC8
31 PC9
32 PC10
33 PC11
34 PC12
35 PC13
36 VDDIO
37 GND
38 VLCD
39 PB11
40 PB12
41 PB13
42 PB14
43 PB15
44 PC14
45 PC15
46 PA12
47 PA13
48 PA14
49 PA15
50 GND

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
	38	50	79	PB23	EIC/EXTINT[7]						SERCOM0/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	TCC/ WO[3]		GCLK/ IO[1]	CCL/ OUT[0]
			80	PB24	EIC/EXTINT[8]						SERCOM0/ PAD[0]	SERCOM4/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
			81	PB25	EIC/EXTINT[9]						SERCOM0/ PAD[1]	SERCOM4/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
			82	PC24	EIC/EXTINT[0]						SERCOM0/ PAD[2]	SERCOM4/ PAD[2]	TC/2/ WO[0]	TCC/ WO[0]			
			83	PC25	EIC/EXTINT[1]						SERCOM0/ PAD[3]	SERCOM4/ PAD[3]	TC/2/ WO[1]	TCC/ WO[1]			
			84	PC26	EIC/EXTINT[2]								TC/3/ WO[0]	TCC/ WO[2]			
			85	PC27	EIC/EXTINT[3]							SERCOM1/ PAD[0]	TC/3/ WO[1]	TCC/ WO[3]			CCL/IN[4]
			86	PC28	EIC/EXTINT[4]				PTC/ XY[20]			SERCOM1/ PAD[1]		TCC/ WO[4]			CCL/IN[5]
recommended for GCLK IO	39	51	87	PA27	EIC/EXTINT[15]				PTC/ XY[21]					TCC/ WO[5]	TAL/BRK	GCLK/ IO[0]	
	40	52	88	RESET_N													
	45	57	93	PA30	EIC/EXTINT[10]				PTC/ XY[22]			SERCOM1/ PAD[2]			CORTEX_M0P/ SWCLK	GCLK/ IO[0]	CCL/IN[3]
	46	58	94	PA31	EIC/EXTINT[11]				PTC/ XY[23]			SERCOM1/ PAD[3]			SWDIO		CCL/ OUT[1]
I2C: Sm, Fm, Fm +, Hs		59	95	PB30	EIC/EXTINT[14]						SERCOM1/ PAD[0]	SERCOM5/ PAD[0]	TCC/ WO[0]				
		60	96	PB31	EIC/EXTINT[15]						SERCOM1/ PAD[1]	SERCOM5/ PAD[1]	TCC/ WO[1]				
Battery backup		61	97	PB00	EIC/EXTINT[0]		ADC/ AIN[8]				SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]		RTC/IN[0]	SUPC/ PSOK	CCL/IN[1]
		62	98	PB01	EIC/EXTINT[1]		ADC/ AIN[9]				SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	RTC/IN[2]	RTC/OUT	SUPC/ OUT[0]	CCL/IN[2]
	47	63	99	PB02	EIC/EXTINT[2]		ADC/ AIN[10]				SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC/2/ WO[0]		RTC/IN[1]	SUPC/ OUT[1]	CCL/ OUT[0]
	48	64	100	PB03	EIC/EXTINT[3]		ADC/ AIN[11]				SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC/2/ WO[1]			SUPC/ VBAT	

Note:

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for supported I^2C modes.
   - Sm: Standard mode, up to 100kHz
   - Fm: Fast mode, up to 400kHz
   - Fm+: Fast mode Plus, up to 1MHz
   - Hs: High-speed mode, up to 3.4MHz
3. These pins are High Sink pins and have different properties than regular pins: PA12, PA13, PA22, PA23, PA27, PA31, PB30, PB31.
4. Clusters of multiple GPIO pins are sharing the same supply pin.
5. The 49th pin of the WLCSP49 package is an additional GND pin.
6. SAM L22N: SERCOM[0:5]. SAM L22G, L22J: SERCOM[0:3].

Related Links

Configuration Summary on page 7
SERCOM USART and I2C Configurations on page 23

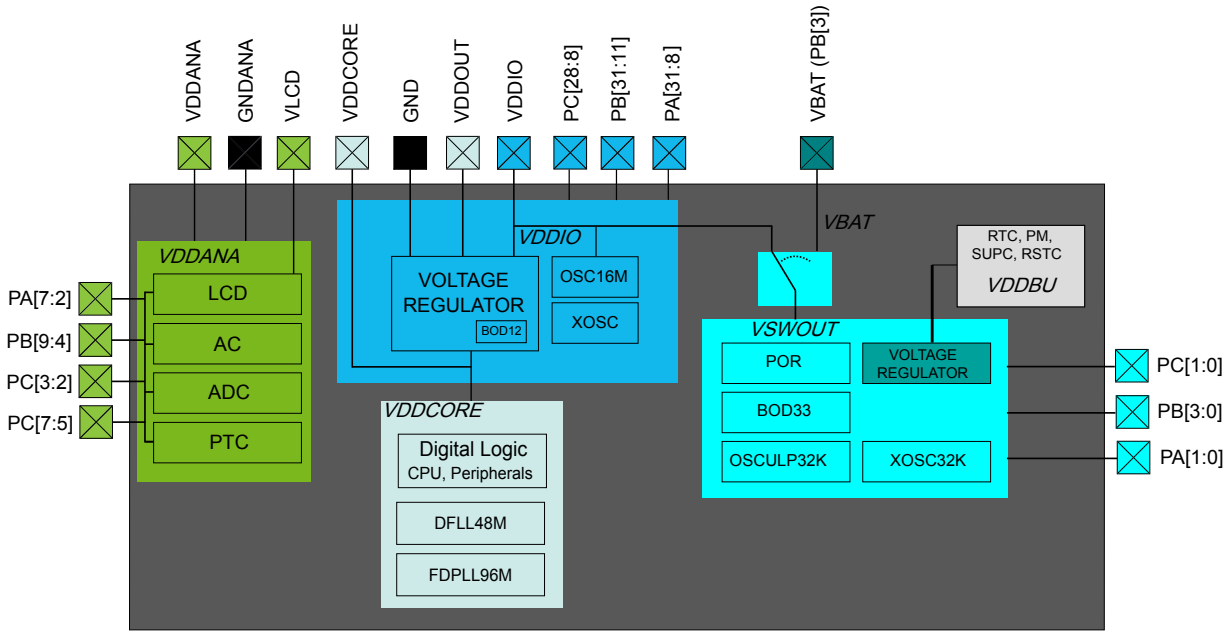
7.2. Other Functions

7.2.1. Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing is controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).

8. Power Supply and Start-Up Considerations

8.1. Power Domain Overview



The Atmel SAM L22 power domains are not independent of each other:

- VDDCORE and VDDIO share GND, whereas VDDANA refers to GNDANA.
- VDDCORE serves as the internal voltage regulator output.
- VSWOUT and VDDBU are internal power domains.

8.2. Power Supply Considerations

8.2.1. Power Supplies

The Atmel SAM L22 has several different power supply pins:

- VDDIO powers I/O lines and OSC16M, XOSC, the internal regulator for VDDCORE and the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDANA powers I/O lines and the ADC, AC, LCD, and PTC. Voltage is 1.62V to 3.63V
- VLCD has two alternative functions:
  - Output of the LCD voltage pump when VLCD is generated internally. Output voltage is 2.5V to 3.5V.
  - Supply input for the bias generator when VLCD is provided externally by the application. Input voltage is 2.4 to 3.6V.
- VBAT powers the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDCORE serves as the internal voltage regulator output. It powers the core, memories, peripherals, DFLL48M and FDPLL96M. Voltage is 0.9V to 1.2V typical.
- The Automatic Power Switch is a configurable switch that selects between VDDIO and VBAT as supply for the internal output VSWOUT, see the figure in Power Domain Overview.

Figure 8-2. Power Supply Connection for Switching/Linear Mode

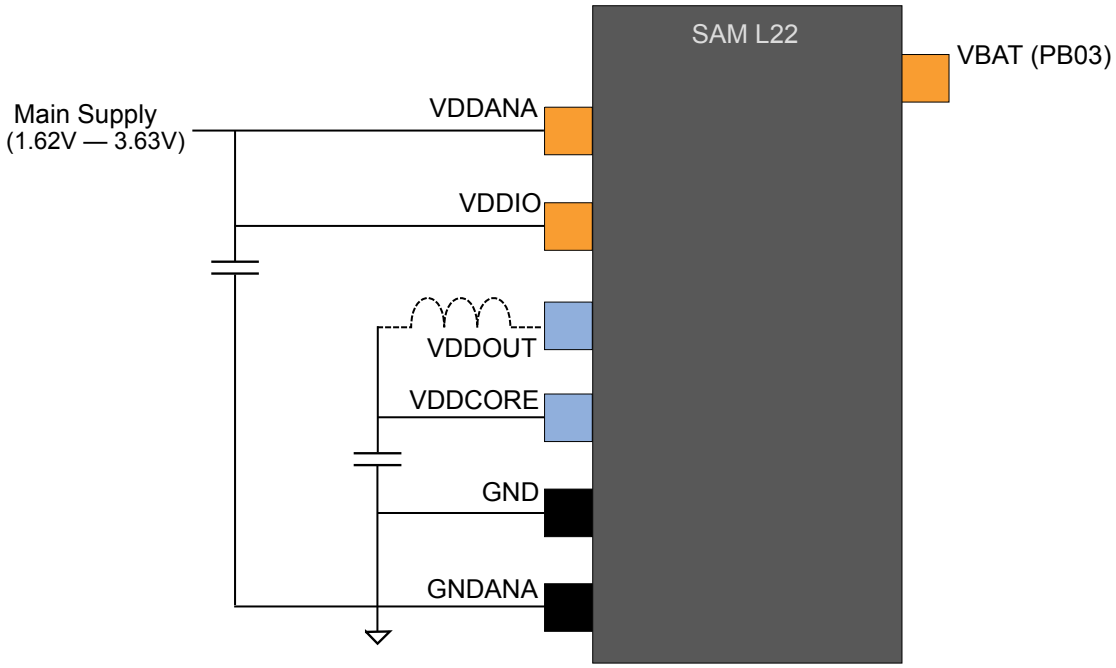
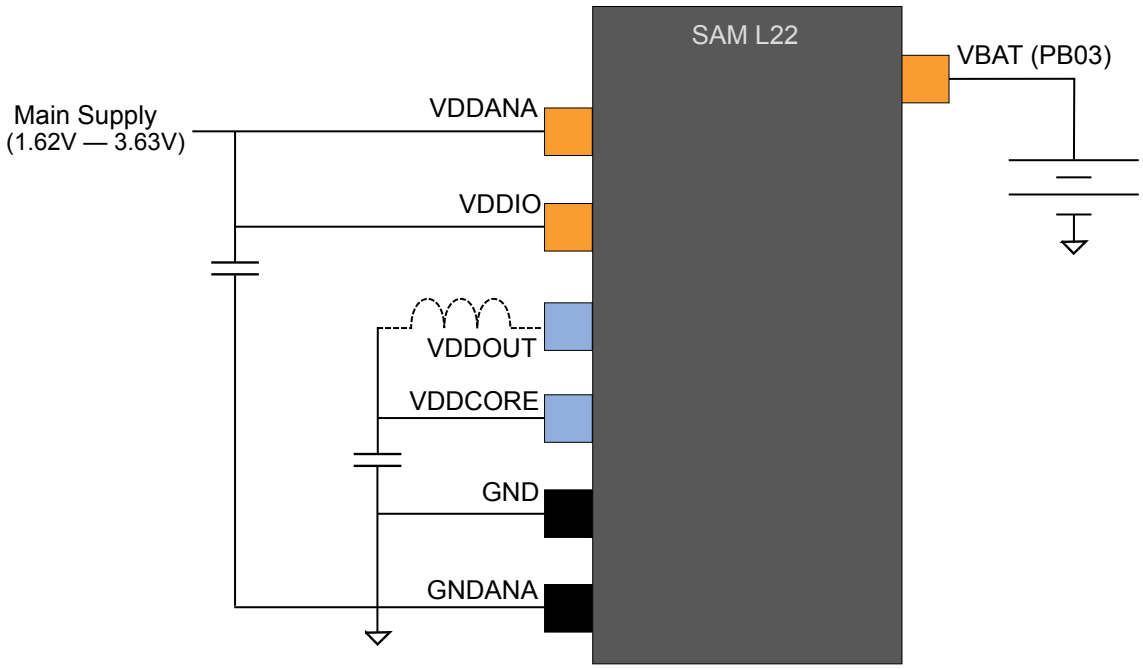


Figure 8-3. Power Supply Connection for Battery Backup



8.2.4. Power-Up Sequence

8.2.4.1. Supply Order

VDDIO and VDDANA must have the same supply sequence. Ideally, they must be connected together.

8.2.4.2. Minimum Rise Rate

One integrated power-on reset (POR) circuits monitoring VDDIO requires a minimum rise rate.

8.2.4.3. Maximum Rise Rate

The rise rate of the power supplies must not exceed the values described in Electrical Characteristics.

8.4.4. Brown-Out Detector on VDDCORE

Once the device has started up, BOD12 monitors the internal VDDCORE.

8.5. Performance Level Overview

By default, the device will start in Performance Level 0. This PL0 is aiming for the lowest power consumption by limiting logic speeds and the CPU frequency. As a consequence, all GCLK will have limited capabilities, and some peripherals and clock sources will not work or with limited capabilities:

List of peripherals/clock sources not available in PL0:

- USB (limited by logic frequency)
- DFLL48M

List of peripherals/clock sources with limited capabilities in PL0:

- All AHB/APB peripherals are limited by CPU frequency
- DPLL96M: may be able to generate 48MHz internally, but the output cannot be used by logic
- GCLK: the maximum frequency is by factor 4 compared to PL2
- SW interface: the maximum frequency is by factor 4 compared to PL2
- TC: the maximum frequency is by factor 4 compared to PL2
- TCC:the maximum frequency is by factor 4 compared to PL2
- SERCOM: the maximum frequency is by factor 4 compared to PL2

List of peripherals/clock sources with full capabilities in PL0:

- AC
- ADC
- EIC
- OSC16M
- PTC
- All 32KHz clock sources and peripherals

Full functionality and capability will be ensured in PL2. When transitioning between performance levels, the Supply Controller (SUPC) will provide a configurable smooth voltage scaling transition.

10.3. NVM User Row Mapping

The Non Volatile Memory (NVM) User Row contains calibration data that are automatically read at device power-on.

The NVM User Row can be read at address 0x00804000.

To write the NVM User Row refer to the documentation of the NVMCTRL - Non-Volatile Memory Controller.

Note: When writing to the User Row, the new values do not get loaded by the other peripherals on the device until a device Reset occurs.

Table 10-4. NVM User Row Mapping

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	0x7	NVMCTRL
3	Reserved	—	0x1	—
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	0x7	NVMCTRL
7	Reserved	—	0x1	—
13:8	BOD33 Level	BOD33 threshold level at power-on.	0x06	SUPC.BOD33
14	BOD33 Disable	BOD33 Disable at power-on.	0x0	SUPC.BOD33
16:15	BOD33 Action	BOD33 Action at power-on.	0x1	SUPC.BOD33
25:17	Reserved	Factory settings - do not change.	0x08F	-
26	WDT Enable	WDT Enable at power-on.	0x0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power-on.	0x0	WDT.CTRLA
31:28	WDT Period	WDT Period at power-on.	0xB	WDT.CONFIG
35:32	WDT Window	WDT Window mode time-out at power-on.	0xB	WDT.CONFIG
39:36	WDT EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on.	0xB	WDT.EWCTRL
40	WDT WEN	WDT Timer Window Mode Enable at power-on.	0x0	WDT.CTRLA
41	BOD33 Hysteresis	BOD33 Hysteresis configuration at power-on.	0x0	SUPC.BOD33
47:42	Reserved	Factory settings - do not change.	0x3E	—
63:48	LOCK	NVM Region Lock Bits.	0xFFFF	NVMCTRL

11. Processor and Architecture

11.1. Cortex M0+ Processor

The Atmel SAM L22 implements the ARM ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

11.1.1. Cortex M0+ Configuration

Table 11-1. Cortex M0+ Configuration

Features	Cortex-M0+ options	SAM L22 configuration
Interrupts	External interrupts 0-32	27
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

11.1.2. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

Peripheral source	NVIC line
EVSYS – Event System	8
SERCOM0 – Serial Communication Interface 0	9
SERCOM1 – Serial Communication Interface 1	10
SERCOM2 – Serial Communication Interface 2	11
SERCOM3 – Serial Communication Interface 3	12
SERCOM4 – Serial Communication Interface 4	13
SERCOM5 – Serial Communication Interface 5	14
TCC0 – Timer Counter for Control 0	15
TC0 – Timer Counter 0	16
TC1 – Timer Counter 1	17
TC2 – Timer Counter 2	18
TC3 – Timer Counter 3	19
ADC – Analog-to-Digital Converter	20
AC – Analog Comparator	21
PTC – Peripheral Touch Controller	22
SLCD - Segmented LCD Controller	23
AES - Advanced Encryption Standard module	24
TRNG - True Random Number Generator	25

11.3. Micro Trace Buffer

11.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

11.3.2. Overview

When enabled, the MTB records the changes in program flow that are reported by the Cortex-M0+ processor over the execution trace interface. This interface is shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. The information is stored by the MTB in the SRAM as trace packets. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB stores trace information into the SRAM and gives the processor access to the SRAM simultaneously. The MTB ensures that trace write accesses have priority over processor accesses.

An execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects a non-sequential change of the program pounter (PC) value. A non-sequential PC change can occur during

branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has four programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit
- MASTER: Contains the main trace enable bit and other trace control fields
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location by a debug agent

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

11.4. High-Speed Bus System

11.4.1. Overview

11.4.2. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

12. Packaging Information

12.1. Thermal Considerations

12.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 12-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
48-pin TQFP	64.2°C/W	12.3°C/W
64-pin TQFP	60.8°C/W	12.0°C/W
100-pin TQFP	58.5°C/W	12.7°C/W
48-pin QFN	32.4°C/W	11.2°C/W
64-pin QFN	32.7°C/W	10.8°C/W
49-pin WLCSP	37.3°C/W	5.8°C/W

Related Links

Junction Temperature on page 42

12.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

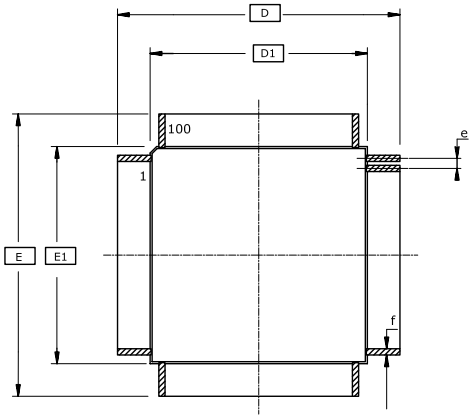
Related Links

Thermal Resistance Data on page 42

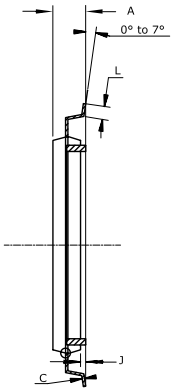
12.2. Package Drawings

12.2.1. 100 pin TQFP

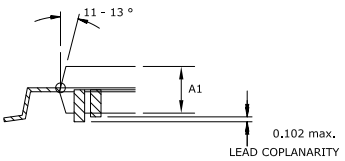
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



DETAIL VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		16.00		
D1/E1		14.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		100		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 12-2. Device and Package Maximum Weight

520	mg

Table 12-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-4. Package Reference

JEDEC Drawing Reference	MS-026, variant AED
JESD97 Classification	e3

Table 12-8. Device and Package Maximum Weight

200	mg

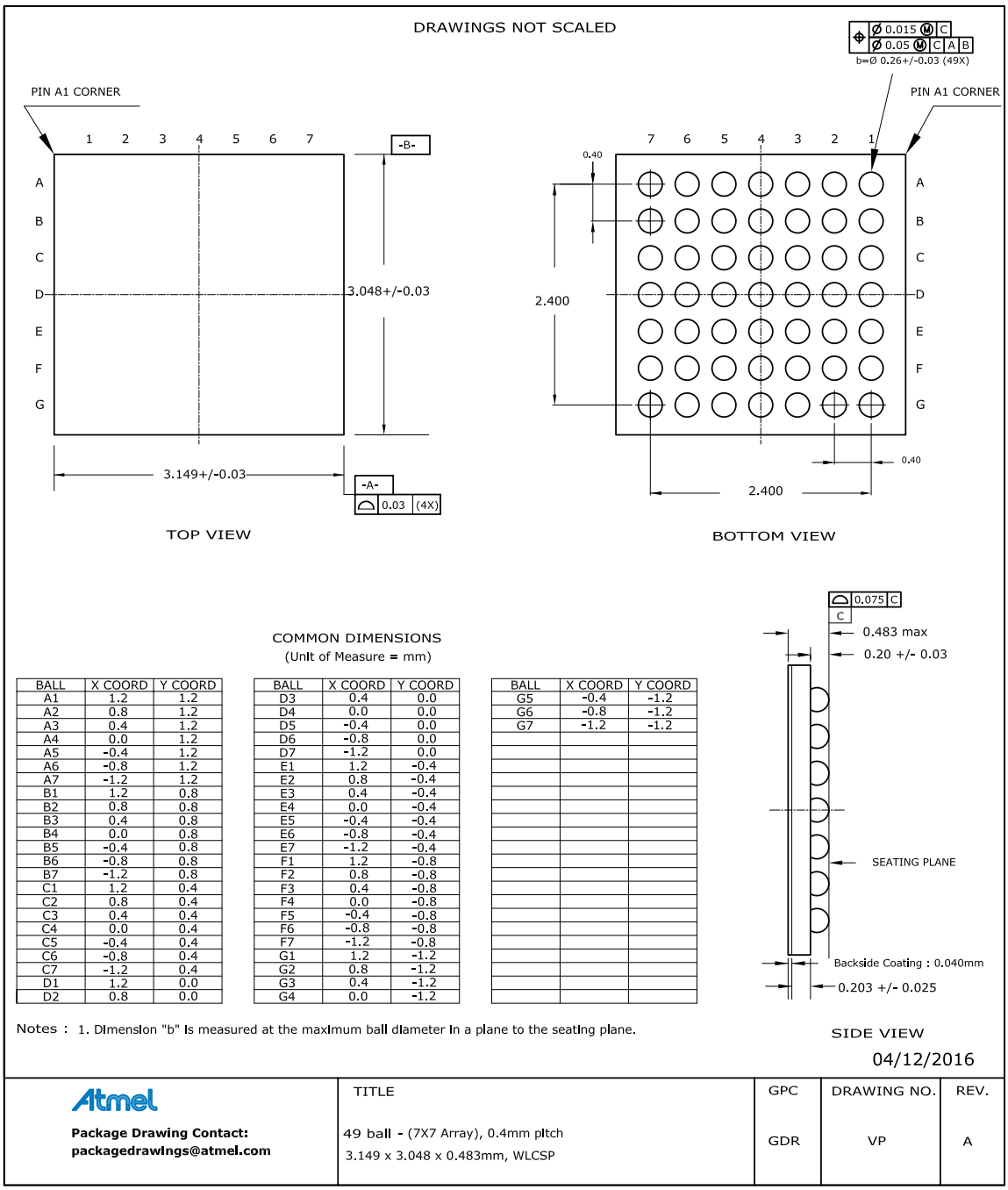
Table 12-9. Package Charateristics

Moisture Sensitivity Level	MSL3

Table 12-10. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

12.2.4. 49-Ball WLCSP



BALL	X COORD	Y COORD
A1	1.2	1.2
A2	0.8	1.2
A3	0.4	1.2
A4	0.0	1.2
A5	-0.4	1.2
A6	-0.8	1.2
A7	-1.2	1.2
B1	1.2	0.8
B2	0.8	0.8
B3	0.4	0.8
B4	0.0	0.8
B5	-0.4	0.8
B6	-0.8	0.8
B7	-1.2	0.8
C1	1.2	0.4
C2	0.8	0.4
C3	0.4	0.4
C4	0.0	0.4
C5	-0.4	0.4
C6	-0.8	0.4
C7	-1.2	0.4
D1	1.2	0.0
D2	0.8	0.0

BALL	X COORD	Y COORD
D3	0.4	0.0
D4	0.0	0.0
D5	-0.4	0.0
D6	-0.8	0.0
D7	-1.2	0.0
E1	1.2	-0.4
E2	0.8	-0.4
E3	0.4	-0.4
E4	0.0	-0.4
E5	-0.4	-0.4
E6	-0.8	-0.4
E7	-1.2	-0.4
F1	1.2	-0.8
F2	0.8	-0.8
F3	0.4	-0.8
F4	0.0	-0.8
F5	-0.4	-0.8
F6	-0.8	-0.8
F7	-1.2	-0.8
G1	1.2	-1.2
G2	0.8	-1.2
G3	0.4	-1.2
G4	0.0	-1.2

BALL	X COORD	Y COORD
G5	-0.4	-1.2
G6	-0.8	-1.2
G7	-1.2	-1.2

Table 12-11. Device and Package Maximum Weight

8.45	mg

Table 12-12. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 12-13. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

12.2.5. 48 pin TQFP

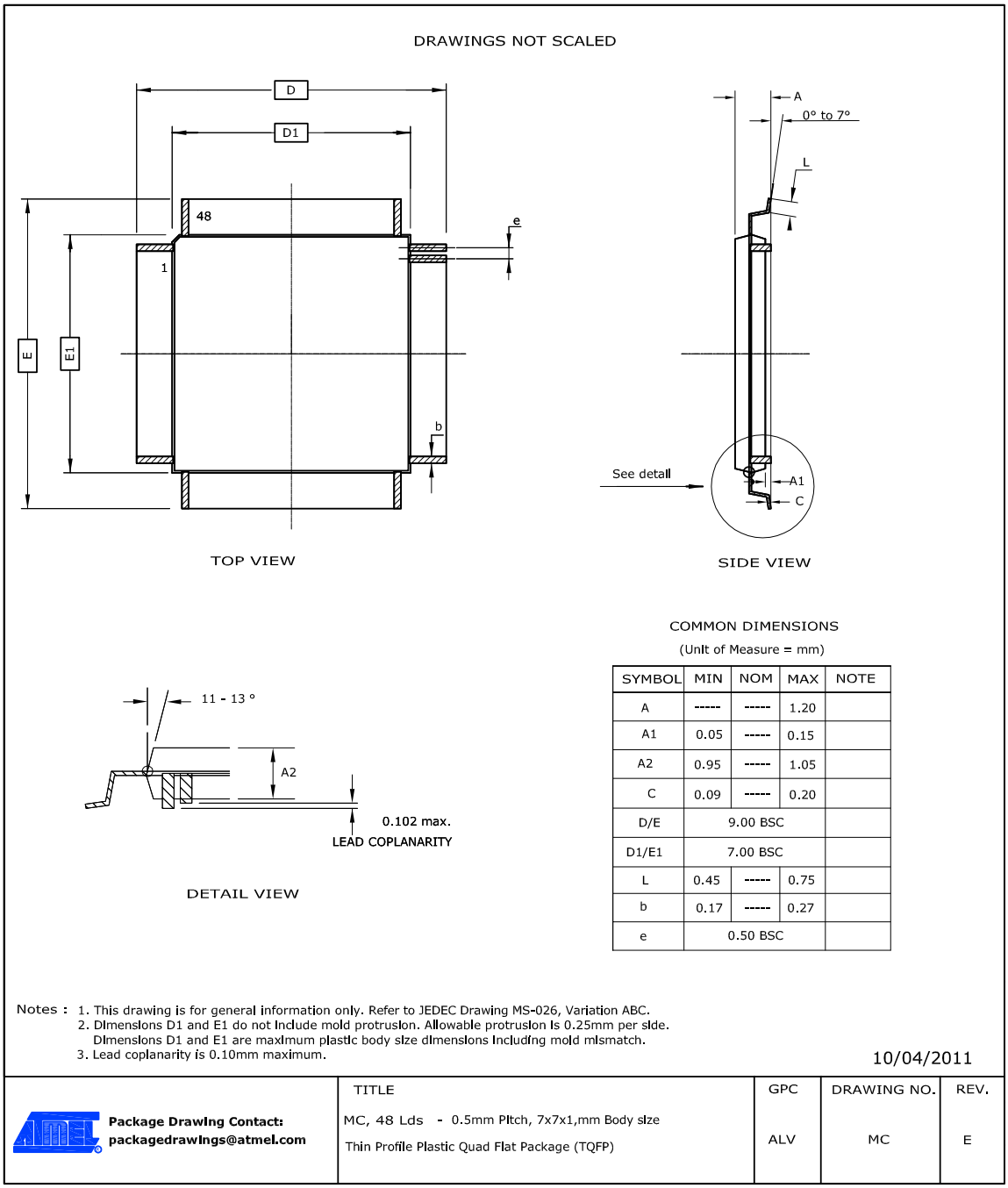


Table 12-14. Device and Package Maximum Weight

140	mg

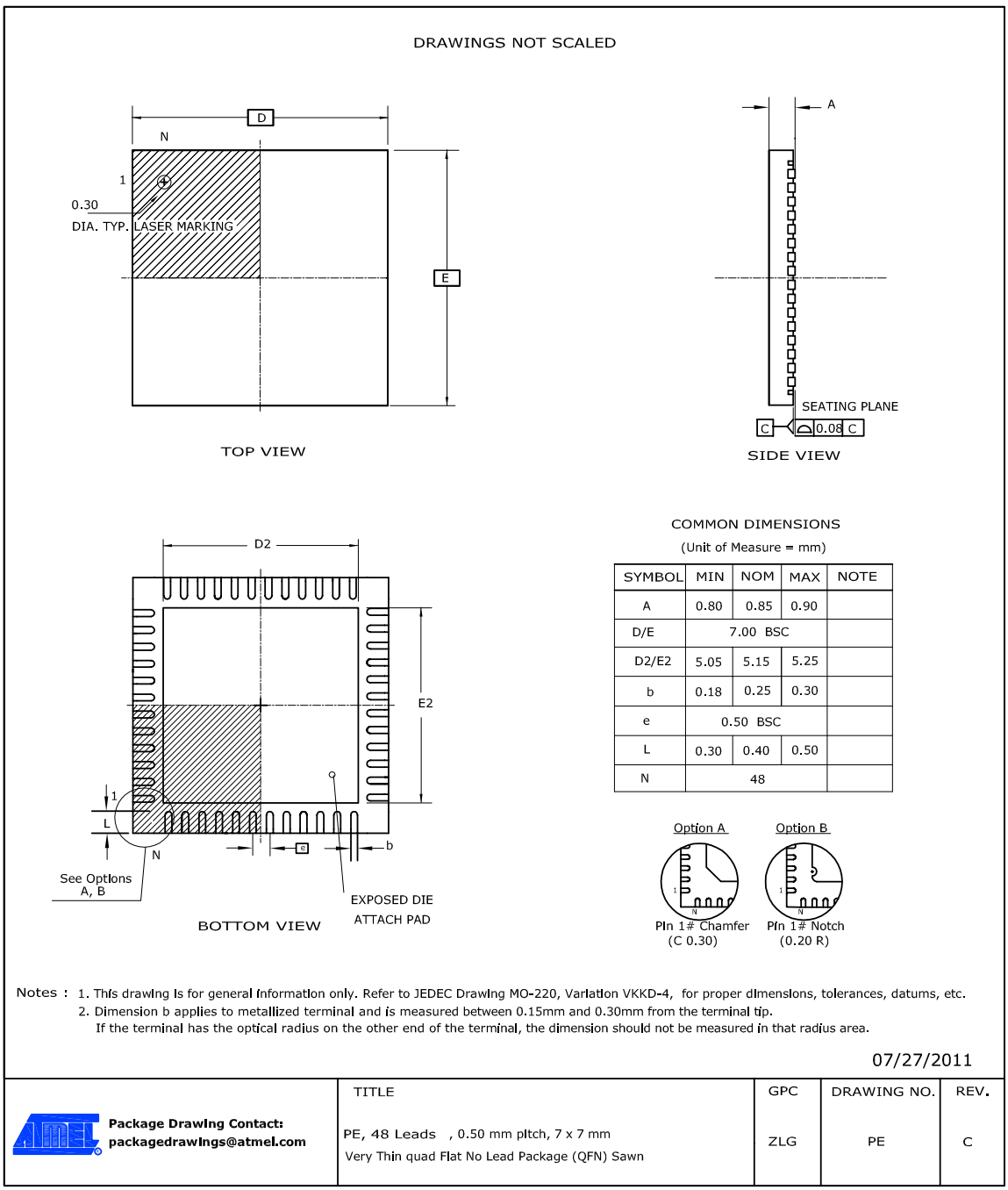
Table 12-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.6. 48 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

Table 12-17. Device and Package Maximum Weight

140	mg

Table 12-18. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-19. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

12.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 12-20.

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.