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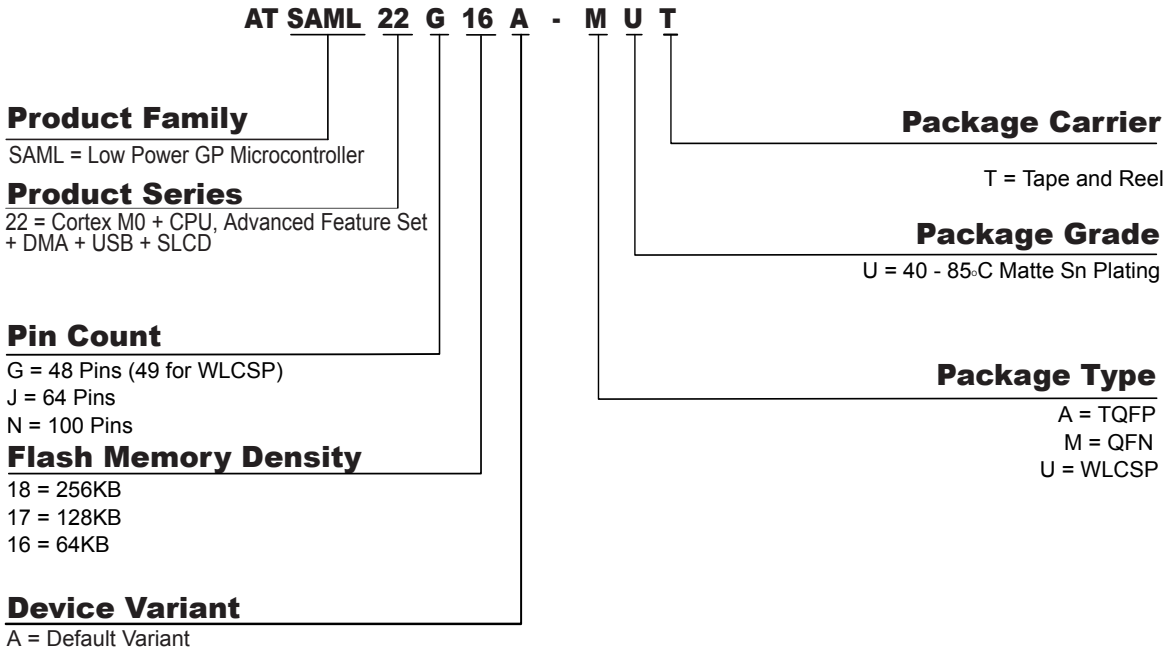
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22n17a-aut

3. Ordering Information



Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

3.1. SAM L22N

Table 3-1. SAM L22N Ordering Codes

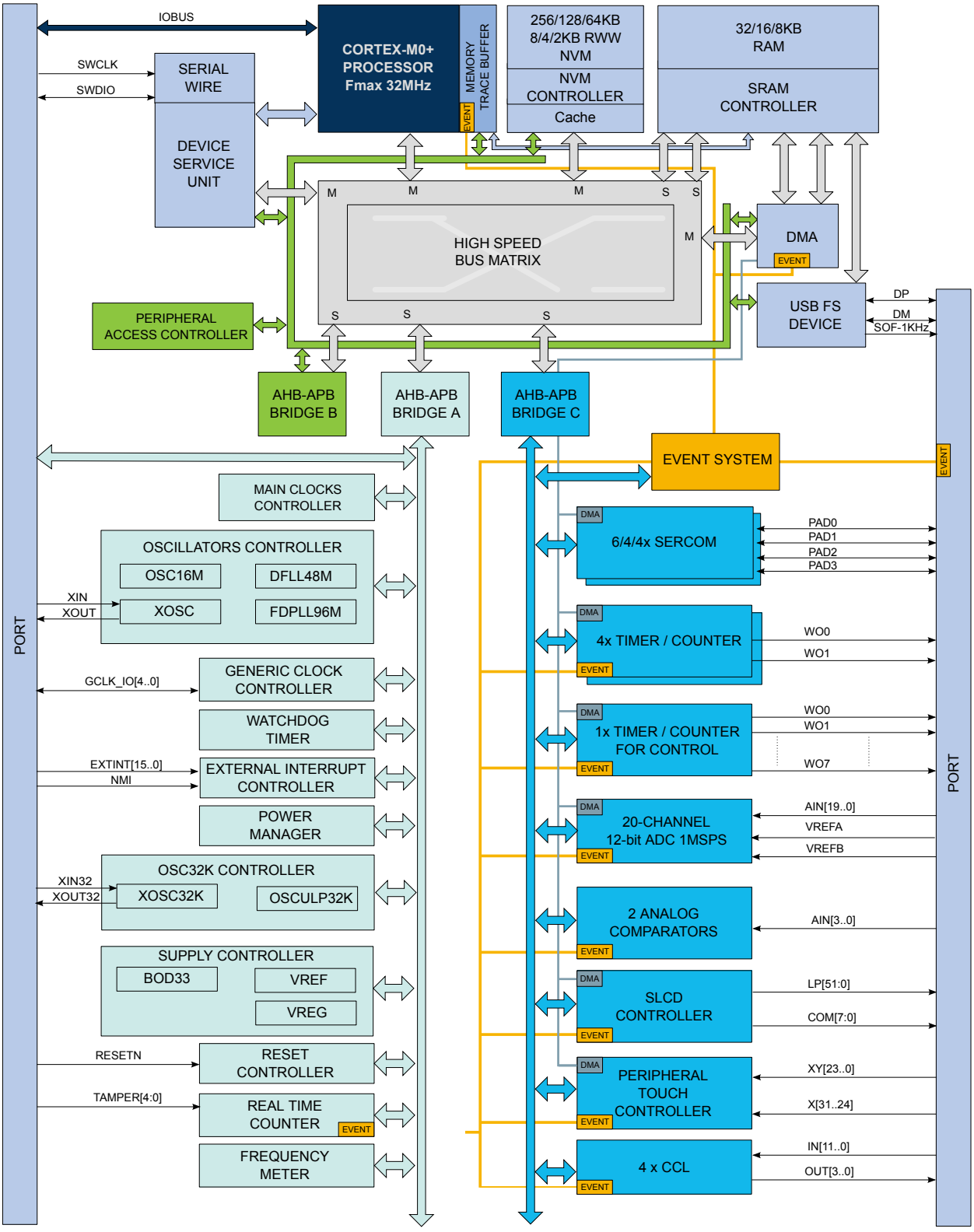
Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22N16A-AUT	64K	8K	TQFP100	Tape & Reel
ATSAML22N17A-AUT	128K	16K	TQFP100	Tape & Reel
ATSAML22N18A-AUT	256K	32K	TQFP100	Tape & Reel

3.2. SAM L22J

Table 3-2. SAM L22J Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J16A-AUT	64K	8K	TQFP64	Tape & Reel
ATSAML22J16A-MUT			QFN64	
ATSAML22J17A-AUT	128K	16K	TQFP64	Tape & Reel
ATSAML22J17A-MUT			QFN64	

4. Block Diagram



Note:

5. Pinout

5.1. SAM L22G

Figure 5-1. 48-Pin QFN, TQFP

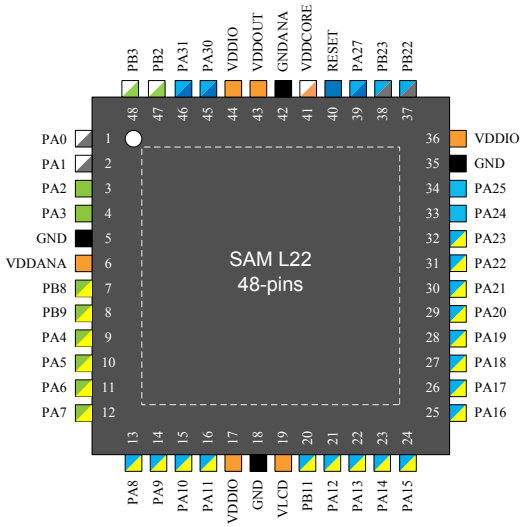
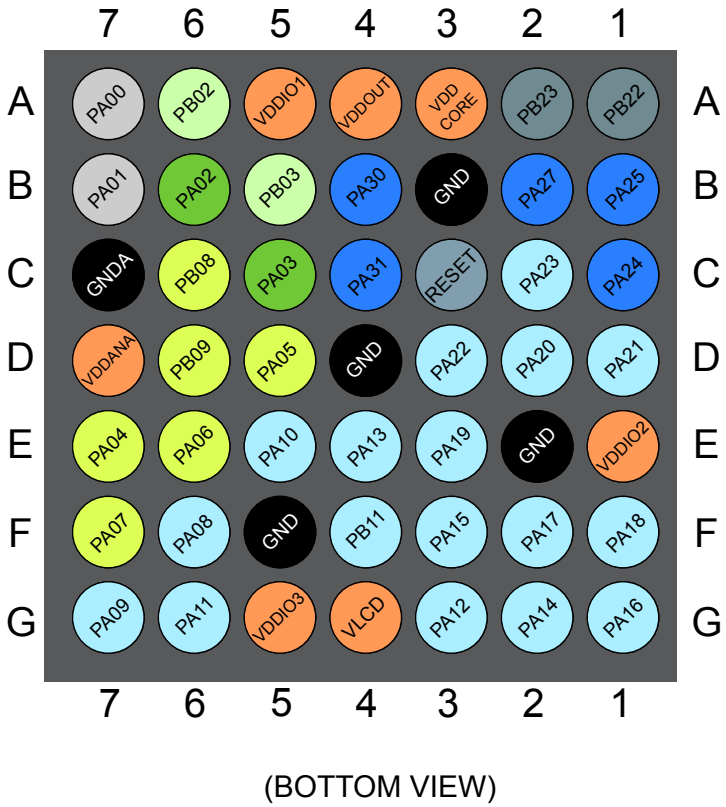


Figure 5-2. 49-Pin WLCSP



(BOTTOM VIEW)

6. Signal Descriptions List

The following table gives details on signal names classified by peripheral.

Table 6-1. Signal Descriptions List

Signal Name	Function	Type	Active Level
Analog Comparators - AC			
AIN[3:0]	AC Analog Inputs	Analog	
CMP[1:0]	AC Analog Output	Analog	
Analog Digital Converter - ADC			
AIN[19:0]	ADC Analog Inputs	Analog	
VREFA	ADC Voltage External Reference A	Analog	
VREFB	ADC Voltage External Reference B	Analog	
External Interrupt Controller - EIC			
EXTINT[15:0]	External Interrupts inputs	Digital	
NMI	External Non-Maskable Interrupt input	Digital	
Generic Clock Generator - GCLK			
GCLK_IO[4:0]	Generic Clock (source clock inputs or generic clock generator output)	Digital	
Custom Control Logic - CCL			
IN[11:0]	Logic Inputs	Digital	
OUT[3:0]	Logic Outputs	Digital	
Supply Controller - SUPC			
VBAT	External battery supply Inputs	Analog	
PSOK	Main Power Supply OK input	Digital	
OUT[1:0]	Logic Outputs	Digital	
Power Manager - PM			
RESETN	Reset input	Digital	Low
Serial Communication Interface - SERCOMx			
PAD[3:0]	SERCOM Inputs/Outputs Pads	Digital	
Oscillators Control - OSCCTRL			
XIN	Crystal or external clock Input	Analog/Digital	
XOUT	Crystal Output	Analog	

7. I/O Multiplexing and Considerations

7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned a different peripheral functions. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral function A to I is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) of the PORT.

This table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 7-1. PORT Function Multiplexing

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
Battery backup	1	1	1	PA00	EIC/EXTINT[0]							SERCOM1/ PAD[0]					
	2	2	2	PA01	EIC/EXTINT[1]							SERCOM1/ PAD[1]					
			3	PC00	EIC/EXTINT[8]		ADC/ AIN[16]								RTC/IN[3]		
			4	PC01	EIC/EXTINT[9]		ADC/ AIN[17]								RTC/IN[4]		
			5	PC02	EIC/EXTINT[10]		ADC/ AIN[18]		PTC/ XY[6]								
			6	PC03	EIC/EXTINT[11]		ADC/ AIN[19]		PTC/ XY[7]								
	3	3	7	PA02	EIC/EXTINT[2]	ADC/ VREFB	ADC/ AIN[0]	AC/ AIN[0]	PTC/ XY[8]						RTC/IN[2]		
	4	4	8	PA03	EIC/EXTINT[3]	ADC/ VREFA	ADC/ AIN[1]	AC/ AIN[1]	PTC/ XY[9]								
		5	9	PB04	EIC/EXTINT[4]		ADC/ AIN[12]	AC/ AIN[2]	PTC/ XY[10]								
		6	10	PB05	EIC/EXTINT[5]		ADC/ AIN[13]	AC/ AIN[3]	PTC/ XY[11]								
		9	13	PB06	EIC/EXTINT[6]		ADC/ AIN[14]		PTC/ XY[12]	SLCD/ LP[0]							CCL/IN[6]
		10	14	PB07	EIC/EXTINT[7]		ADC/ AIN[15]		PTC/ XY[13]	SLCD/ LP[1]							CCL/IN[7]
	7	11	15	PB08	EIC/EXTINT[8]		ADC/ AIN[2]		PTC/ XY[14]	SLCD/ LP[2]		SERCOM3/ PAD[0]	TC/0/ WO[0]				CCL/IN[8]
	8	12	16	PB09	EIC/EXTINT[9]		ADC/ AIN[3]		PTC/ XY[15]	SLCD/ LP[3]		SERCOM3/ PAD[1]	TC/0/ WO[1]				CCL/ OUT[2]
	9	13	17	PA04	EIC/EXTINT[4]		ADC/ AIN[4]		PTC/ X[24]	SLCD/ LP[4]		SERCOM0/ PAD[0]	TCC/ WO[0]				CCL/IN[0]
	10	14	18	PA05	EIC/EXTINT[5]		ADC/ AIN[5]		PTC/ X[25]	SLCD/ LP[5]		SERCOM0/ PAD[1]	TCC/ WO[1]				CCL/IN[1]
	11	15	19	PA06	EIC/EXTINT[6]		ADC/ AIN[6]		PTC/ X[26]	SLCD/ LP[6]		SERCOM0/ PAD[2]					CCL/IN[2]
	12	16	20	PA07	EIC/EXTINT[7]		ADC/ AIN[7]		PTC/ X[27]	SLCD/ LP[7]		SERCOM0/ PAD[3]					CCL/ OUT[0]
			21	PC05	EIC/EXTINT[13]				PTC/ XY[4]	SLCD/ LP[8]							
			22	PC06	EIC/EXTINT[14]				PTC/ XY[5]	SLCD/ LP[9]							
			23	PC07	EIC/EXTINT[15]					SLCD/ LP[10]							
	13	17	26	PA08	EIC/NMI				PTC/ XY[3]	SLCD/ LP[11]	SERCOM0/ PAD[0]	SERCOM4/ PAD[0]	TCC/ WO[0]				CCL/IN[3]
	14	18	27	PA09	EIC/EXTINT[9]				PTC/ XY[2]	SLCD/ LP[12]	SERCOM0/ PAD[1]	SERCOM4/ PAD[1]	TCC/ WO[1]				CCL/IN[4]
	15	19	28	PA10	EIC/EXTINT[10]				PTC/ XY[1]	SLCD/ LP[13]	SERCOM0/ PAD[2]	SERCOM4/ PAD[2]		TCC/ WO[2]		GCLK/ IO[4]	CCL/IN[5]
	16	20	29	PA11	EIC/EXTINT[11]				PTC/ XY[0]	SLCD/ LP[14]	SERCOM0/ PAD[3]	SERCOM4/ PAD[3]		TCC/ WO[3]			CCL/ OUT[1]

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
digital: input only			30	PC08	EIC/EXTINT[0]					SLCD/ LP[15]							
			31	PC09	EIC/EXTINT[1]					SLCD/ LP[16]							
			32	PC10	EIC/EXTINT[2]					SLCD/ LP[17]	SERCOM1/ PAD[2]						
			33	PC11	EIC/EXTINT[3]					SLCD/ LP[18]	SERCOM1/ PAD[3]						
			34	PC12	EIC/EXTINT[4]					SLCD/ LP[19]	SERCOM1/ PAD[0]						
			35	PC13	EIC/EXTINT[5]					SLCD/ LP[20]	SERCOM1/ PAD[1]						
	19	23	38	VLCD													
	20	24	39	PB11	EIC/EXTINT[11]					SLCD/ LP[21]		SERCOM3/ PAD[3]	TC/1/ WO[1]	TCC/ WO[5]			CCL/ OUT[1]
I2C: full Fm+. Limited currents for Sm, Fm		25	40	PB12	EIC/EXTINT[12]					SLCD/ LP[22]	SERCOM3/ PAD[0]		TC/0/ WO[0]	TCC/ WO[6]			
		26	41	PB13	EIC/EXTINT[13]					SLCD/ LP[23]	SERCOM3/ PAD[1]		TC/0/ WO[1]	TCC/ WO[7]			
		27	42	PB14	EIC/EXTINT[14]					SLCD/ LP[24]	SERCOM3/ PAD[2]		TC/1/ WO[0]			GCLK/ IO[0]	CCL/IN[9]
		28	43	PB15	EIC/EXTINT[15]					SLCD/ LP[25]	SERCOM3/ PAD[3]		TC/1/ WO[1]			GCLK/ IO[1]	CCL/ IN[10]
			44	PC14	EIC/EXTINT[6]					SLCD/ LP[26]							
			45	PC15	EIC/EXTINT[7]					SLCD/ LP[27]							
I2C: Sm, Fm, Fm+	21	29	46	PA12	EIC/EXTINT[12]					SLCD/ LP[28]	SERCOM4/ PAD[0]	SERCOM3/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
	22	30	47	PA13	EIC/EXTINT[13]					SLCD/ LP[29]	SERCOM4/ PAD[1]	SERCOM3/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
	23	31	48	PA14	EIC/EXTINT[14]					SLCD/ LP[30]	SERCOM4/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[4]		GCLK/ IO[0]	
	24	32	49	PA15	EIC/EXTINT[15]					SLCD/ LP[31]	SERCOM4/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[5]		GCLK/ IO[1]	
	25	35	52	PA16	EIC/EXTINT[0]				PTC/ X[28]	SLCD/ LP[32]	SERCOM1/ PAD[0]	SERCOM2/ PAD[0]		TCC/ WO[6]		GCLK/ IO[2]	CCL/IN[0]
	26	36	53	PA17	EIC/EXTINT[1]				PTC/ X[29]	SLCD/ LP[33]	SERCOM1/ PAD[1]	SERCOM2/ PAD[1]		TCC/ WO[7]		GCLK/ IO[3]	CCL/IN[1]
	27	37	54	PA18	EIC/EXTINT[2]				PTC/ X[30]	SLCD/ LP[34]	SERCOM1/ PAD[2]	SERCOM2/ PAD[2]		TCC/ WO[2]		AC/ CMP[0]	CCL/IN[2]
	28	38	55	PA19	EIC/EXTINT[3]				PTC/ X[31]	SLCD/ LP[35]	SERCOM1/ PAD[3]	SERCOM2/ PAD[3]		TCC/ WO[3]		AC/ CMP[1]	CCL/ OUT[0]
			56	PC16	EIC/EXTINT[8]					SLCD/ LP[36]							
			57	PC17	EIC/EXTINT[9]					SLCD/ LP[37]							
digital: input only			58	PC18	EIC/EXTINT[10]					SLCD/ LP[38]							
			59	PC19	EIC/EXTINT[11]					SLCD/ LP[39]							
			60	PC20	EIC/EXTINT[12]					SLCD/ LP[40]							CCL/IN[9]
			61	PC21	EIC/EXTINT[13]					SLCD/ LP[41]							CCL/ IN[10]
		39	64	PB16	EIC/EXTINT[0]					SLCD/ LP[42]	SERCOM5/ PAD[0]		TC/2/ WO[0]	TCC/ WO[4]		GCLK/ IO[2]	CCL/IN[11]
		40	65	PB17	EIC/EXTINT[1]					SLCD/ LP[43]	SERCOM5/ PAD[1]		TC/2/ WO[1]	TCC/ WO[5]		GCLK/ IO[3]	CCL/ OUT[3]
			66	PB18	EIC/EXTINT[2]					SLCD/ LP[44]	SERCOM5/ PAD[2]	SERCOM3/ PAD[2]		TCC/ WO[0]			
			67	PB19	EIC/EXTINT[3]					SLCD/ LP[45]	SERCOM5/ PAD[3]	SERCOM3/ PAD[3]		TCC/ WO[1]			
			68	PB20	EIC/EXTINT[4]					SLCD/ LP[46]	SERCOM3/ PAD[0]	SERCOM5/ PAD[0]		TCC/ WO[2]			
			69	PB21	EIC/EXTINT[5]					SLCD/ LP[47]	SERCOM3/ PAD[1]	SERCOM5/ PAD[1]		TCC/ WO[3]			
	29	41	70	PA20	EIC/EXTINT[4]				PTC/ XY[16]	SLCD/ LP[48]	SERCOM0/ PAD[0]	SERCOM2/ PAD[2]	TC/3/ WO[0]	TCC/ WO[6]		GCLK/ IO[4]	
	30	42	71	PA21	EIC/EXTINT[5]				PTC/ XY[17]	SLCD/ LP[49]	SERCOM0/ PAD[1]	SERCOM2/ PAD[3]	TC/3/ WO[1]	TCC/ WO[7]			
I2C: Sm, Fm, Fm+	31	43	72	PA22	EIC/EXTINT[6]				PTC/ XY[18]	SLCD/ LP[50]	SERCOM0/ PAD[2]	SERCOM2/ PAD[0]	TC/0/ WO[0]	TCC/ WO[4]			CCL/IN[6]
	32	44	73	PA23	EIC/EXTINT[7]				PTC/ XY[19]	SLCD/ LP[51]	SERCOM0/ PAD[3]	SERCOM2/ PAD[1]	TC/0/ WO[1]	TCC/ WO[5]	USB/SOF_1KHZ		CCL/IN[7]
	33	45	74	PA24	EIC/EXTINT[12]						SERCOM2/ PAD[2]	SERCOM5/ PAD[0]	TC/1/ WO[0]	TCC/ WO[0]	USB/DM		CCL/IN[8]
	34	46	75	PA25	EIC/EXTINT[13]						SERCOM2/ PAD[3]	SERCOM5/ PAD[1]	TC/1/ WO[1]	TCC/ WO[1]	USB/DP		CCL/ OUT[2]
	37	49	78	PB22	EIC/EXTINT[6]						SERCOM0/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]	TCC/ WO[2]	USB/SOF_1KHZ	GCLK/ IO[0]	CCL/IN[0]

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
	38	50	79	PB23	EIC/EXTINT[7]						SERCOM0/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	TCC/ WO[3]		GCLK/ IO[1]	CCL/ OUT[0]
			80	PB24	EIC/EXTINT[8]						SERCOM0/ PAD[0]	SERCOM4/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
			81	PB25	EIC/EXTINT[9]						SERCOM0/ PAD[1]	SERCOM4/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
			82	PC24	EIC/EXTINT[0]						SERCOM0/ PAD[2]	SERCOM4/ PAD[2]	TC/2/ WO[0]	TCC/ WO[0]			
			83	PC25	EIC/EXTINT[1]						SERCOM0/ PAD[3]	SERCOM4/ PAD[3]	TC/2/ WO[1]	TCC/ WO[1]			
			84	PC26	EIC/EXTINT[2]								TC/3/ WO[0]	TCC/ WO[2]			
			85	PC27	EIC/EXTINT[3]							SERCOM1/ PAD[0]	TC/3/ WO[1]	TCC/ WO[3]			CCL/IN[4]
			86	PC28	EIC/EXTINT[4]				PTC/ XY[20]			SERCOM1/ PAD[1]		TCC/ WO[4]			CCL/IN[5]
recommended for GCLK IO	39	51	87	PA27	EIC/EXTINT[15]				PTC/ XY[21]					TCC/ WO[5]	TAL/BRK	GCLK/ IO[0]	
	40	52	88	RESET_N													
	45	57	93	PA30	EIC/EXTINT[10]				PTC/ XY[22]			SERCOM1/ PAD[2]			CORTEX_M0P/ SWCLK	GCLK/ IO[0]	CCL/IN[3]
	46	58	94	PA31	EIC/EXTINT[11]				PTC/ XY[23]			SERCOM1/ PAD[3]			SWDIO		CCL/ OUT[1]
I2C: Sm, Fm, Fm +, Hs		59	95	PB30	EIC/EXTINT[14]						SERCOM1/ PAD[0]	SERCOM5/ PAD[0]	TCC/ WO[0]				
		60	96	PB31	EIC/EXTINT[15]						SERCOM1/ PAD[1]	SERCOM5/ PAD[1]	TCC/ WO[1]				
Battery backup		61	97	PB00	EIC/EXTINT[0]		ADC/ AIN[8]				SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]		RTC/IN[0]	SUPC/ PSOK	CCL/IN[1]
		62	98	PB01	EIC/EXTINT[1]		ADC/ AIN[9]				SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	RTC/IN[2]	RTC/OUT	SUPC/ OUT[0]	CCL/IN[2]
	47	63	99	PB02	EIC/EXTINT[2]		ADC/ AIN[10]				SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC/2/ WO[0]		RTC/IN[1]	SUPC/ OUT[1]	CCL/ OUT[0]
	48	64	100	PB03	EIC/EXTINT[3]		ADC/ AIN[11]				SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC/2/ WO[1]			SUPC/ VBAT	

Note:

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for supported I^2C modes.
   - Sm: Standard mode, up to 100kHz
   - Fm: Fast mode, up to 400kHz
   - Fm+: Fast mode Plus, up to 1MHz
   - Hs: High-speed mode, up to 3.4MHz
3. These pins are High Sink pins and have different properties than regular pins: PA12, PA13, PA22, PA23, PA27, PA31, PB30, PB31.
4. Clusters of multiple GPIO pins are sharing the same supply pin.
5. The 49th pin of the WLCSP49 package is an additional GND pin.
6. SAM L22N: SERCOM[0:5]. SAM L22G, L22J: SERCOM[0:3].

Related Links

Configuration Summary on page 7
SERCOM USART and I2C Configurations on page 23

7.2. Other Functions

7.2.1. Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing is controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PB22
		XOUT	PB23
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Table 7-3. XOSC32K Jitter Minimization

Package	Steady Signal Recommended
L22N	PB00, PB01, PB02, PB03, PC00, PC01
L22J	PB00, PB01, PB02, PB03, PA02, PA03
L22G	PB02, PB03, PA02, PA03

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

7.2.3. SERCOM USART and I²C Configurations

The SAM L22 has up to six instances of the serial communication interface (SERCOM) peripheral. The following table lists the supported communication protocols for each SERCOM instance.

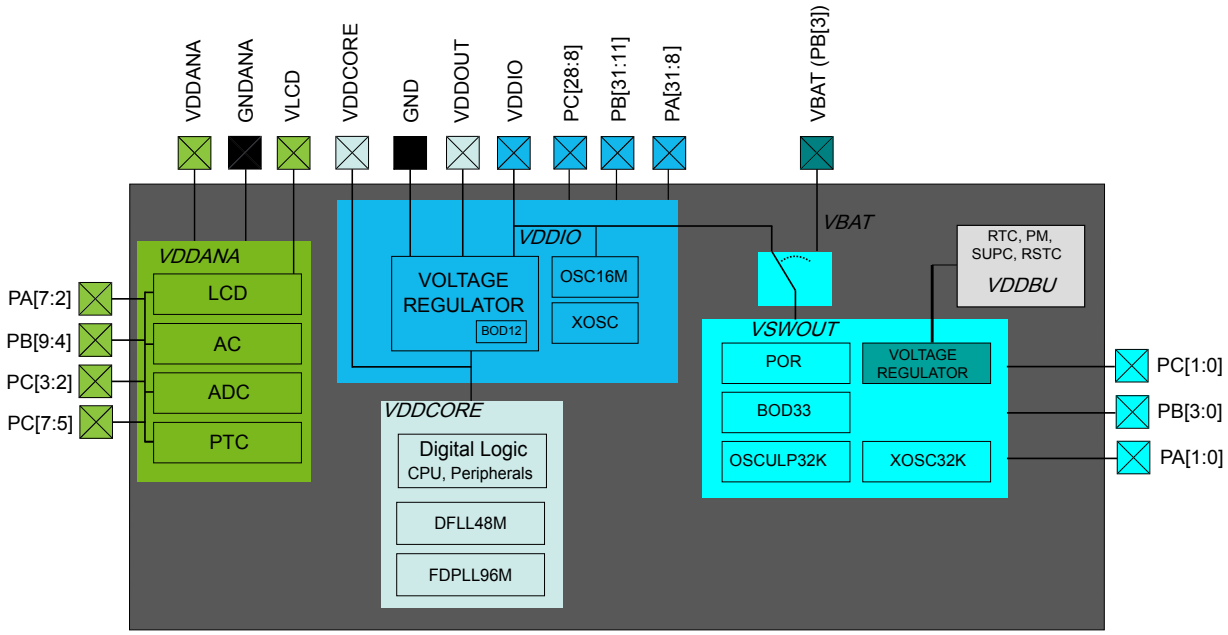
Table 7-5. SERCOM USART and I²C Protocols

	SERCOM Instance					
Protocol	SERCOM0	SERCOM1	SERCOM2	SERCOM3	SERCOM4	SERCOM5
I²C	no	yes	yes	yes	yes	yes
I²C at 3.4MHz	no	yes	no	no	no	yes
USART including RS485 and ISO 7816	yes	yes	yes	yes	yes	yes
SPI	yes	yes	yes	yes	yes	yes

Note: Not all available I²C pins support I²C mode at 3.4MHz.

8. Power Supply and Start-Up Considerations

8.1. Power Domain Overview



The Atmel SAM L22 power domains are not independent of each other:

- VDDCORE and VDDIO share GND, whereas VDDANA refers to GNDANA.
- VDDCORE serves as the internal voltage regulator output.
- VSWOUT and VDDBU are internal power domains.

8.2. Power Supply Considerations

8.2.1. Power Supplies

The Atmel SAM L22 has several different power supply pins:

- VDDIO powers I/O lines and OSC16M, XOSC, the internal regulator for VDDCORE and the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDANA powers I/O lines and the ADC, AC, LCD, and PTC. Voltage is 1.62V to 3.63V
- VLCD has two alternative functions:
  - Output of the LCD voltage pump when VLCD is generated internally. Output voltage is 2.5V to 3.5V.
  - Supply input for the bias generator when VLCD is provided externally by the application. Input voltage is 2.4 to 3.6V.
- VBAT powers the Automatic Power Switch. Voltage is 1.62V to 3.63V
- VDDCORE serves as the internal voltage regulator output. It powers the core, memories, peripherals, DFLL48M and FDPLL96M. Voltage is 0.9V to 1.2V typical.
- The Automatic Power Switch is a configurable switch that selects between VDDIO and VBAT as supply for the internal output VSWOUT, see the figure in Power Domain Overview.

The same voltage must be applied to both VDDIO and VDDANA. This common voltage is referred to as VDD in the datasheet.

The ground pins, GND, are common to VDDCORE, and VDDIO. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

8.2.2. Voltage Regulator

The SAM L22 internal Voltage Regulator has four different modes:

- Linear mode : This is the default mode when CPU and peripherals are running. It does not require an external inductor.
- Switching mode. This is the most efficient mode when the CPU and peripherals are running. This mode can be selected by software on the fly.
- Low Power (LP) mode. This is the default mode used when the chip is in standby mode.
- Shutdown mode. When the chip is in backup mode, the internal regulator is off.

Note that the Voltage Regulator modes are controlled by the Power Manager.

8.2.3. Typical Powering Schematic

The SAM L22 uses a single supply from 1.62V to 3.63V.

The following figure shows the recommended power supply connection.

Figure 8-1. Power Supply Connection for Linear Mode Only

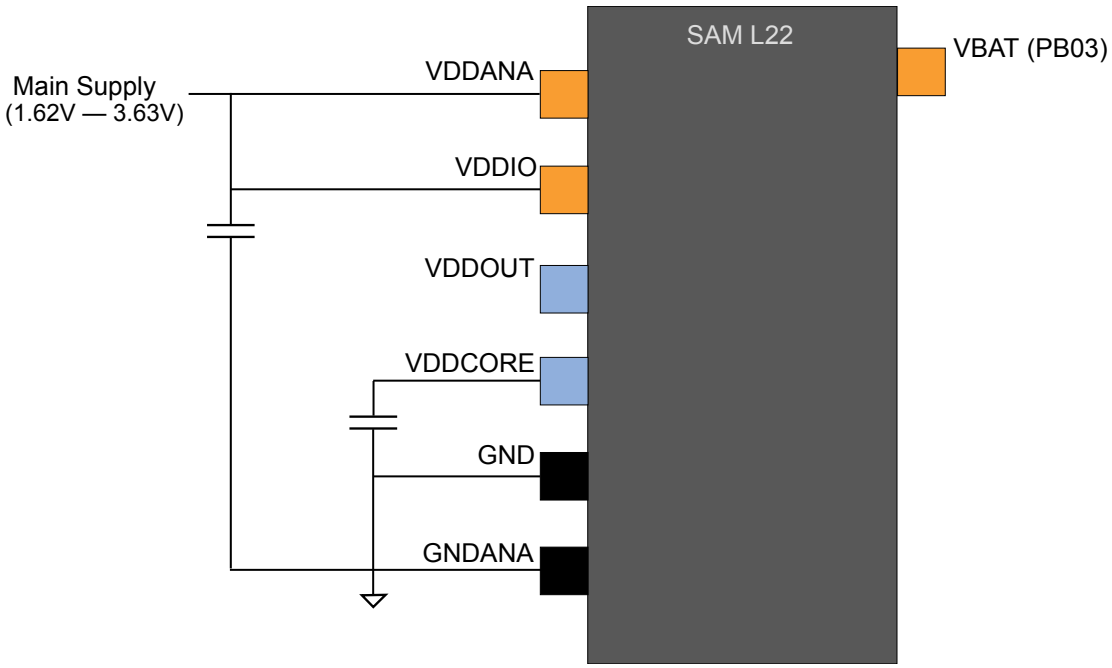


Figure 8-2. Power Supply Connection for Switching/Linear Mode

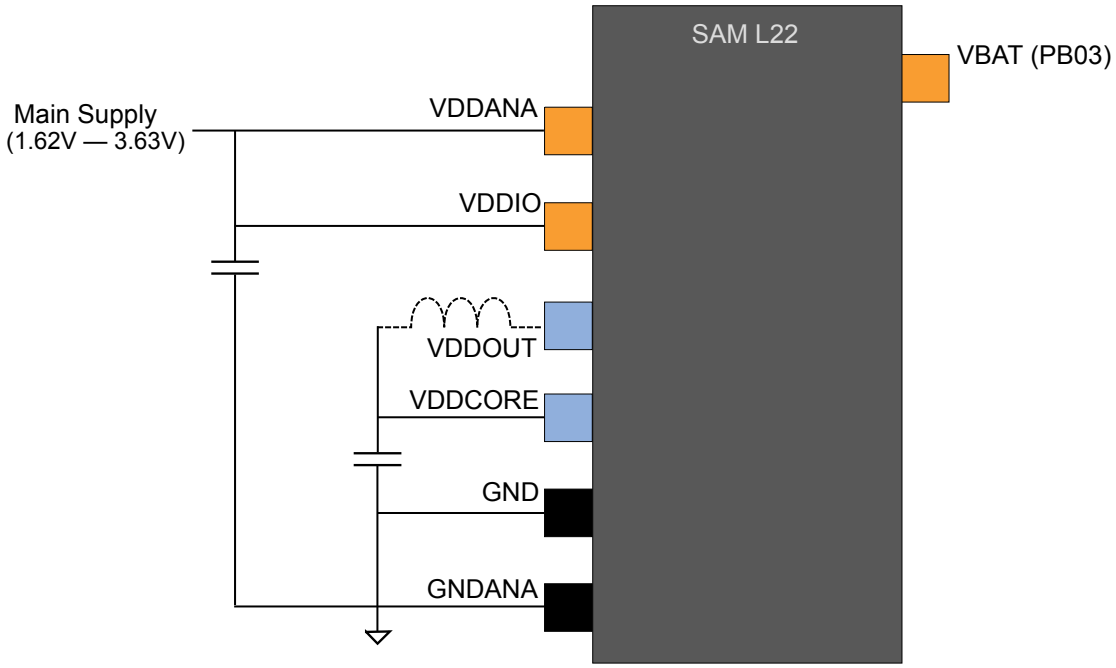
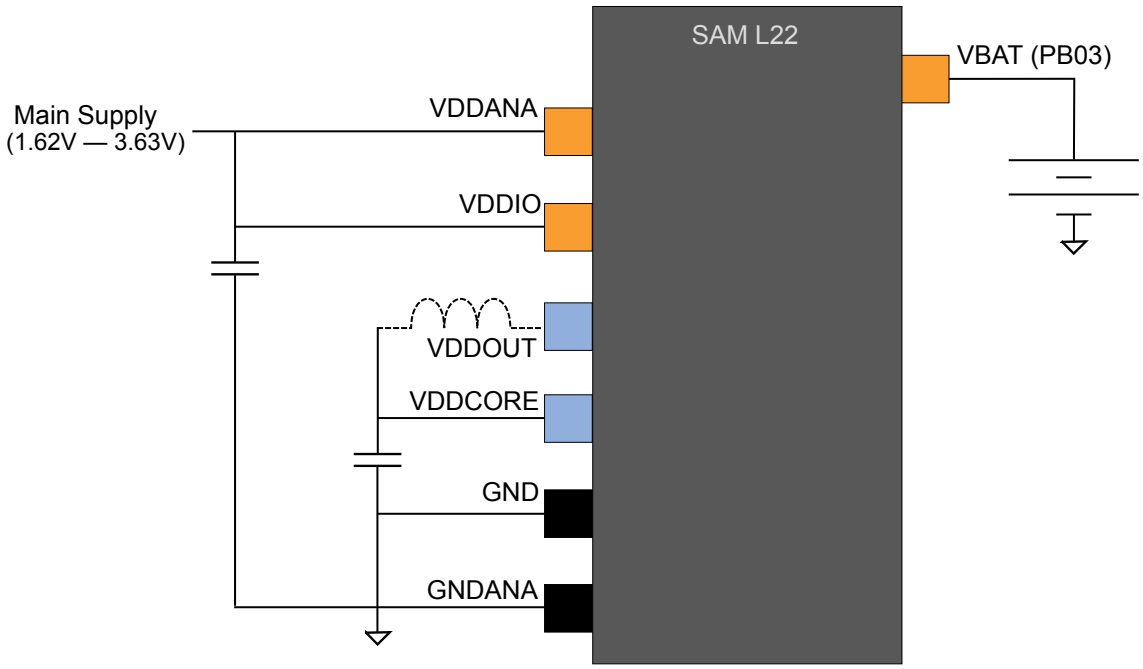


Figure 8-3. Power Supply Connection for Battery Backup



8.2.4. Power-Up Sequence

8.2.4.1. Supply Order

VDDIO and VDDANA must have the same supply sequence. Ideally, they must be connected together.

8.2.4.2. Minimum Rise Rate

One integrated power-on reset (POR) circuits monitoring VDDIO requires a minimum rise rate.

8.2.4.3. Maximum Rise Rate

The rise rate of the power supplies must not exceed the values described in Electrical Characteristics.

10.3. NVM User Row Mapping

The Non Volatile Memory (NVM) User Row contains calibration data that are automatically read at device power-on.

The NVM User Row can be read at address 0x00804000.

To write the NVM User Row refer to the documentation of the NVMCTRL - Non-Volatile Memory Controller.

Note: When writing to the User Row, the new values do not get loaded by the other peripherals on the device until a device Reset occurs.

Table 10-4. NVM User Row Mapping

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	0x7	NVMCTRL
3	Reserved	—	0x1	—
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	0x7	NVMCTRL
7	Reserved	—	0x1	—
13:8	BOD33 Level	BOD33 threshold level at power-on.	0x06	SUPC.BOD33
14	BOD33 Disable	BOD33 Disable at power-on.	0x0	SUPC.BOD33
16:15	BOD33 Action	BOD33 Action at power-on.	0x1	SUPC.BOD33
25:17	Reserved	Factory settings - do not change.	0x08F	-
26	WDT Enable	WDT Enable at power-on.	0x0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power-on.	0x0	WDT.CTRLA
31:28	WDT Period	WDT Period at power-on.	0xB	WDT.CONFIG
35:32	WDT Window	WDT Window mode time-out at power-on.	0xB	WDT.CONFIG
39:36	WDT EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on.	0xB	WDT.EWCTRL
40	WDT WEN	WDT Timer Window Mode Enable at power-on.	0x0	WDT.CTRLA
41	BOD33 Hysteresis	BOD33 Hysteresis configuration at power-on.	0x0	SUPC.BOD33
47:42	Reserved	Factory settings - do not change.	0x3E	—
63:48	LOCK	NVM Region Lock Bits.	0xFFFF	NVMCTRL

10.4. NVM Software Calibration Area Mapping

The NVM Software Calibration Area contains calibration data that are determined and written during production test. These calibration values should be read by the application software and written back to the corresponding register.

The NVM Software Calibration Area can be read at address 0x00806020.

The NVM Software Calibration Area can not be written.

Table 10-5. NVM Software Calibration Area Mapping

Bit Position	Name	Description
2:0	ADC LINEARITY	ADC Linearity Calibration. Should be written to CALIB register.
5:3	ADC BIASCAL	ADC Bias Calibration. Should be written to CALIB register.
12:6	Reserved	Reserved for future use.
17:13	USB TRANSN	USB TRANSN calibration value. Should be written to the USB PADCAL register.
22:18	USB TRANSP	USB TRANSP calibration value. Should be written to the USB PADCAL register.
25:23	USB TRIM	USB TRIM calibration value. Should be written to the USB PADCAL register.
31:26	DFLL48M COARSE CAL	DFLL48M Coarse calibration value. Should be written to the OSCCTRL DFLLVAL register.

10.5. Serial Number

Each device has a unique 128-bit serial number which is a concatenation of four 32-bit words contained at the following addresses:

Word 0: 0x0080A00C

Word 1: 0x0080A040

Word 2: 0x0080A044

Word 3: 0x0080A048

The uniqueness of the serial number is guaranteed only when using all 128 bits.

11. Processor and Architecture

11.1. Cortex M0+ Processor

The Atmel SAM L22 implements the ARM ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

11.1.1. Cortex M0+ Configuration

Table 11-1. Cortex M0+ Configuration

Features	Cortex-M0+ options	SAM L22 configuration
Interrupts	External interrupts 0-32	27
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

11.1.2. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

arriving interrupts. Refer to NVIC-Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).

Note: When the CPU frequency is much higher than the APB frequency it is recommended to insert a memory read barrier after each CPU write to registers mapped on the APB. Failing to do so in such conditions may lead to unexpected behavior such as e.g. re-entering a peripheral interrupt handler just after leaving it.

- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section MTB-Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (http://www.arm.com).
- Memory Protection Unit (MPU)
  - The Memory Protection Unit divides the memory map into a number of regions, and defines the location, size, access permissions and memory attributes of each region. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com)

11.1.3. Cortex M0+ Address Map

Table 11-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000	Micro Trace Buffer (MTB)

Related Links

Product Mapping on page 30

11.1.4. I/O Interface

The device allows direct access to PORT registers. Accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, so the Cortex M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O access to be sustained for as long as necessary.

Peripheral source	NVIC line
EVSYS – Event System	8
SERCOM0 – Serial Communication Interface 0	9
SERCOM1 – Serial Communication Interface 1	10
SERCOM2 – Serial Communication Interface 2	11
SERCOM3 – Serial Communication Interface 3	12
SERCOM4 – Serial Communication Interface 4	13
SERCOM5 – Serial Communication Interface 5	14
TCC0 – Timer Counter for Control 0	15
TC0 – Timer Counter 0	16
TC1 – Timer Counter 1	17
TC2 – Timer Counter 2	18
TC3 – Timer Counter 3	19
ADC – Analog-to-Digital Converter	20
AC – Analog Comparator	21
PTC – Peripheral Touch Controller	22
SLCD - Segmented LCD Controller	23
AES - Advanced Encryption Standard module	24
TRNG - True Random Number Generator	25

11.3. Micro Trace Buffer

11.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

11.3.2. Overview

When enabled, the MTB records the changes in program flow that are reported by the Cortex-M0+ processor over the execution trace interface. This interface is shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. The information is stored by the MTB in the SRAM as trace packets. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB stores trace information into the SRAM and gives the processor access to the SRAM simultaneously. The MTB ensures that trace write accesses have priority over processor accesses.

An execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects a non-sequential change of the program pounter (PC) value. A non-sequential PC change can occur during

11.4.3. Configuration

Figure 11-1. Master-Slave Relations High-Speed Bus Matrix

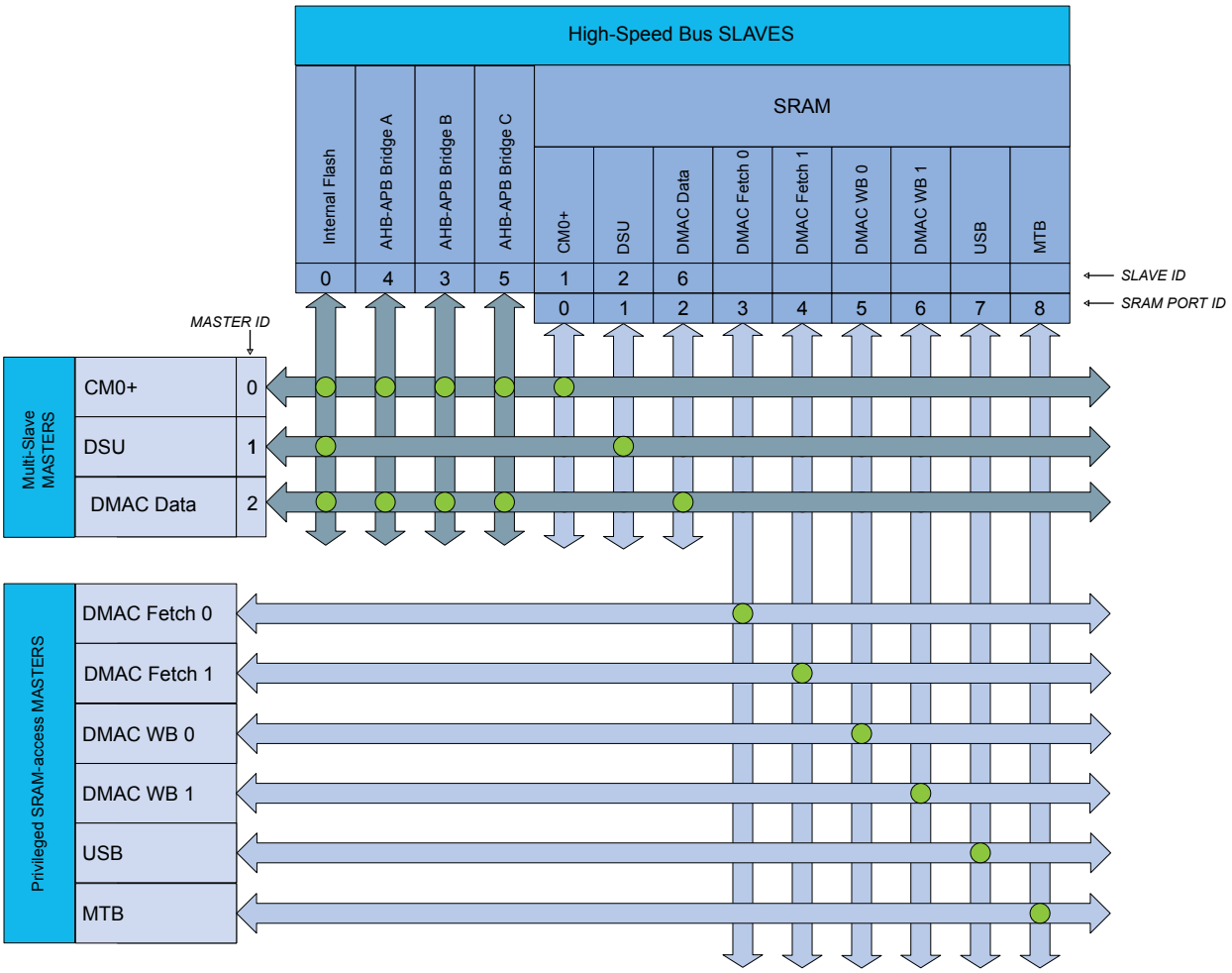


Table 11-4. High Speed Bus Matrix Masters

High-Speed Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1
DMAC - Direct Memory Access Controller / Data Access	2

Table 11-5. High-Speed Bus Matrix Slaves

High-Speed Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
SRAM Port 0 - CM0+ Access	1
SRAM Port 1 - DSU Access	2
AHB-APB Bridge B	3
AHB-APB Bridge A	4

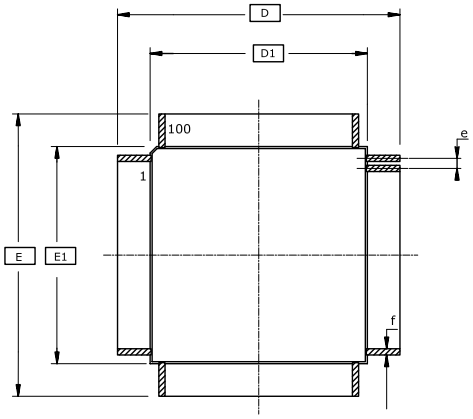
SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
USB - Universal Serial Bus	7	Direct	IP-QOSCTRL	0x3
MTB - Micro Trace Buffer	8	Direct	STATIC-3	0x3

Note: 1. Using 32-bit access only.

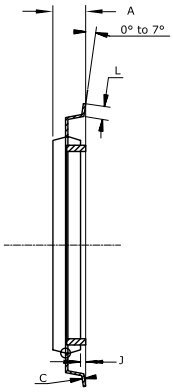
12.2. Package Drawings

12.2.1. 100 pin TQFP

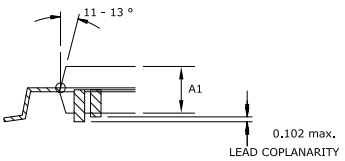
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



DETAIL VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		16.00		
D1/E1		14.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		100		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

Table 12-2. Device and Package Maximum Weight

520	mg

Table 12-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-4. Package Reference

JEDEC Drawing Reference	MS-026, variant AED
JESD97 Classification	e3