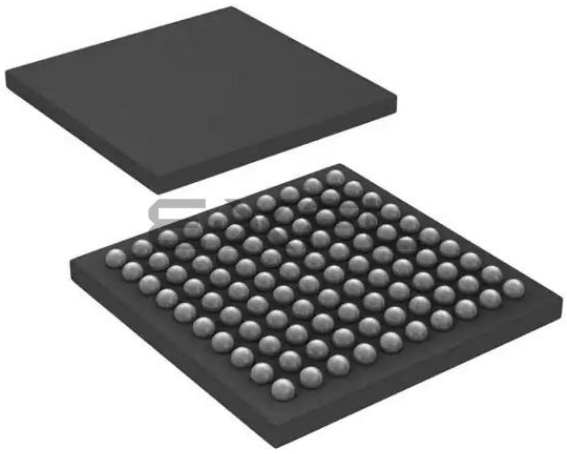

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22n17a-cfut

- Battery backup support
- Two runtime selectable power/performance levels
- Embedded Buck/LDO regulator supporting on-the-fly selection
- Active mode: <50µA/MHz
- Standby with full retention, RTC and LCD = 3.47µA
  - 2.1µs wake-up time
- Standby with full retention and RTC: 1.87µA
  - 2.1µs wake-up time
- Ultra low power Backup mode with RTC: 490nA
  - 90µs wake-up time

- Peripherals
  - Segment LCD controller
    - Up to 8 (4) common and 40 (44) segment terminals to drive 320 (176) segments
    - Static, ½, 1/3, ¼ bias
    - Internal charge pump able to generate VLCD higher than VDDIO
  - 16-channel Direct Memory Access Controller (DMAC)
  - 8-channel Event System
  - Up to four 16-bit Timer/Counters (TC), each configurable as:
    - 16-bit TC with two compare/capture channels
    - 8-bit TC with two compare/capture channels
    - 32-bit TC with two compare/capture channels, by using two TCs
  - One 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - Frequency Meter
  - 32-bit Real Time Counter (RTC) with clock/calendar function
    - 8x32-bit Backup Register
    - Tamper Detection
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 Device
    - Eight endpoints
    - Crystal less operation
  - Up to six Serial Communication Interfaces (SERCOM), each configurable as:
    - USART with full-duplex and single-wire half-duplex configuration
    - ISO7816
    - I^2C up to 3.4MHz[1]
    - SPI
  - One AES encryption engine

[1] Max 1 high-speed mode and max 3 fast mode I^2C

Table of Contents

	SAM L22N	SAM L22J	SAM L22G
Wake-up Pins with debouncing	5	3	2
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values	One 32-bit value or two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) channels (X- x Y-lines) for mutual capacitance[3]	256 (16x16)	182 (13x14)	132 (11x12)
Peripheral Touch Controller (PTC) channels for self capacitance (Y-lines only)[4]	24	19	15
Maximum CPU frequency	32MHz	32MHz	32MHz
Packages	TQFP	QFN TQFP	QFN TQFP WLCSP
Oscillators			
Event System channels	8	8	8
SW Debug Interface	Yes	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes	Yes

Note:

1. L22J, L22G: All SLCD Pins can be configured also as GPIOs. L22N: 44 SLCD Pins can be configured as GPIOs, 8 SLCD Pins can be used as GP input.
2. SAM L22N: SERCOM[5:0]. L22G, L22J: SERCOM[3:0].
3. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines.
4. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML22J18A-MUT			QFN64	

3.3. SAM L22G

Table 3-3. SAM L22G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML22G16A-MUT			QFN48	
ATSAML22G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML22G17A-MUT			QFN48	
ATSAML22G17A-UUT			WLCSP49	
ATSAML22G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML22G18A-MUT			QFN48	
ATSAML22G18A-UUT			WLCSP49	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

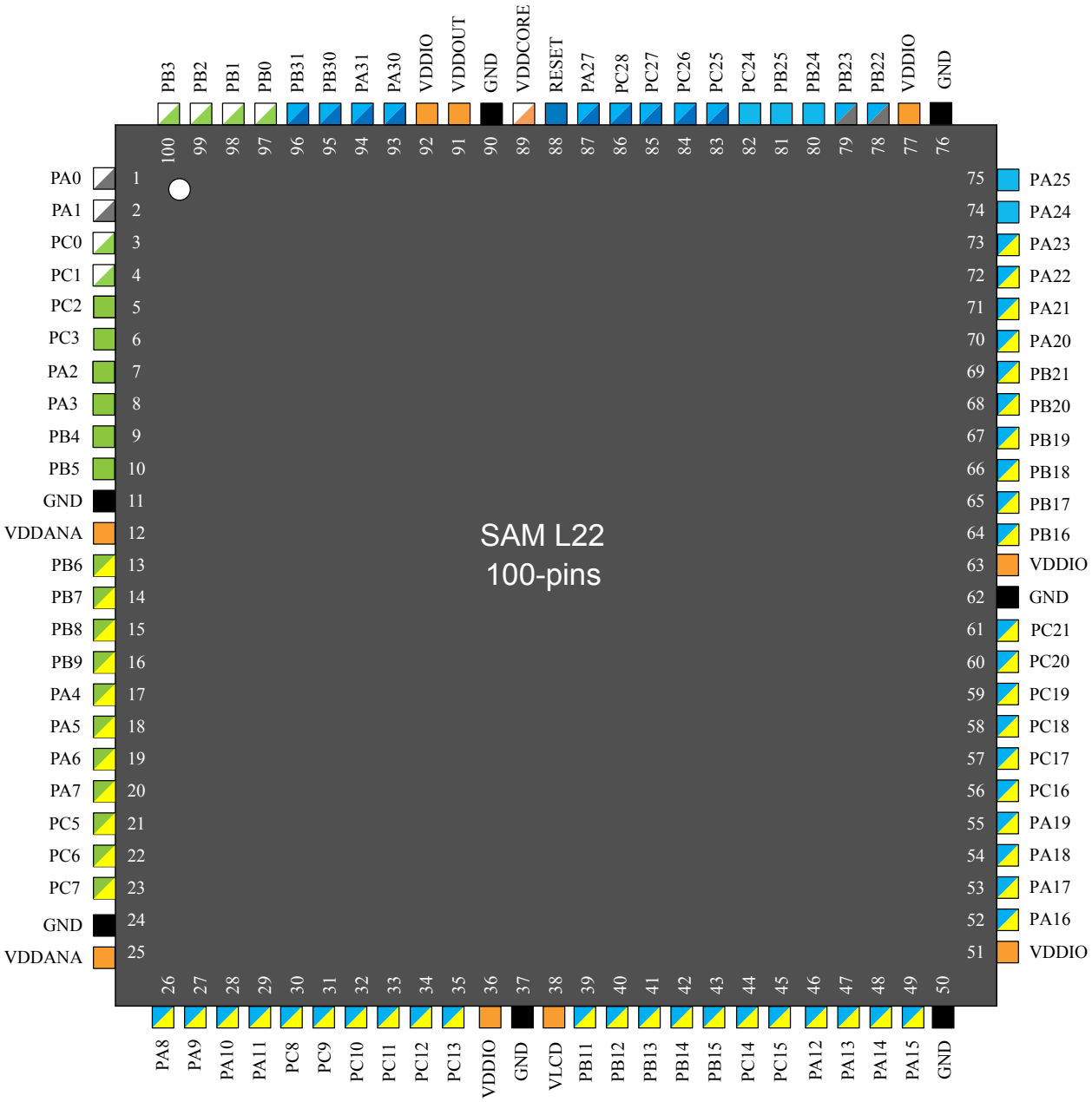
Table 3-4. SAM L22 Device Identification Values

DSU DID.DEVSEL	Device
0x0	L22N18
0x1	L22N17
0x2	L22N16
0x3-0x4	Reserved
0x5	L22J18
0x6	L22J17
0x7	L22J16
0x8-0x9	Reserved
0xA	L22G18
0xB	L22G17
0xC	L22G16
0xD-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

1. Some device configurations have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. The number of PTC X and Y signals is configurable.

5.3. SAM L22N


SAM L22
100-pins
PB3 100
PB2 99
PB1 98
PB0 97
PB31 96
PB30 95
PA31 94
PA30 93
VDDIO 92
VDDOUT 91
GND 90
VDDCORE 89
RESET 88
PA27 87
PC28 86
PC27 85
PC26 84
PC25 83
PC24 82
PB25 81
PB24 80
PB23 79
PB22 78
VDDIO 77
GND 76
PA0 1
PA1 2
PC0 3
PC1 4
PC2 5
PC3 6
PA2 7
PA3 8
PB4 9
PB5 10
GND 11
VDDANA 12
PB6 13
PB7 14
PB8 15
PB9 16
PA4 17
PA5 18
PA6 19
PA7 20
PC5 21
PC6 22
PC7 23
GND 24
VDDANA 25
75 PA25
74 PA24
73 PA23
72 PA22
71 PA21
70 PA20
69 PB21
68 PB20
67 PB19
66 PB18
65 PB17
64 PB16
63 VDDIO
62 GND
61 PC21
60 PC20
59 PC19
58 PC18
57 PC17
56 PC16
55 PA19
54 PA18
53 PA17
52 PA16
51 VDDIO
26 PA8
27 PA9
28 PA10
29 PA11
30 PC8
31 PC9
32 PC10
33 PC11
34 PC12
35 PC13
36 VDDIO
37 GND
38 VLCD
39 PB11
40 PB12
41 PB13
42 PB14
43 PB15
44 PC14
45 PC15
46 PA12
47 PA13
48 PA14
49 PA15
50 GND

Signal Name	Function	Type	Active Level
SOF 1kHz	USB Start of Frame	Digital	
Real Timer Clock - RTC			
RTC_IN[4:0]	Tamper or external wake-up pins	Digital	
RTC_OUT	Tamper output	Digital	

7. I/O Multiplexing and Considerations

7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned a different peripheral functions. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral function A to I is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) of the PORT.

This table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 7-1. PORT Function Multiplexing

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
Battery backup	1	1	1	PA00	EIC/EXTINT[0]							SERCOM1/ PAD[0]					
	2	2	2	PA01	EIC/EXTINT[1]							SERCOM1/ PAD[1]					
			3	PC00	EIC/EXTINT[8]		ADC/ AIN[16]								RTC/IN[3]		
			4	PC01	EIC/EXTINT[9]		ADC/ AIN[17]								RTC/IN[4]		
			5	PC02	EIC/EXTINT[10]		ADC/ AIN[18]		PTC/ XY[6]								
			6	PC03	EIC/EXTINT[11]		ADC/ AIN[19]		PTC/ XY[7]								
	3	3	7	PA02	EIC/EXTINT[2]	ADC/ VREFB	ADC/ AIN[0]	AC/ AIN[0]	PTC/ XY[8]						RTC/IN[2]		
	4	4	8	PA03	EIC/EXTINT[3]	ADC/ VREFA	ADC/ AIN[1]	AC/ AIN[1]	PTC/ XY[9]								
		5	9	PB04	EIC/EXTINT[4]		ADC/ AIN[12]	AC/ AIN[2]	PTC/ XY[10]								
		6	10	PB05	EIC/EXTINT[5]		ADC/ AIN[13]	AC/ AIN[3]	PTC/ XY[11]								
		9	13	PB06	EIC/EXTINT[6]		ADC/ AIN[14]		PTC/ XY[12]	SLCD/ LP[0]							CCL/IN[6]
		10	14	PB07	EIC/EXTINT[7]		ADC/ AIN[15]		PTC/ XY[13]	SLCD/ LP[1]							CCL/IN[7]
	7	11	15	PB08	EIC/EXTINT[8]		ADC/ AIN[2]		PTC/ XY[14]	SLCD/ LP[2]		SERCOM3/ PAD[0]	TC/0/ WO[0]				CCL/IN[8]
	8	12	16	PB09	EIC/EXTINT[9]		ADC/ AIN[3]		PTC/ XY[15]	SLCD/ LP[3]		SERCOM3/ PAD[1]	TC/0/ WO[1]				CCL/ OUT[2]
	9	13	17	PA04	EIC/EXTINT[4]		ADC/ AIN[4]		PTC/ X[24]	SLCD/ LP[4]		SERCOM0/ PAD[0]	TCC/ WO[0]				CCL/IN[0]
	10	14	18	PA05	EIC/EXTINT[5]		ADC/ AIN[5]		PTC/ X[25]	SLCD/ LP[5]		SERCOM0/ PAD[1]	TCC/ WO[1]				CCL/IN[1]
	11	15	19	PA06	EIC/EXTINT[6]		ADC/ AIN[6]		PTC/ X[26]	SLCD/ LP[6]		SERCOM0/ PAD[2]					CCL/IN[2]
	12	16	20	PA07	EIC/EXTINT[7]		ADC/ AIN[7]		PTC/ X[27]	SLCD/ LP[7]		SERCOM0/ PAD[3]					CCL/ OUT[0]
			21	PC05	EIC/EXTINT[13]				PTC/ XY[4]	SLCD/ LP[8]							
			22	PC06	EIC/EXTINT[14]				PTC/ XY[5]	SLCD/ LP[9]							
			23	PC07	EIC/EXTINT[15]					SLCD/ LP[10]							
	13	17	26	PA08	EIC/NMI				PTC/ XY[3]	SLCD/ LP[11]	SERCOM0/ PAD[0]	SERCOM4/ PAD[0]	TCC/ WO[0]				CCL/IN[3]
	14	18	27	PA09	EIC/EXTINT[9]				PTC/ XY[2]	SLCD/ LP[12]	SERCOM0/ PAD[1]	SERCOM4/ PAD[1]	TCC/ WO[1]				CCL/IN[4]
	15	19	28	PA10	EIC/EXTINT[10]				PTC/ XY[1]	SLCD/ LP[13]	SERCOM0/ PAD[2]	SERCOM4/ PAD[2]		TCC/ WO[2]		GCLK/ IO[4]	CCL/IN[5]
	16	20	29	PA11	EIC/EXTINT[11]				PTC/ XY[0]	SLCD/ LP[14]	SERCOM0/ PAD[3]	SERCOM4/ PAD[3]		TCC/ WO[3]			CCL/ OUT[1]

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
	38	50	79	PB23	EIC/EXTINT[7]						SERCOM0/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	TCC/ WO[3]		GCLK/ IO[1]	CCL/ OUT[0]
			80	PB24	EIC/EXTINT[8]						SERCOM0/ PAD[0]	SERCOM4/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
			81	PB25	EIC/EXTINT[9]						SERCOM0/ PAD[1]	SERCOM4/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
			82	PC24	EIC/EXTINT[0]						SERCOM0/ PAD[2]	SERCOM4/ PAD[2]	TC/2/ WO[0]	TCC/ WO[0]			
			83	PC25	EIC/EXTINT[1]						SERCOM0/ PAD[3]	SERCOM4/ PAD[3]	TC/2/ WO[1]	TCC/ WO[1]			
			84	PC26	EIC/EXTINT[2]								TC/3/ WO[0]	TCC/ WO[2]			
			85	PC27	EIC/EXTINT[3]							SERCOM1/ PAD[0]	TC/3/ WO[1]	TCC/ WO[3]			CCL/IN[4]
			86	PC28	EIC/EXTINT[4]				PTC/ XY[20]			SERCOM1/ PAD[1]		TCC/ WO[4]			CCL/IN[5]
recommended for GCLK IO	39	51	87	PA27	EIC/EXTINT[15]				PTC/ XY[21]					TCC/ WO[5]	TAL/BRK	GCLK/ IO[0]	
	40	52	88	RESET_N													
	45	57	93	PA30	EIC/EXTINT[10]				PTC/ XY[22]			SERCOM1/ PAD[2]			CORTEX_M0P/ SWCLK	GCLK/ IO[0]	CCL/IN[3]
	46	58	94	PA31	EIC/EXTINT[11]				PTC/ XY[23]			SERCOM1/ PAD[3]			SWDIO		CCL/ OUT[1]
I2C: Sm, Fm, Fm +, Hs		59	95	PB30	EIC/EXTINT[14]						SERCOM1/ PAD[0]	SERCOM5/ PAD[0]	TCC/ WO[0]				
		60	96	PB31	EIC/EXTINT[15]						SERCOM1/ PAD[1]	SERCOM5/ PAD[1]	TCC/ WO[1]				
Battery backup		61	97	PB00	EIC/EXTINT[0]		ADC/ AIN[8]				SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]		RTC/IN[0]	SUPC/ PSOK	CCL/IN[1]
		62	98	PB01	EIC/EXTINT[1]		ADC/ AIN[9]				SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	RTC/IN[2]	RTC/OUT	SUPC/ OUT[0]	CCL/IN[2]
	47	63	99	PB02	EIC/EXTINT[2]		ADC/ AIN[10]				SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC/2/ WO[0]		RTC/IN[1]	SUPC/ OUT[1]	CCL/ OUT[0]
	48	64	100	PB03	EIC/EXTINT[3]		ADC/ AIN[11]				SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC/2/ WO[1]			SUPC/ VBAT	

Note:

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for supported I^2C modes.
   - Sm: Standard mode, up to 100kHz
   - Fm: Fast mode, up to 400kHz
   - Fm+: Fast mode Plus, up to 1MHz
   - Hs: High-speed mode, up to 3.4MHz
3. These pins are High Sink pins and have different properties than regular pins: PA12, PA13, PA22, PA23, PA27, PA31, PB30, PB31.
4. Clusters of multiple GPIO pins are sharing the same supply pin.
5. The 49th pin of the WLCSP49 package is an additional GND pin.
6. SAM L22N: SERCOM[0:5]. SAM L22G, L22J: SERCOM[0:3].

Related Links

Configuration Summary on page 7
SERCOM USART and I2C Configurations on page 23

7.2. Other Functions

7.2.1. Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing is controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PB22
		XOUT	PB23
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Table 7-3. XOSC32K Jitter Minimization

Package	Steady Signal Recommended
L22N	PB00, PB01, PB02, PB03, PC00, PC01
L22J	PB00, PB01, PB02, PB03, PA02, PA03
L22G	PB02, PB03, PA02, PA03

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

7.2.3. SERCOM USART and I²C Configurations

The SAM L22 has up to six instances of the serial communication interface (SERCOM) peripheral. The following table lists the supported communication protocols for each SERCOM instance.

Table 7-5. SERCOM USART and I²C Protocols

	SERCOM Instance					
Protocol	SERCOM0	SERCOM1	SERCOM2	SERCOM3	SERCOM4	SERCOM5
I²C	no	yes	yes	yes	yes	yes
I²C at 3.4MHz	no	yes	no	no	no	yes
USART including RS485 and ISO 7816	yes	yes	yes	yes	yes	yes
SPI	yes	yes	yes	yes	yes	yes

Note: Not all available I²C pins support I²C mode at 3.4MHz.

The same voltage must be applied to both VDDIO and VDDANA. This common voltage is referred to as VDD in the datasheet.

The ground pins, GND, are common to VDDCORE, and VDDIO. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic checklist.

8.2.2. Voltage Regulator

The SAM L22 internal Voltage Regulator has four different modes:

- Linear mode : This is the default mode when CPU and peripherals are running. It does not require an external inductor.
- Switching mode. This is the most efficient mode when the CPU and peripherals are running. This mode can be selected by software on the fly.
- Low Power (LP) mode. This is the default mode used when the chip is in standby mode.
- Shutdown mode. When the chip is in backup mode, the internal regulator is off.

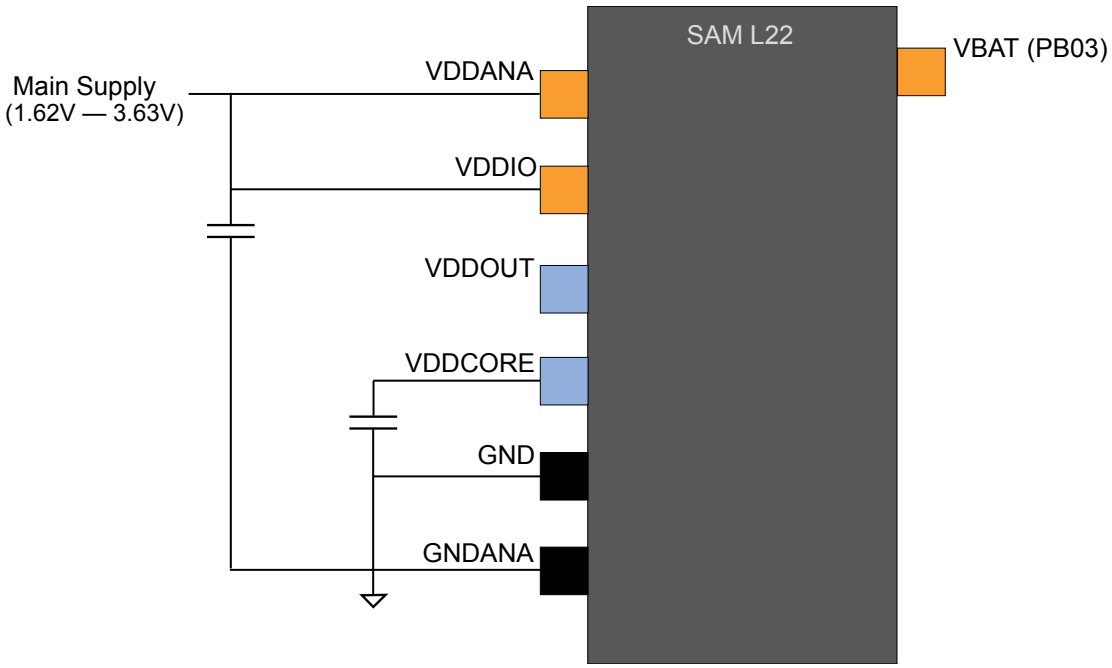
Note that the Voltage Regulator modes are controlled by the Power Manager.

8.2.3. Typical Powering Schematic

The SAM L22 uses a single supply from 1.62V to 3.63V.

The following figure shows the recommended power supply connection.

Figure 8-1. Power Supply Connection for Linear Mode Only



8.3. Power-Up

This section summarizes the power-up sequence of the SAM L22. The behavior after power-up is controlled by the Power Manager.

8.3.1. Starting of Internal Regulator

After power-up, the device is set to its initial state and kept in Reset, until the power has stabilized throughout the device. The default performance level after power-up is PL0.

The internal regulator provides the internal VDDCORE corresponding to this performance level. Once the external voltage VDDIO and the internal VDDCORE reach a stable value, the internal Reset is released.

8.3.2. Starting of Clocks

Once the power has stabilized and the internal Reset is released, the device will use a 4MHz clock by default. The clock source for this clock signal is OSC16M, which is enabled and configured at 4MHz after a reset by default. This is also the default time base for Generic Clock Generator 0. In turn, Generator 0 provides the main clock GCLK_MAIN which is used by the Power Manager (PM).

Some synchronous system clocks are active after Start-Up, allowing software execution. Refer to the “Clock Mask Register” section in the PM-Power Manager documentation for the list of clocks that are running by default. Synchronous system clocks that are running receive the 4MHz clock from Generic Clock Generator 0. Other generic clocks are disabled.

8.3.3. I/O Pins

After power-up, the I/O pins are tri-stated except PA30, which is pull-up enabled and configured as input.

8.3.4. Fetching of Initial Instructions

After Reset has been released, the CPU starts fetching PC and SP values from the Reset address, 0x00000000. This points to the first executable address in the internal Flash memory. The code read from the internal Flash can be used to configure the clock system and clock sources. See the related peripheral documentation for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

8.4. Power-On Reset and Brown-Out Detector

The SAM L22 embeds three features to monitor, warn and/or reset the device:

- POR: Power-on Reset on VSWOUT and VDDIO
- BOD33: Brown-out detector on VSWOUT/VBAT
- Brown-out detector internal to the voltage regulator for VDDCORE. BOD12 is calibrated in production and its calibration parameters are stored in the NVM User Row. This data should not be changed if the User Row is written to in order to assure correct behavior.

8.4.1. Power-On Reset on VSWOUT

VSWOUT is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VSWOUT goes below the threshold voltage, the entire chip is reset.

8.4.2. Power-On Reset on VDDIO

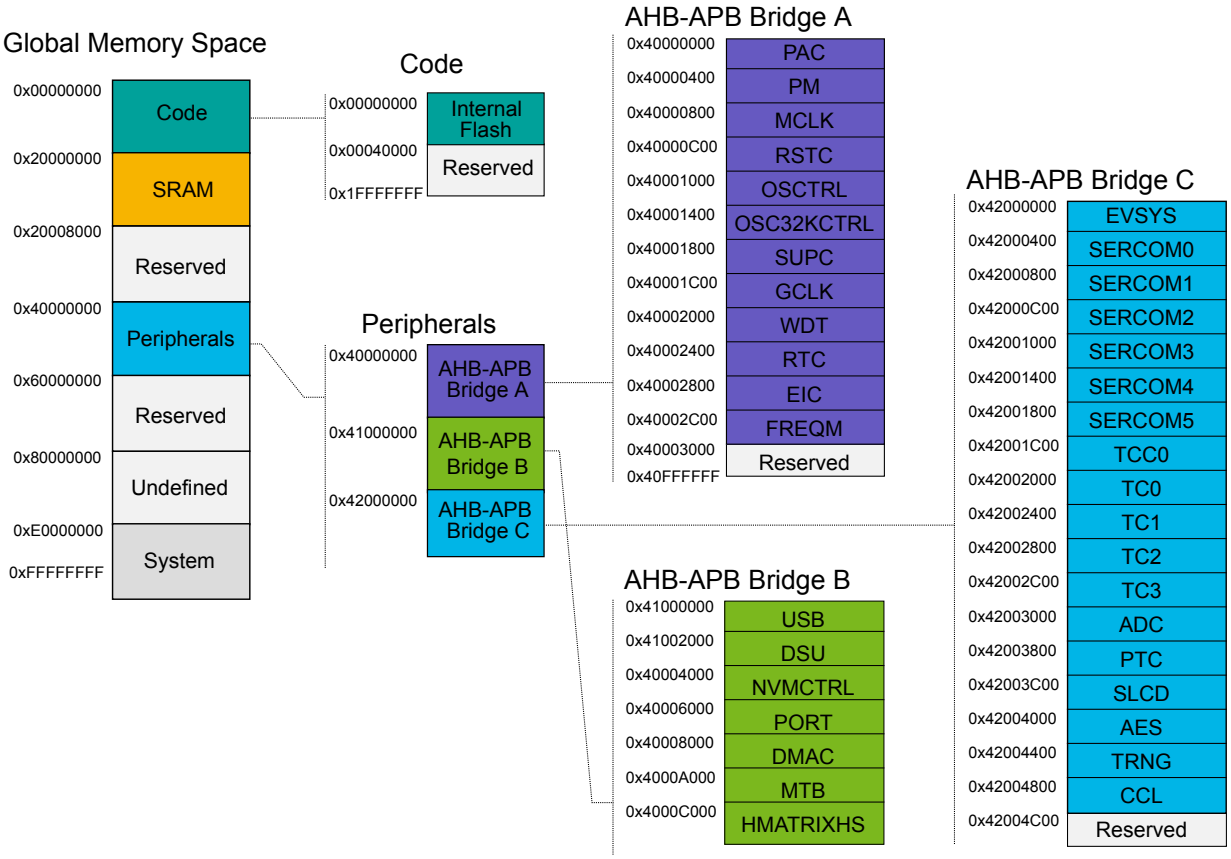
VDDIO is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VDDIO goes below the threshold voltage, all I/Os supplied by VDDIO are reset.

8.4.3. Brown-Out Detector on VSWOUT/VBAT

BOD33 monitors VSWOUT or VBAT depending on configuration.

9. Product Mapping

Figure 9-1. Atmel SAM L22 Product Mapping



10. Memories

10.1. Embedded Memories

- Internal high-speed Flash with Read-While-Write (RWW) capability on a section of the array
- Internal high-speed RAM, single-cycle access at full speed

10.2. Physical Memory Map

The high-speed bus is implemented as a bus matrix. All high-speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follows:

Table 10-1. SAM L22 Physical Memory Map

Memory	Start address	Size [KB]		
		SAML22x18(1)	SAML22x17(1)	SAML22x16(1)
Embedded Flash	0x00000000	256	128	64
Embedded RWW section	0x00400000	8	4	2
Embedded SRAM	0x20000000	32	16	8
Peripheral Bridge A	0x40000000	64	64	64
Peripheral Bridge B	0x41000000	64	64	64
Peripheral Bridge C	0x42000000	64	64	64
IOBUS	0x60000000	0.5	0.5	0.5

Note: 1. x = G, J, or E.

Table 10-2. Flash Memory Parameters

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	256	4096	64
SAML22x17(1)	128	2048	64
SAML22x16(1)	64	1024	64

Note: 1. x = G, J, or E.

Table 10-3. RWW Section Parameters(1)

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	8	128	64
SAML22x17(1)	4	64	64
SAML22x16(1)	2	32	64

Note: 1. x = G, J, or E.

10.3. NVM User Row Mapping

The Non Volatile Memory (NVM) User Row contains calibration data that are automatically read at device power-on.

The NVM User Row can be read at address 0x00804000.

To write the NVM User Row refer to the documentation of the NVMCTRL - Non-Volatile Memory Controller.

Note: When writing to the User Row, the new values do not get loaded by the other peripherals on the device until a device Reset occurs.

Table 10-4. NVM User Row Mapping

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	BOOTPROT	Used to select one of eight different bootloader sizes.	0x7	NVMCTRL
3	Reserved	—	0x1	—
6:4	EEPROM	Used to select one of eight different EEPROM sizes.	0x7	NVMCTRL
7	Reserved	—	0x1	—
13:8	BOD33 Level	BOD33 threshold level at power-on.	0x06	SUPC.BOD33
14	BOD33 Disable	BOD33 Disable at power-on.	0x0	SUPC.BOD33
16:15	BOD33 Action	BOD33 Action at power-on.	0x1	SUPC.BOD33
25:17	Reserved	Factory settings - do not change.	0x08F	-
26	WDT Enable	WDT Enable at power-on.	0x0	WDT.CTRLA
27	WDT Always-On	WDT Always-On at power-on.	0x0	WDT.CTRLA
31:28	WDT Period	WDT Period at power-on.	0xB	WDT.CONFIG
35:32	WDT Window	WDT Window mode time-out at power-on.	0xB	WDT.CONFIG
39:36	WDT EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on.	0xB	WDT.EWCTRL
40	WDT WEN	WDT Timer Window Mode Enable at power-on.	0x0	WDT.CTRLA
41	BOD33 Hysteresis	BOD33 Hysteresis configuration at power-on.	0x0	SUPC.BOD33
47:42	Reserved	Factory settings - do not change.	0x3E	—
63:48	LOCK	NVM Region Lock Bits.	0xFFFF	NVMCTRL

SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
USB - Universal Serial Bus	7	Direct	IP-QOSCTRL	0x3
MTB - Micro Trace Buffer	8	Direct	STATIC-3	0x3

Note: 1. Using 32-bit access only.

12. Packaging Information

12.1. Thermal Considerations

12.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

Table 12-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
48-pin TQFP	64.2°C/W	12.3°C/W
64-pin TQFP	60.8°C/W	12.0°C/W
100-pin TQFP	58.5°C/W	12.7°C/W
48-pin QFN	32.4°C/W	11.2°C/W
64-pin QFN	32.7°C/W	10.8°C/W
49-pin WLCSP	37.3°C/W	5.8°C/W

Related Links

Junction Temperature on page 42

12.1.2. Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

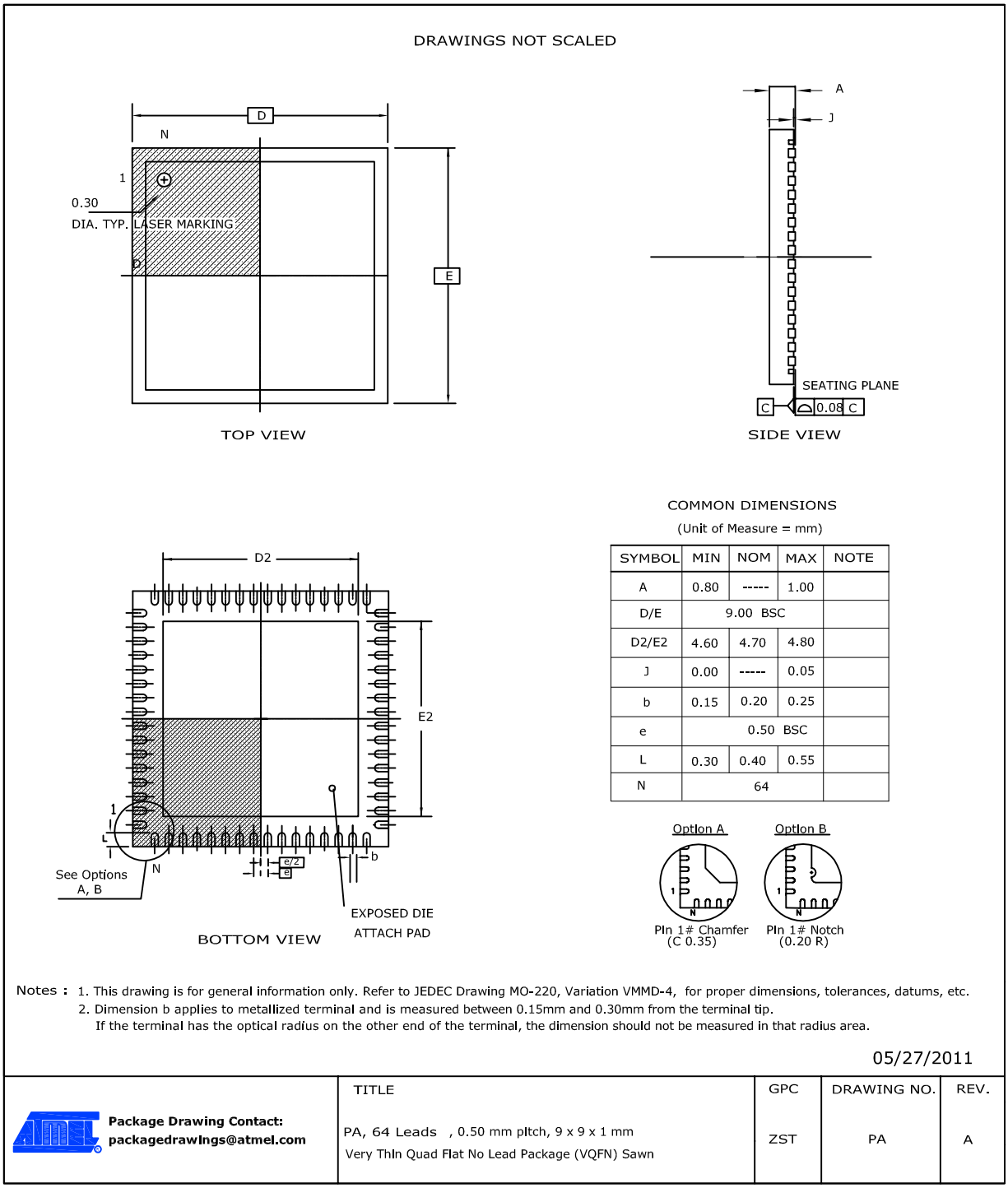
Related Links

Thermal Resistance Data on page 42

Table 12-7. Package Reference

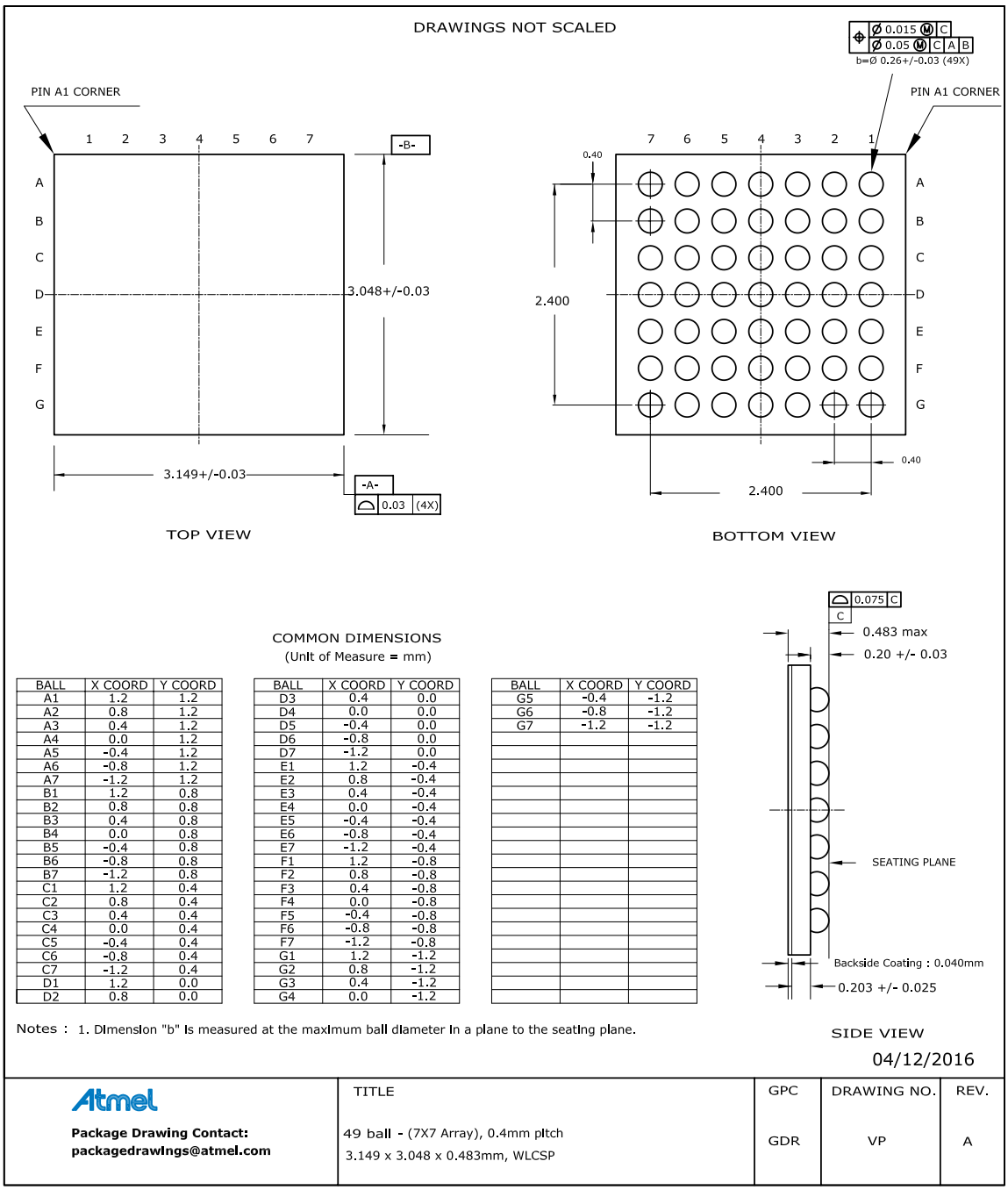
JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.3. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

12.2.4. 49-Ball WLCSP



BALL	X COORD	Y COORD
A1	1.2	1.2
A2	0.8	1.2
A3	0.4	1.2
A4	0.0	1.2
A5	-0.4	1.2
A6	-0.8	1.2
A7	-1.2	1.2
B1	1.2	0.8
B2	0.8	0.8
B3	0.4	0.8
B4	0.0	0.8
B5	-0.4	0.8
B6	-0.8	0.8
B7	-1.2	0.8
C1	1.2	0.4
C2	0.8	0.4
C3	0.4	0.4
C4	0.0	0.4
C5	-0.4	0.4
C6	-0.8	0.4
C7	-1.2	0.4
D1	1.2	0.0
D2	0.8	0.0

BALL	X COORD	Y COORD
D3	0.4	0.0
D4	0.0	0.0
D5	-0.4	0.0
D6	-0.8	0.0
D7	-1.2	0.0
E1	1.2	-0.4
E2	0.8	-0.4
E3	0.4	-0.4
E4	0.0	-0.4
E5	-0.4	-0.4
E6	-0.8	-0.4
E7	-1.2	-0.4
F1	1.2	-0.8
F2	0.8	-0.8
F3	0.4	-0.8
F4	0.0	-0.8
F5	-0.4	-0.8
F6	-0.8	-0.8
F7	-1.2	-0.8
G1	1.2	-1.2
G2	0.8	-1.2
G3	0.4	-1.2
G4	0.0	-1.2

BALL	X COORD	Y COORD
G5	-0.4	-1.2
G6	-0.8	-1.2
G7	-1.2	-1.2

Table 12-11. Device and Package Maximum Weight

8.45	mg

Table 12-12. Package Characteristics

Moisture Sensitivity Level	MSL1