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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22n18a-aut

Table of Contents

1. Description

Atmel | SMART SAM L22 is a series of Ultra low-power segment LCD microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, ranging from 48- to 100-pins with up to 256KB Flash and 32KB of SRAM and can drive up to 320 LCD segments. The SAM L22 devices operate at a maximum frequency of 32MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM L22 devices provide the following features: Segment LCD (SLCD) controller with up to 48 selectable SLCD pins from max. 52 pins to drive up to 320 segments, all SLCD Pins can be used also as GPIOs (100-pin package: 8 of the SLCD pins can be used only as GP input), in-system programmable Flash, sixteen-channel direct memory access (DMA) controller, 8 channel Event System, programmable interrupt controller, up to 82 programmable I/O pins, 32-bit real-time clock and calendar, up to four 16-bit Timer/Counters (TC) and one 24-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and the TCC has extended functions optimized for motor, lighting and other control applications. The series provide one full-speed USB 2.0 device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I^2C up to 3.4MHz, SMBus, PMBus, and ISO7816 smart card interface; up to twenty channel 1Msps 12-bit ADC with optional oversampling and decimation supporting up to 16-bit resolution, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM L22 devices have four software-selectable sleep modes, idle, standby, backup and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The SAM L22 devices have two software-selectable performance level (PL0 and PL2) allowing the user to scale the lowest core voltage level that will support the operating frequency.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for nonintrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The Atmel SAM L22 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

2. Configuration Summary

	SAM L22N	SAM L22J	SAM L22G
Pins	100	64	48 (QFN and TQFP) 49 (WLCSP)
General Purpose I/O-pins (GPIOs)[1]	82	50	36
Flash	256/128/64KB	256/128/64KB	256/128/64KB
Flash RWW section	8/4/2KB	8/4/2KB	8/4/2KB
System SRAM	32/16/8KB	32/16/8KB	32/16/8KB
Segment LCD (SLCD) Pins[1]	48 selectable from 52	31	23
Timer Counter (TC) instances	4	4	4
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	1	1	1
Waveform output channels per TCC	4	4	4
DMA channels	16	16	16
USB interface	1	1	1
AES engine	1	1	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
True Random Generator (TRNG)	1	1	1
Serial Communication Interface (SERCOM) instances	6	4[2]	4[2]
Analog-to-Digital Converter (ADC) channels	20	16	10
Two Analog Comparators (AC) with number of external input channels	4	4	2
Tamper Input Pins	5	3	2

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML22J18A-MUT			QFN64	

3.3. SAM L22G

Table 3-3. SAM L22G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML22G16A-MUT			QFN48	
ATSAML22G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML22G17A-MUT			QFN48	
ATSAML22G17A-UUT			WLCSP49	
ATSAML22G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML22G18A-MUT			QFN48	
ATSAML22G18A-UUT			WLCSP49	

3.4. Device Identification

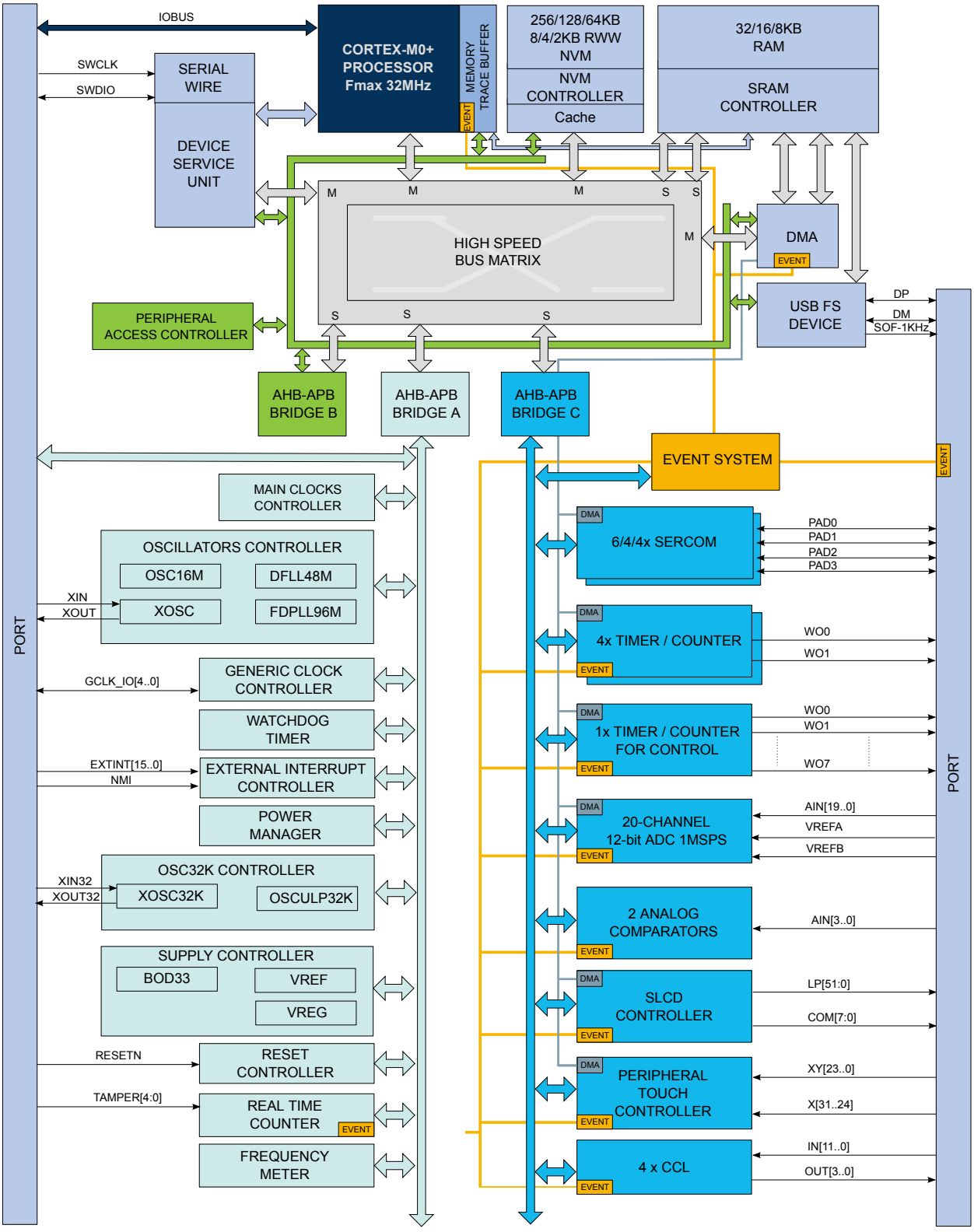
The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

Table 3-4. SAM L22 Device Identification Values

DSU DID.DEVSEL	Device
0x0	L22N18
0x1	L22N17
0x2	L22N16
0x3-0x4	Reserved
0x5	L22J18
0x6	L22J17
0x7	L22J16
0x8-0x9	Reserved
0xA	L22G18
0xB	L22G17
0xC	L22G16
0xD-0xFF	Reserved

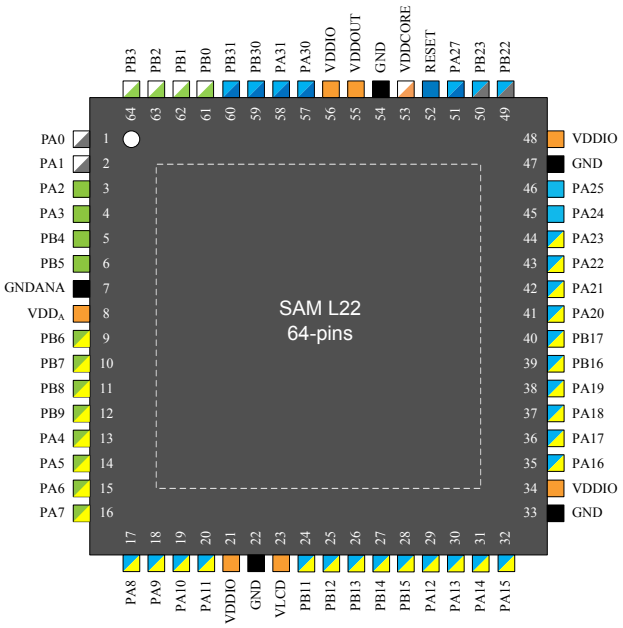
Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

4. Block Diagram

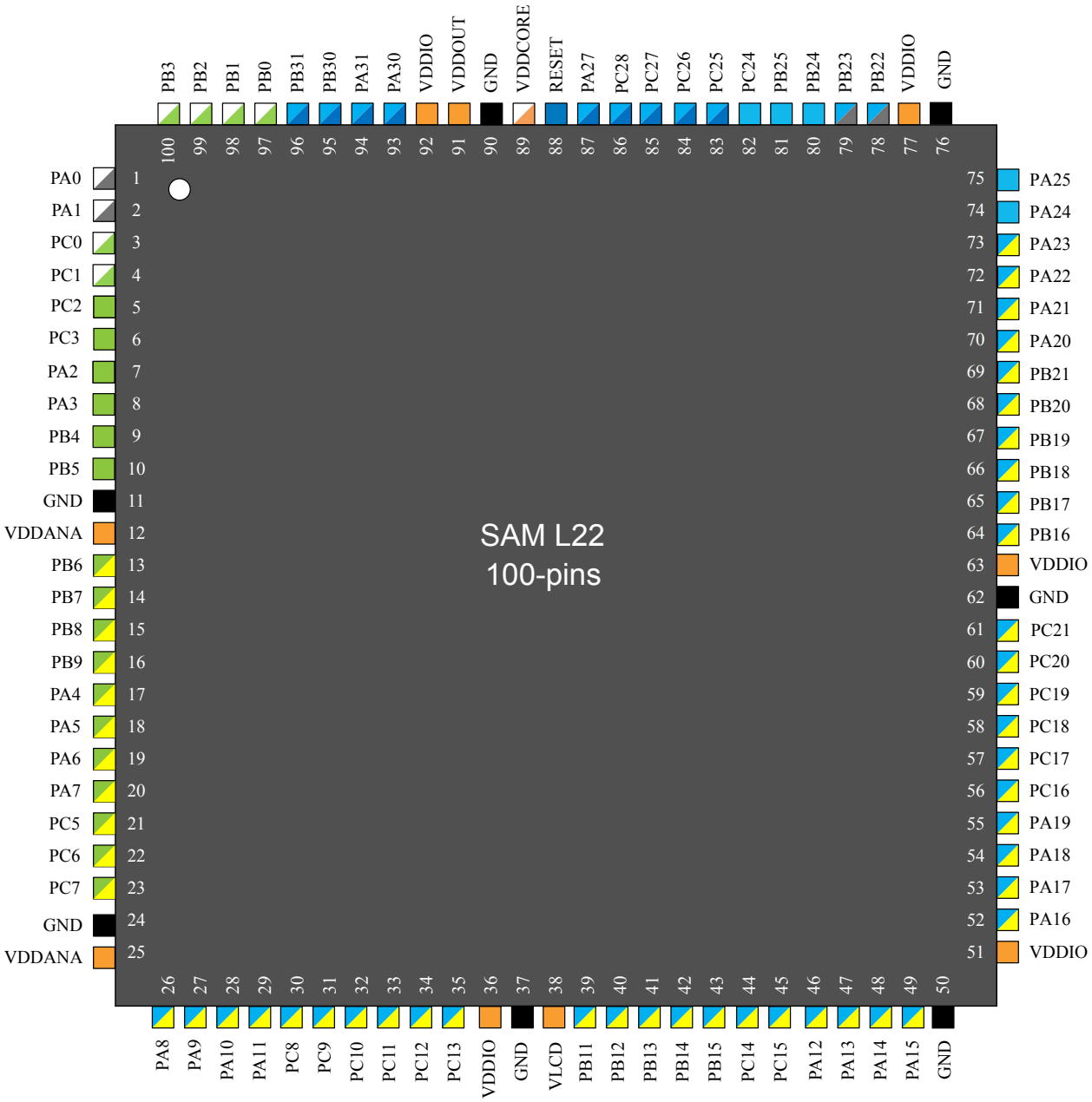


Note:

5.2. SAM L22J


SAM L22
64-pins
PB3 64
PB2 63
PB1 62
PB0 61
PB31 60
PB30 59
PA31 58
PA30 57
VDDIO 56
VDDOUT 55
GND 54
VDDCORE 53
RESET 52
PA27 51
PB23 50
PB22 49
PA0 1
PA1 2
PA2 3
PA3 4
PB4 5
PB5 6
GNDANA 7
VDDA 8
PB6 9
PB7 10
PB8 11
PB9 12
PA4 13
PA5 14
PA6 15
PA7 16
48 VDDIO
47 GND
46 PA25
45 PA24
44 PA23
43 PA22
42 PA21
41 PA20
40 PB17
39 PB16
38 PA19
37 PA18
36 PA17
35 PA16
34 VDDIO
33 GND
17 PA8
18 PA9
19 PA10
20 PA11
21 VDDIO
22 GND
23 VLCD
24 PB11
25 PB12
26 PB13
27 PB14
28 PB15
29 PA12
30 PA13
31 PA14
32 PA15

5.3. SAM L22N


SAM L22
100-pins
PB3 100
PB2 99
PB1 98
PB0 97
PB31 96
PB30 95
PA31 94
PA30 93
VDDIO 92
VDDOUT 91
GND 90
VDDCORE 89
RESET 88
PA27 87
PC28 86
PC27 85
PC26 84
PC25 83
PC24 82
PB25 81
PB24 80
PB23 79
PB22 78
VDDIO 77
GND 76
PA0 1
PA1 2
PC0 3
PC1 4
PC2 5
PC3 6
PA2 7
PA3 8
PB4 9
PB5 10
GND 11
VDDANA 12
PB6 13
PB7 14
PB8 15
PB9 16
PA4 17
PA5 18
PA6 19
PA7 20
PC5 21
PC6 22
PC7 23
GND 24
VDDANA 25
75 PA25
74 PA24
73 PA23
72 PA22
71 PA21
70 PA20
69 PB21
68 PB20
67 PB19
66 PB18
65 PB17
64 PB16
63 VDDIO
62 GND
61 PC21
60 PC20
59 PC19
58 PC18
57 PC17
56 PC16
55 PA19
54 PA18
53 PA17
52 PA16
51 VDDIO
26 PA8
27 PA9
28 PA10
29 PA11
30 PC8
31 PC9
32 PC10
33 PC11
34 PC12
35 PC13
36 VDDIO
37 GND
38 VLCD
39 PB11
40 PB12
41 PB13
42 PB14
43 PB15
44 PC14
45 PC15
46 PA12
47 PA13
48 PA14
49 PA15
50 GND

Signal Name	Function	Type	Active Level
SOF 1kHz	USB Start of Frame	Digital	
Real Timer Clock - RTC			
RTC_IN[4:0]	Tamper or external wake-up pins	Digital	
RTC_OUT	Tamper output	Digital	

7. I/O Multiplexing and Considerations

7.1. Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned a different peripheral functions. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to '1'. The selection of peripheral function A to I is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) of the PORT.

This table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 7-1. PORT Function Multiplexing

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
Battery backup	1	1	1	PA00	EIC/EXTINT[0]							SERCOM1/ PAD[0]					
	2	2	2	PA01	EIC/EXTINT[1]							SERCOM1/ PAD[1]					
			3	PC00	EIC/EXTINT[8]		ADC/ AIN[16]								RTC/IN[3]		
			4	PC01	EIC/EXTINT[9]		ADC/ AIN[17]								RTC/IN[4]		
			5	PC02	EIC/EXTINT[10]		ADC/ AIN[18]		PTC/ XY[6]								
			6	PC03	EIC/EXTINT[11]		ADC/ AIN[19]		PTC/ XY[7]								
	3	3	7	PA02	EIC/EXTINT[2]	ADC/ VREFB	ADC/ AIN[0]	AC/ AIN[0]	PTC/ XY[8]						RTC/IN[2]		
	4	4	8	PA03	EIC/EXTINT[3]	ADC/ VREFA	ADC/ AIN[1]	AC/ AIN[1]	PTC/ XY[9]								
		5	9	PB04	EIC/EXTINT[4]		ADC/ AIN[12]	AC/ AIN[2]	PTC/ XY[10]								
		6	10	PB05	EIC/EXTINT[5]		ADC/ AIN[13]	AC/ AIN[3]	PTC/ XY[11]								
		9	13	PB06	EIC/EXTINT[6]		ADC/ AIN[14]		PTC/ XY[12]	SLCD/ LP[0]							CCL/IN[6]
		10	14	PB07	EIC/EXTINT[7]		ADC/ AIN[15]		PTC/ XY[13]	SLCD/ LP[1]							CCL/IN[7]
	7	11	15	PB08	EIC/EXTINT[8]		ADC/ AIN[2]		PTC/ XY[14]	SLCD/ LP[2]		SERCOM3/ PAD[0]	TC/0/ WO[0]				CCL/IN[8]
	8	12	16	PB09	EIC/EXTINT[9]		ADC/ AIN[3]		PTC/ XY[15]	SLCD/ LP[3]		SERCOM3/ PAD[1]	TC/0/ WO[1]				CCL/ OUT[2]
	9	13	17	PA04	EIC/EXTINT[4]		ADC/ AIN[4]		PTC/ X[24]	SLCD/ LP[4]		SERCOM0/ PAD[0]	TCC/ WO[0]				CCL/IN[0]
	10	14	18	PA05	EIC/EXTINT[5]		ADC/ AIN[5]		PTC/ X[25]	SLCD/ LP[5]		SERCOM0/ PAD[1]	TCC/ WO[1]				CCL/IN[1]
	11	15	19	PA06	EIC/EXTINT[6]		ADC/ AIN[6]		PTC/ X[26]	SLCD/ LP[6]		SERCOM0/ PAD[2]					CCL/IN[2]
	12	16	20	PA07	EIC/EXTINT[7]		ADC/ AIN[7]		PTC/ X[27]	SLCD/ LP[7]		SERCOM0/ PAD[3]					CCL/ OUT[0]
			21	PC05	EIC/EXTINT[13]				PTC/ XY[4]	SLCD/ LP[8]							
			22	PC06	EIC/EXTINT[14]				PTC/ XY[5]	SLCD/ LP[9]							
			23	PC07	EIC/EXTINT[15]					SLCD/ LP[10]							
	13	17	26	PA08	EIC/NMI				PTC/ XY[3]	SLCD/ LP[11]	SERCOM0/ PAD[0]	SERCOM4/ PAD[0]	TCC/ WO[0]				CCL/IN[3]
	14	18	27	PA09	EIC/EXTINT[9]				PTC/ XY[2]	SLCD/ LP[12]	SERCOM0/ PAD[1]	SERCOM4/ PAD[1]	TCC/ WO[1]				CCL/IN[4]
	15	19	28	PA10	EIC/EXTINT[10]				PTC/ XY[1]	SLCD/ LP[13]	SERCOM0/ PAD[2]	SERCOM4/ PAD[2]		TCC/ WO[2]		GCLK/ IO[4]	CCL/IN[5]
	16	20	29	PA11	EIC/EXTINT[11]				PTC/ XY[0]	SLCD/ LP[14]	SERCOM0/ PAD[3]	SERCOM4/ PAD[3]		TCC/ WO[3]			CCL/ OUT[1]

Figure 8-2. Power Supply Connection for Switching/Linear Mode

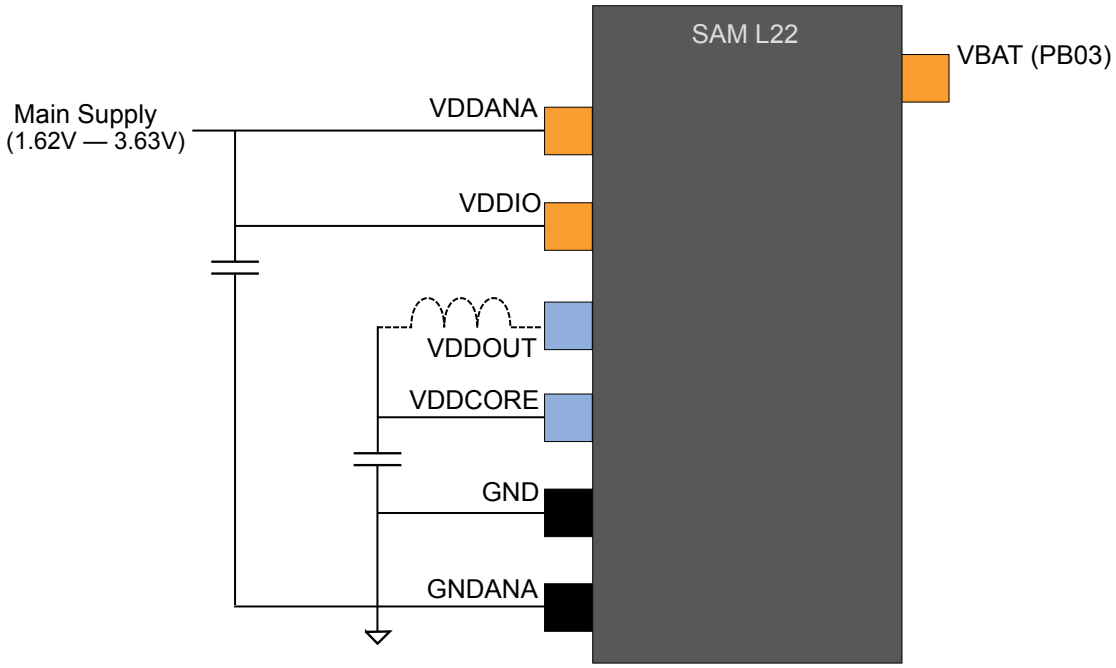
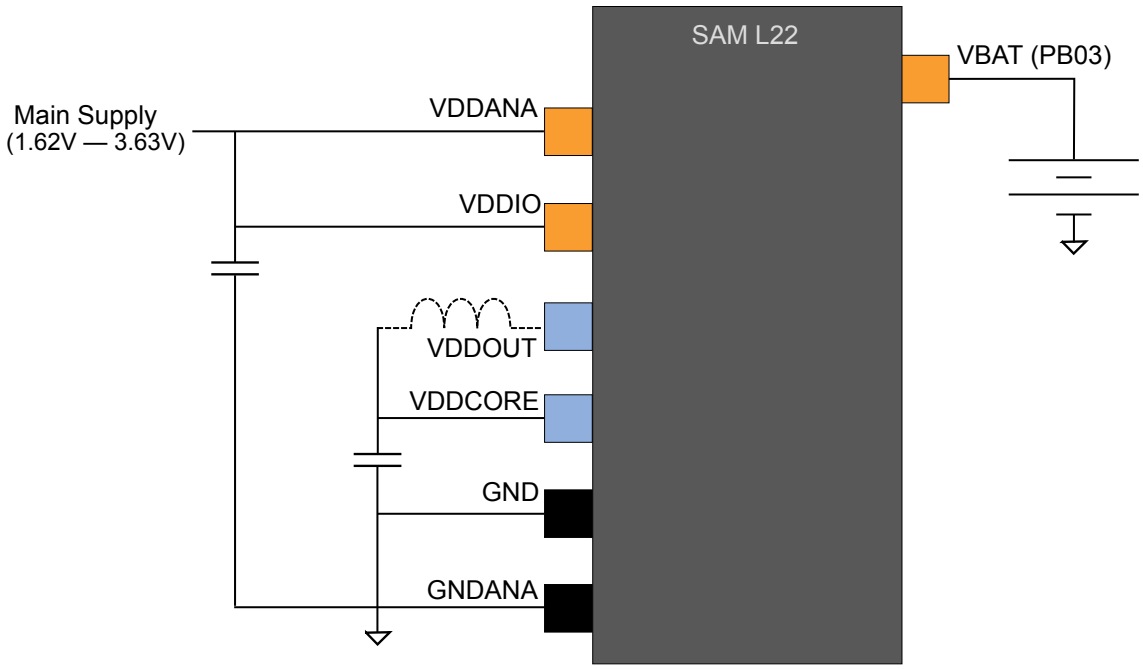


Figure 8-3. Power Supply Connection for Battery Backup



8.2.4. Power-Up Sequence

8.2.4.1. Supply Order

VDDIO and VDDANA must have the same supply sequence. Ideally, they must be connected together.

8.2.4.2. Minimum Rise Rate

One integrated power-on reset (POR) circuits monitoring VDDIO requires a minimum rise rate.

8.2.4.3. Maximum Rise Rate

The rise rate of the power supplies must not exceed the values described in Electrical Characteristics.

8.3. Power-Up

This section summarizes the power-up sequence of the SAM L22. The behavior after power-up is controlled by the Power Manager.

8.3.1. Starting of Internal Regulator

After power-up, the device is set to its initial state and kept in Reset, until the power has stabilized throughout the device. The default performance level after power-up is PL0.

The internal regulator provides the internal VDDCORE corresponding to this performance level. Once the external voltage VDDIO and the internal VDDCORE reach a stable value, the internal Reset is released.

8.3.2. Starting of Clocks

Once the power has stabilized and the internal Reset is released, the device will use a 4MHz clock by default. The clock source for this clock signal is OSC16M, which is enabled and configured at 4MHz after a reset by default. This is also the default time base for Generic Clock Generator 0. In turn, Generator 0 provides the main clock GCLK_MAIN which is used by the Power Manager (PM).

Some synchronous system clocks are active after Start-Up, allowing software execution. Refer to the “Clock Mask Register” section in the PM-Power Manager documentation for the list of clocks that are running by default. Synchronous system clocks that are running receive the 4MHz clock from Generic Clock Generator 0. Other generic clocks are disabled.

8.3.3. I/O Pins

After power-up, the I/O pins are tri-stated except PA30, which is pull-up enabled and configured as input.

8.3.4. Fetching of Initial Instructions

After Reset has been released, the CPU starts fetching PC and SP values from the Reset address, 0x00000000. This points to the first executable address in the internal Flash memory. The code read from the internal Flash can be used to configure the clock system and clock sources. See the related peripheral documentation for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

8.4. Power-On Reset and Brown-Out Detector

The SAM L22 embeds three features to monitor, warn and/or reset the device:

- POR: Power-on Reset on VSWOUT and VDDIO
- BOD33: Brown-out detector on VSWOUT/VBAT
- Brown-out detector internal to the voltage regulator for VDDCORE. BOD12 is calibrated in production and its calibration parameters are stored in the NVM User Row. This data should not be changed if the User Row is written to in order to assure correct behavior.

8.4.1. Power-On Reset on VSWOUT

VSWOUT is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VSWOUT goes below the threshold voltage, the entire chip is reset.

8.4.2. Power-On Reset on VDDIO

VDDIO is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VDDIO goes below the threshold voltage, all I/Os supplied by VDDIO are reset.

8.4.3. Brown-Out Detector on VSWOUT/VBAT

BOD33 monitors VSWOUT or VBAT depending on configuration.

8.4.4. Brown-Out Detector on VDDCORE

Once the device has started up, BOD12 monitors the internal VDDCORE.

8.5. Performance Level Overview

By default, the device will start in Performance Level 0. This PL0 is aiming for the lowest power consumption by limiting logic speeds and the CPU frequency. As a consequence, all GCLK will have limited capabilities, and some peripherals and clock sources will not work or with limited capabilities:

List of peripherals/clock sources not available in PL0:

- USB (limited by logic frequency)
- DFLL48M

List of peripherals/clock sources with limited capabilities in PL0:

- All AHB/APB peripherals are limited by CPU frequency
- DPLL96M: may be able to generate 48MHz internally, but the output cannot be used by logic
- GCLK: the maximum frequency is by factor 4 compared to PL2
- SW interface: the maximum frequency is by factor 4 compared to PL2
- TC: the maximum frequency is by factor 4 compared to PL2
- TCC:the maximum frequency is by factor 4 compared to PL2
- SERCOM: the maximum frequency is by factor 4 compared to PL2

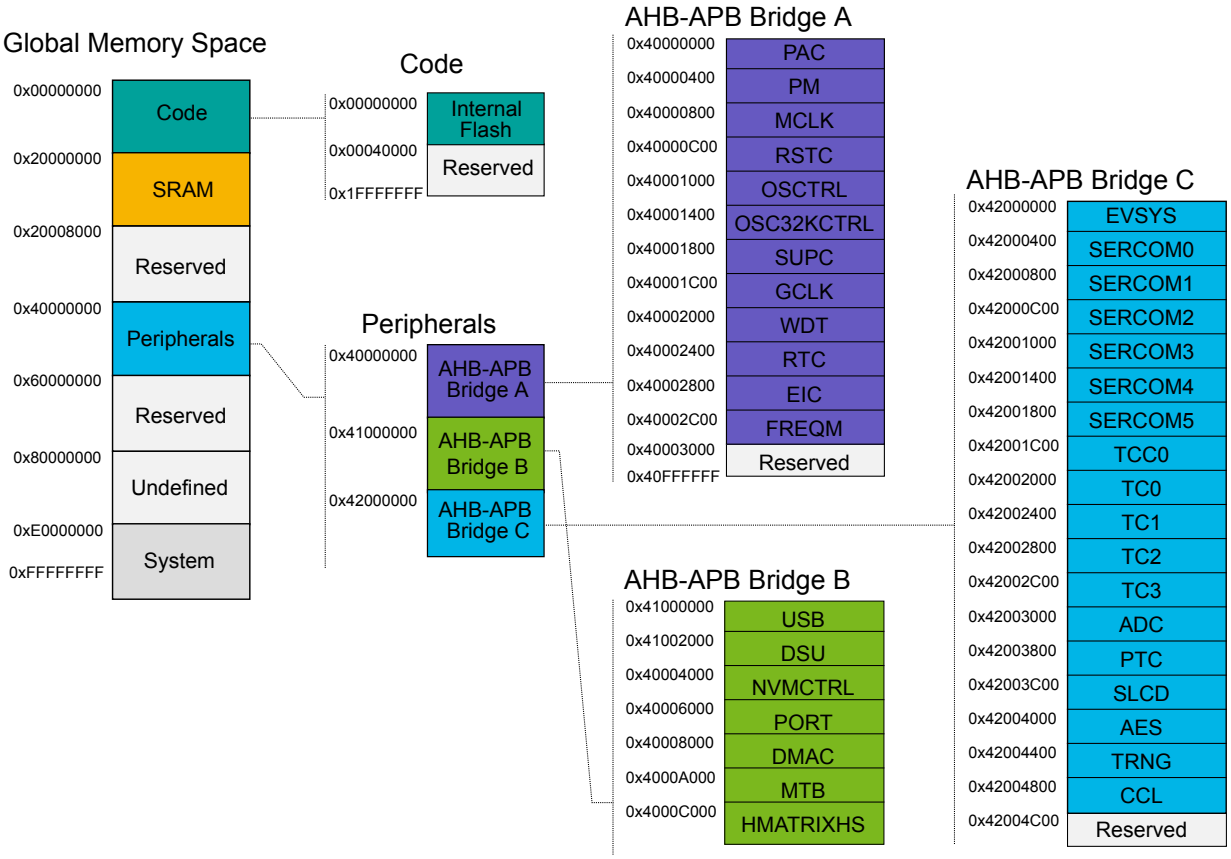
List of peripherals/clock sources with full capabilities in PL0:

- AC
- ADC
- EIC
- OSC16M
- PTC
- All 32KHz clock sources and peripherals

Full functionality and capability will be ensured in PL2. When transitioning between performance levels, the Supply Controller (SUPC) will provide a configurable smooth voltage scaling transition.

9. Product Mapping

Figure 9-1. Atmel SAM L22 Product Mapping



11. Processor and Architecture

11.1. Cortex M0+ Processor

The Atmel SAM L22 implements the ARM ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

11.1.1. Cortex M0+ Configuration

Table 11-1. Cortex M0+ Configuration

Features	Cortex-M0+ options	SAM L22 configuration
Interrupts	External interrupts 0-32	27
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

11.1.2. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

arriving interrupts. Refer to NVIC-Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).

Note: When the CPU frequency is much higher than the APB frequency it is recommended to insert a memory read barrier after each CPU write to registers mapped on the APB. Failing to do so in such conditions may lead to unexpected behavior such as e.g. re-entering a peripheral interrupt handler just after leaving it.

- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section MTB-Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (http://www.arm.com).
- Memory Protection Unit (MPU)
  - The Memory Protection Unit divides the memory map into a number of regions, and defines the location, size, access permissions and memory attributes of each region. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com)

11.1.3. Cortex M0+ Address Map

Table 11-2. Cortex-M0+ Address Map

Address	Peripheral
0xE000E000	System Control Space (SCS)
0xE000E010	System Timer (SysTick)
0xE000E100	Nested Vectored Interrupt Controller (NVIC)
0xE000ED00	System Control Block (SCB)
0x41006000	Micro Trace Buffer (MTB)

Related Links

Product Mapping on page 30

11.1.4. I/O Interface

The device allows direct access to PORT registers. Accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, so the Cortex M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O access to be sustained for as long as necessary.

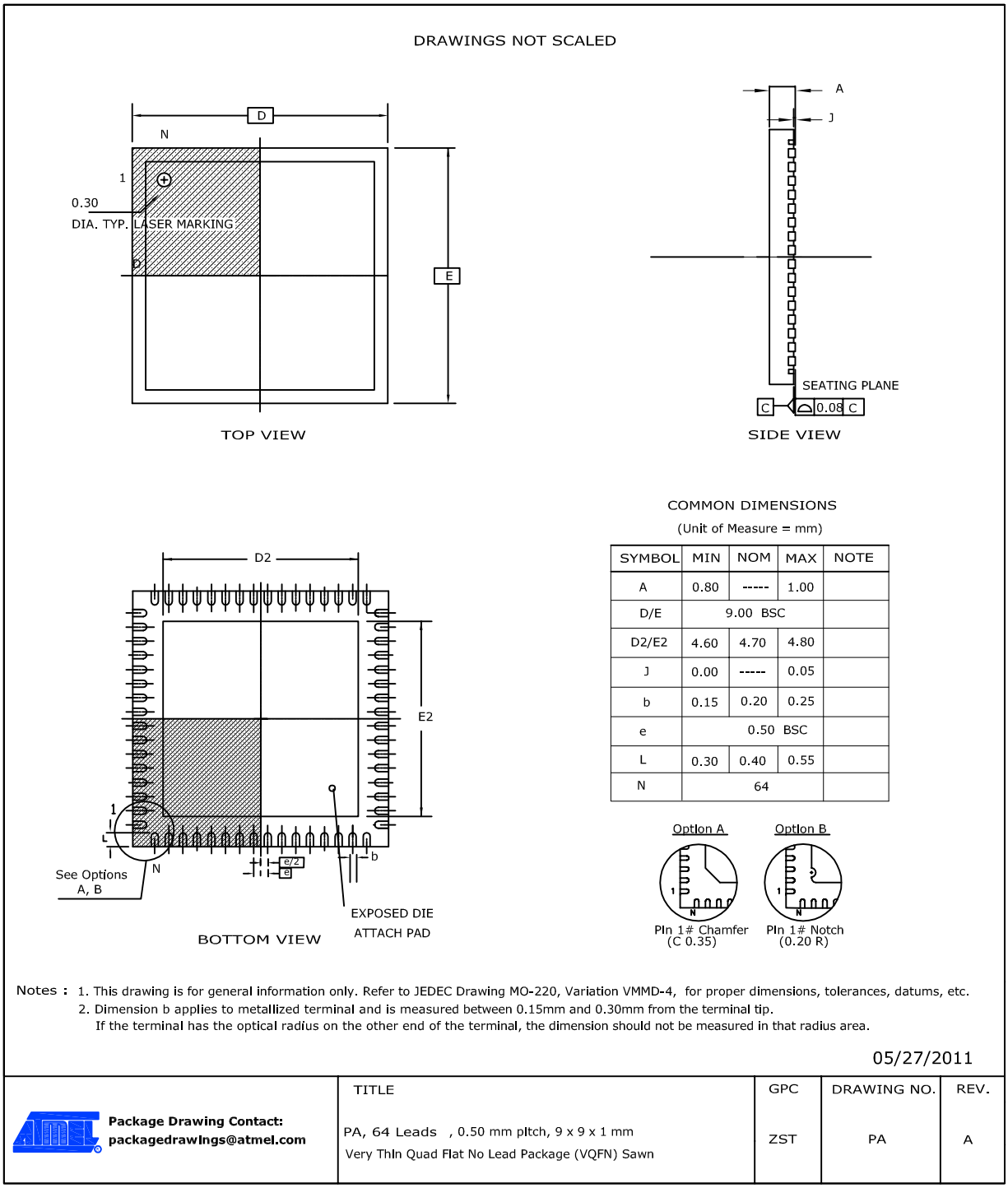
SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
USB - Universal Serial Bus	7	Direct	IP-QOSCTRL	0x3
MTB - Micro Trace Buffer	8	Direct	STATIC-3	0x3

Note: 1. Using 32-bit access only.

Table 12-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.3. 64 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.

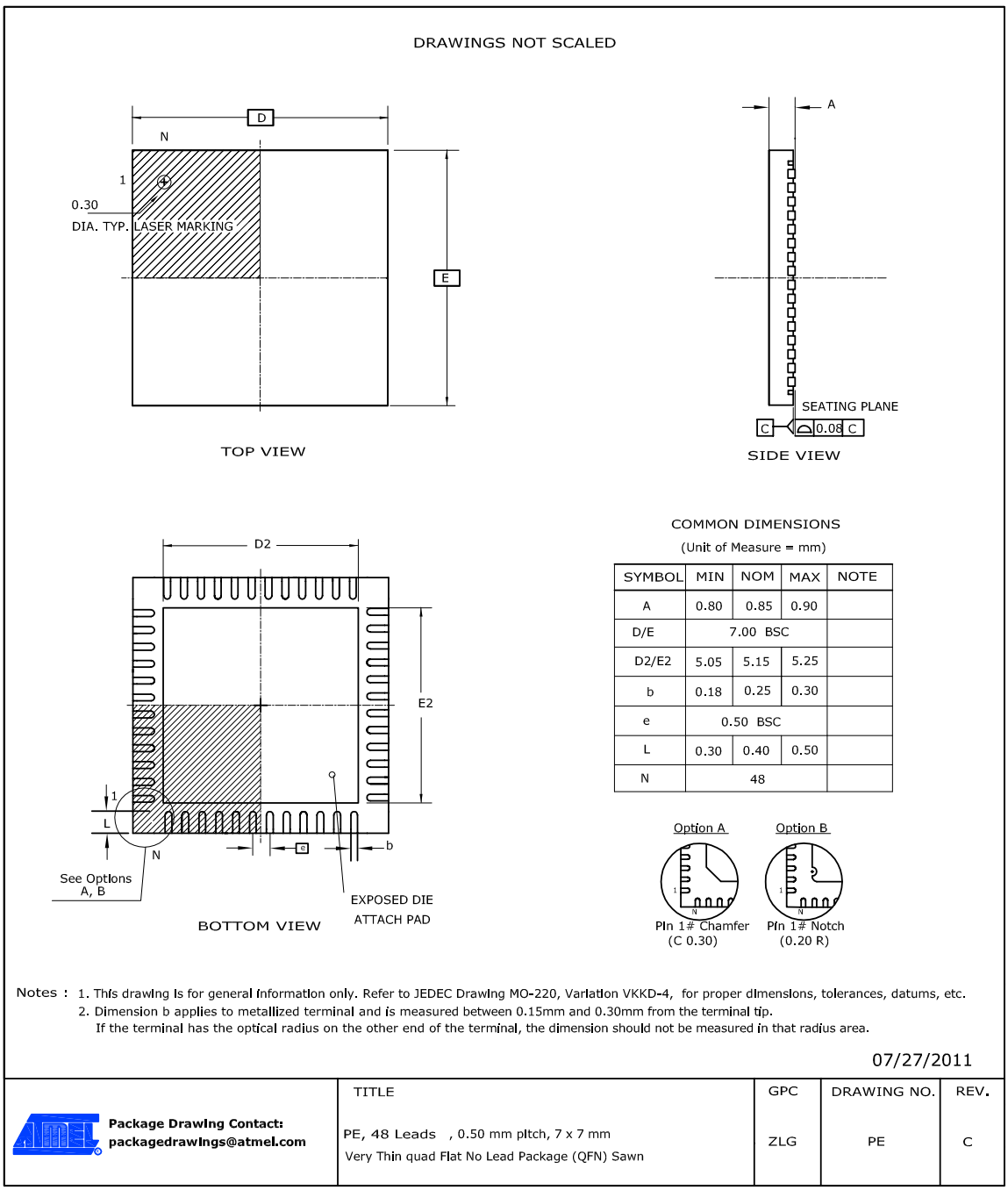
Table 12-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 12-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

12.2.6. 48 pin QFN



Note: The exposed die attach pad is not connected electrically inside the device.