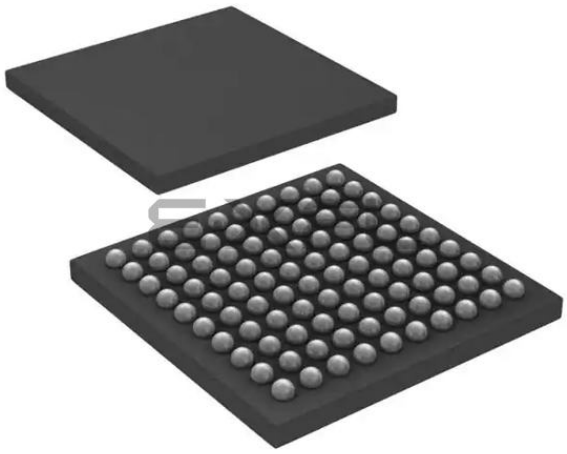

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml22n18a-cfut

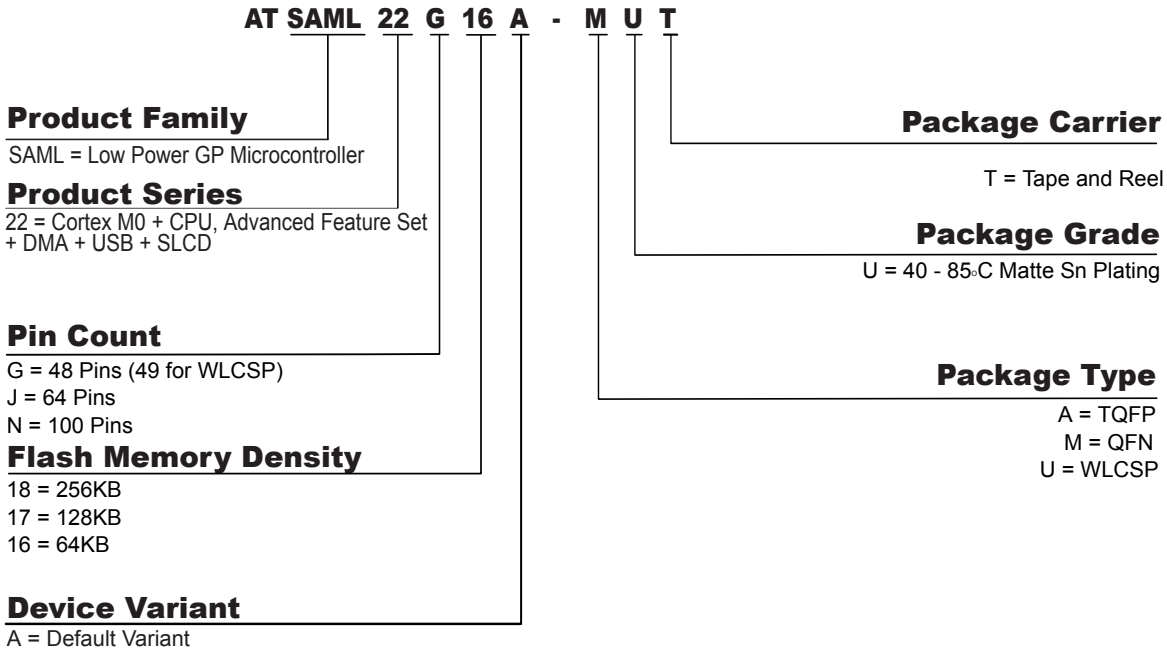
  - One True Random Generator (TRNG)
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - Up to 256-Channel capacitive touch sensing
      - Maximum Mutual-Cap up to 16x16 channels
      - Maximum Self-Cap up to 24 channels
    - Wake-up on touch in standby mode
- Oscillators
  - 32.768kHz crystal oscillator (XOSC32K)
  - 0.4-32MHz crystal oscillator (XOSC)
  - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
  - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
  - 48MHz Digital Frequency Locked Loop (DFLL48M)
  - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
  - Up to 82 programmable I/O pins
  - Up to 52 segment LCD pins can be used as GPIO/GPI
  - Up to 5 wake-up pins with optional debouncing
  - Up to 5 tamper input pins
  - 1 tamper output pin
- Pin and code compatible with SAM D and SAM L Cortex-M0+ Families[2]
- Packages
  - 100-pin TQFP
  - 64-pin TQFP, QFN
  - 49-pin WLCSP
  - 48-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V

[2] except the VLCD

2. Configuration Summary

	SAM L22N	SAM L22J	SAM L22G
Pins	100	64	48 (QFN and TQFP) 49 (WLCSP)
General Purpose I/O-pins (GPIOs)[1]	82	50	36
Flash	256/128/64KB	256/128/64KB	256/128/64KB
Flash RWW section	8/4/2KB	8/4/2KB	8/4/2KB
System SRAM	32/16/8KB	32/16/8KB	32/16/8KB
Segment LCD (SLCD) Pins[1]	48 selectable from 52	31	23
Timer Counter (TC) instances	4	4	4
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	1	1	1
Waveform output channels per TCC	4	4	4
DMA channels	16	16	16
USB interface	1	1	1
AES engine	1	1	1
Configurable Custom Logic (CCL) (LUTs)	4	4	4
True Random Generator (TRNG)	1	1	1
Serial Communication Interface (SERCOM) instances	6	4[2]	4[2]
Analog-to-Digital Converter (ADC) channels	20	16	10
Two Analog Comparators (AC) with number of external input channels	4	4	2
Tamper Input Pins	5	3	2

3. Ordering Information



Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

3.1. SAM L22N

Table 3-1. SAM L22N Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22N16A-AUT	64K	8K	TQFP100	Tape & Reel
ATSAML22N17A-AUT	128K	16K	TQFP100	Tape & Reel
ATSAML22N18A-AUT	256K	32K	TQFP100	Tape & Reel

3.2. SAM L22J

Table 3-2. SAM L22J Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J16A-AUT	64K	8K	TQFP64	Tape & Reel
ATSAML22J16A-MUT			QFN64	
ATSAML22J17A-AUT	128K	16K	TQFP64	Tape & Reel
ATSAML22J17A-MUT			QFN64	

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22J18A-AUT	256K	32K	TQFP64	Tape & Reel
ATSAML22J18A-MUT			QFN64	

3.3. SAM L22G

Table 3-3. SAM L22G Ordering Codes

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAML22G16A-AUT	64K	8K	TQFP48	Tape & Reel
ATSAML22G16A-MUT			QFN48	
ATSAML22G17A-AUT	128K	16K	TQFP48	Tape & Reel
ATSAML22G17A-MUT			QFN48	
ATSAML22G17A-UUT			WLCSP49	
ATSAML22G18A-AUT	256K	32K	TQFP48	Tape & Reel
ATSAML22G18A-MUT			QFN48	
ATSAML22G18A-UUT			WLCSP49	

3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

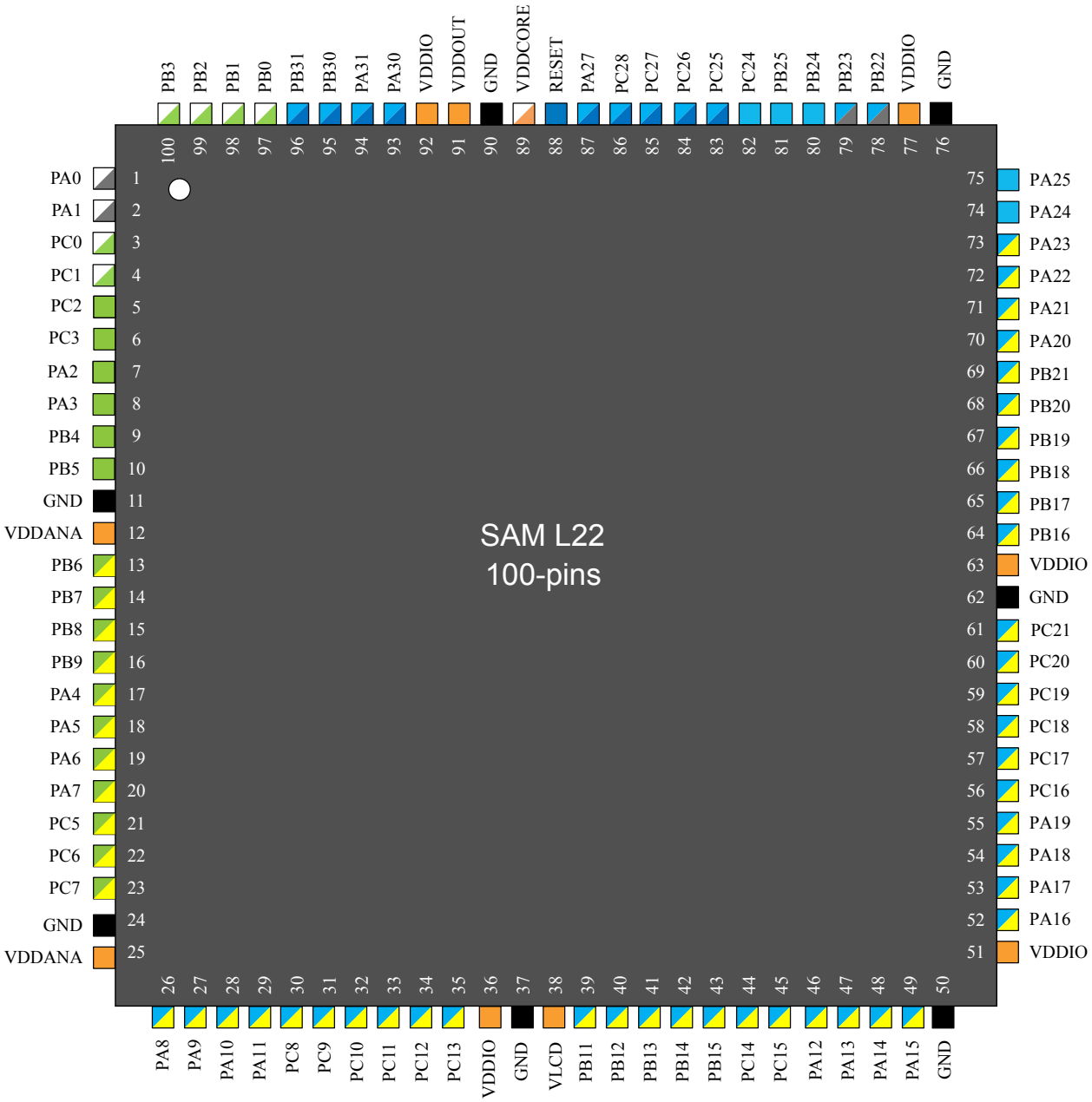
Table 3-4. SAM L22 Device Identification Values

DSU DID.DEVSEL	Device
0x0	L22N18
0x1	L22N17
0x2	L22N16
0x3-0x4	Reserved
0x5	L22J18
0x6	L22J17
0x7	L22J16
0x8-0x9	Reserved
0xA	L22G18
0xB	L22G17
0xC	L22G16
0xD-0xFF	Reserved

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

1. Some device configurations have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. The number of PTC X and Y signals is configurable.

5.3. SAM L22N


SAM L22
100-pins
PB3 100
PB2 99
PB1 98
PB0 97
PB31 96
PB30 95
PA31 94
PA30 93
VDDIO 92
VDDOUT 91
GND 90
VDDCORE 89
RESET 88
PA27 87
PC28 86
PC27 85
PC26 84
PC25 83
PC24 82
PB25 81
PB24 80
PB23 79
PB22 78
VDDIO 77
GND 76
PA0 1
PA1 2
PC0 3
PC1 4
PC2 5
PC3 6
PA2 7
PA3 8
PB4 9
PB5 10
GND 11
VDDANA 12
PB6 13
PB7 14
PB8 15
PB9 16
PA4 17
PA5 18
PA6 19
PA7 20
PC5 21
PC6 22
PC7 23
GND 24
VDDANA 25
75 PA25
74 PA24
73 PA23
72 PA22
71 PA21
70 PA20
69 PB21
68 PB20
67 PB19
66 PB18
65 PB17
64 PB16
63 VDDIO
62 GND
61 PC21
60 PC20
59 PC19
58 PC18
57 PC17
56 PC16
55 PA19
54 PA18
53 PA17
52 PA16
51 VDDIO
26 PA8
27 PA9
28 PA10
29 PA11
30 PC8
31 PC9
32 PC10
33 PC11
34 PC12
35 PC13
36 VDDIO
37 GND
38 VLCD
39 PB11
40 PB12
41 PB13
42 PB14
43 PB15
44 PC14
45 PC15
46 PA12
47 PA13
48 PA14
49 PA15
50 GND

6. Signal Descriptions List

The following table gives details on signal names classified by peripheral.

Table 6-1. Signal Descriptions List

Signal Name	Function	Type	Active Level
Analog Comparators - AC			
AIN[3:0]	AC Analog Inputs	Analog	
CMP[1:0]	AC Analog Output	Analog	
Analog Digital Converter - ADC			
AIN[19:0]	ADC Analog Inputs	Analog	
VREFA	ADC Voltage External Reference A	Analog	
VREFB	ADC Voltage External Reference B	Analog	
External Interrupt Controller - EIC			
EXTINT[15:0]	External Interrupts inputs	Digital	
NMI	External Non-Maskable Interrupt input	Digital	
Generic Clock Generator - GCLK			
GCLK_IO[4:0]	Generic Clock (source clock inputs or generic clock generator output)	Digital	
Custom Control Logic - CCL			
IN[11:0]	Logic Inputs	Digital	
OUT[3:0]	Logic Outputs	Digital	
Supply Controller - SUPC			
VBAT	External battery supply Inputs	Analog	
PSOK	Main Power Supply OK input	Digital	
OUT[1:0]	Logic Outputs	Digital	
Power Manager - PM			
RESETN	Reset input	Digital	Low
Serial Communication Interface - SERCOMx			
PAD[3:0]	SERCOM Inputs/Outputs Pads	Digital	
Oscillators Control - OSCCTRL			
XIN	Crystal or external clock Input	Analog/Digital	
XOUT	Crystal Output	Analog	

Signal Name	Function	Type	Active Level
32KHz Oscillators Control - OSC32KCTRL			
XIN32	32KHz Crystal or external clock Input	Analog/Digital	
XOUT32	32KHz Crystal Output	Analog	
Timer Counter - TCx			
WO[1:0]	Waveform Outputs	Digital	
Timer Counter - TCCx			
WO[7:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[7:0]	PTC Input/Output	Analog	
Y[23:0]	PTC Input/Output	Analog	
X[31:24]	PTC Output	Analog	
General Purpose I/O - PORT			
PA25 - PA00	Parallel I/O Controller I/O Port A	Digital	
PA27	Parallel I/O Controller I/O Port A	Digital	
PA31 - PA30	Parallel I/O Controller I/O Port A	Digital	
PB09 - PB00	Parallel I/O Controller I/O Port B	Digital	
PB25 - PB11	Parallel I/O Controller I/O Port B	Digital	
PB31 - PB30	Parallel I/O Controller I/O Port B	Digital	
PC03 - PC00	Parallel I/O Controller I/O Port C	Digital	
PC07 - PC05	Parallel I/O Controller I/O Port C	Digital	
PC17 - PC12	Parallel I/O Controller I/O Port C	Digital	
PC28 - PC24	Parallel I/O Controller I/O Port C	Digital	
General Purpose input - PORT			
PC11 - PC08	Parallel I/O Controller input Port C	Digital	
PC21 - PC18	Parallel I/O Controller input Port C	Digital	
Segment LCD			
SLCD51 - SLCD00	Segment LCD	Analog	
VLCD	Bias Voltage	Analog	
Universal Serial Bus - USB			
DP	DP for USB	Digital	
DM	DM for USB	Digital	

Function	-				A	B					C	D	E		F	H	I
Type	L22G[5]	L22J	L22N	Pad Name	EIC	ANAREF	ADC	AC	PTC	SLCD	SERCOM[6]	SERCOM[6]	TC/TCC	TCC/RTC	COM/RTC	AC/ GCLK/ SUPC	CCL
	38	50	79	PB23	EIC/EXTINT[7]						SERCOM0/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	TCC/ WO[3]		GCLK/ IO[1]	CCL/ OUT[0]
			80	PB24	EIC/EXTINT[8]						SERCOM0/ PAD[0]	SERCOM4/ PAD[0]		TCC/ WO[6]		AC/ CMP[0]	
			81	PB25	EIC/EXTINT[9]						SERCOM0/ PAD[1]	SERCOM4/ PAD[1]		TCC/ WO[7]		AC/ CMP[1]	
			82	PC24	EIC/EXTINT[0]						SERCOM0/ PAD[2]	SERCOM4/ PAD[2]	TC/2/ WO[0]	TCC/ WO[0]			
			83	PC25	EIC/EXTINT[1]						SERCOM0/ PAD[3]	SERCOM4/ PAD[3]	TC/2/ WO[1]	TCC/ WO[1]			
			84	PC26	EIC/EXTINT[2]								TC/3/ WO[0]	TCC/ WO[2]			
			85	PC27	EIC/EXTINT[3]							SERCOM1/ PAD[0]	TC/3/ WO[1]	TCC/ WO[3]			CCL/IN[4]
			86	PC28	EIC/EXTINT[4]				PTC/ XY[20]			SERCOM1/ PAD[1]		TCC/ WO[4]			CCL/IN[5]
recommended for GCLK IO	39	51	87	PA27	EIC/EXTINT[15]				PTC/ XY[21]					TCC/ WO[5]	TAL/BRK	GCLK/ IO[0]	
	40	52	88	RESET_N													
	45	57	93	PA30	EIC/EXTINT[10]				PTC/ XY[22]			SERCOM1/ PAD[2]			CORTEX_M0P/ SWCLK	GCLK/ IO[0]	CCL/IN[3]
	46	58	94	PA31	EIC/EXTINT[11]				PTC/ XY[23]			SERCOM1/ PAD[3]			SWDIO		CCL/ OUT[1]
I2C: Sm, Fm, Fm +, Hs		59	95	PB30	EIC/EXTINT[14]						SERCOM1/ PAD[0]	SERCOM5/ PAD[0]	TCC/ WO[0]				
		60	96	PB31	EIC/EXTINT[15]						SERCOM1/ PAD[1]	SERCOM5/ PAD[1]	TCC/ WO[1]				
Battery backup		61	97	PB00	EIC/EXTINT[0]		ADC/ AIN[8]				SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC/3/ WO[0]		RTC/IN[0]	SUPC/ PSOK	CCL/IN[1]
		62	98	PB01	EIC/EXTINT[1]		ADC/ AIN[9]				SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC/3/ WO[1]	RTC/IN[2]	RTC/OUT	SUPC/ OUT[0]	CCL/IN[2]
	47	63	99	PB02	EIC/EXTINT[2]		ADC/ AIN[10]				SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC/2/ WO[0]		RTC/IN[1]	SUPC/ OUT[1]	CCL/ OUT[0]
	48	64	100	PB03	EIC/EXTINT[3]		ADC/ AIN[11]				SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC/2/ WO[1]			SUPC/ VBAT	

Note:

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See the Type column for supported I^2C modes.
   - Sm: Standard mode, up to 100kHz
   - Fm: Fast mode, up to 400kHz
   - Fm+: Fast mode Plus, up to 1MHz
   - Hs: High-speed mode, up to 3.4MHz
3. These pins are High Sink pins and have different properties than regular pins: PA12, PA13, PA22, PA23, PA27, PA31, PB30, PB31.
4. Clusters of multiple GPIO pins are sharing the same supply pin.
5. The 49th pin of the WLCSP49 package is an additional GND pin.
6. SAM L22N: SERCOM[0:5]. SAM L22G, L22J: SERCOM[0:3].

Related Links

Configuration Summary on page 7
SERCOM USART and I2C Configurations on page 23

7.2. Other Functions

7.2.1. Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing is controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32K Oscillators Controller (OSC32KCTRL).

Table 7-2. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PB22
		XOUT	PB23
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Table 7-3. XOSC32K Jitter Minimization

Package	Steady Signal Recommended
L22N	PB00, PB01, PB02, PB03, PC00, PC01
L22J	PB00, PB01, PB02, PB03, PA02, PA03
L22G	PB02, PB03, PA02, PA03

7.2.2. Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 7-4. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIO	PA30
SWDIO	VDDIO	PA31

7.2.3. SERCOM USART and I²C Configurations

The SAM L22 has up to six instances of the serial communication interface (SERCOM) peripheral. The following table lists the supported communication protocols for each SERCOM instance.

Table 7-5. SERCOM USART and I²C Protocols

	SERCOM Instance					
Protocol	SERCOM0	SERCOM1	SERCOM2	SERCOM3	SERCOM4	SERCOM5
I²C	no	yes	yes	yes	yes	yes
I²C at 3.4MHz	no	yes	no	no	no	yes
USART including RS485 and ISO 7816	yes	yes	yes	yes	yes	yes
SPI	yes	yes	yes	yes	yes	yes

Note: Not all available I²C pins support I²C mode at 3.4MHz.

Figure 8-2. Power Supply Connection for Switching/Linear Mode

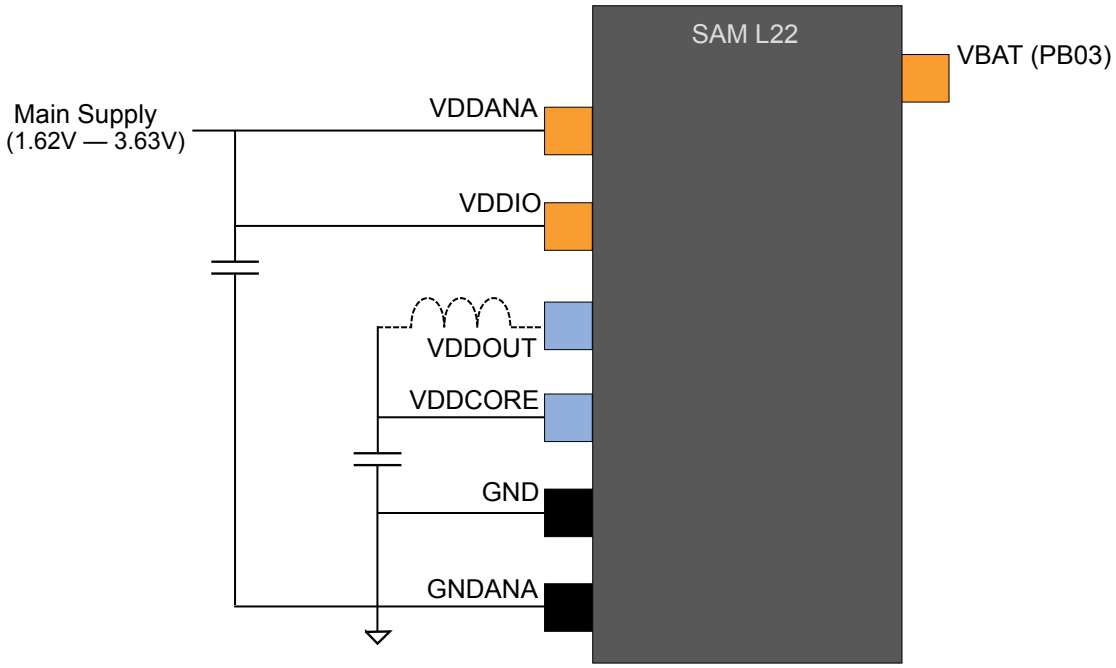
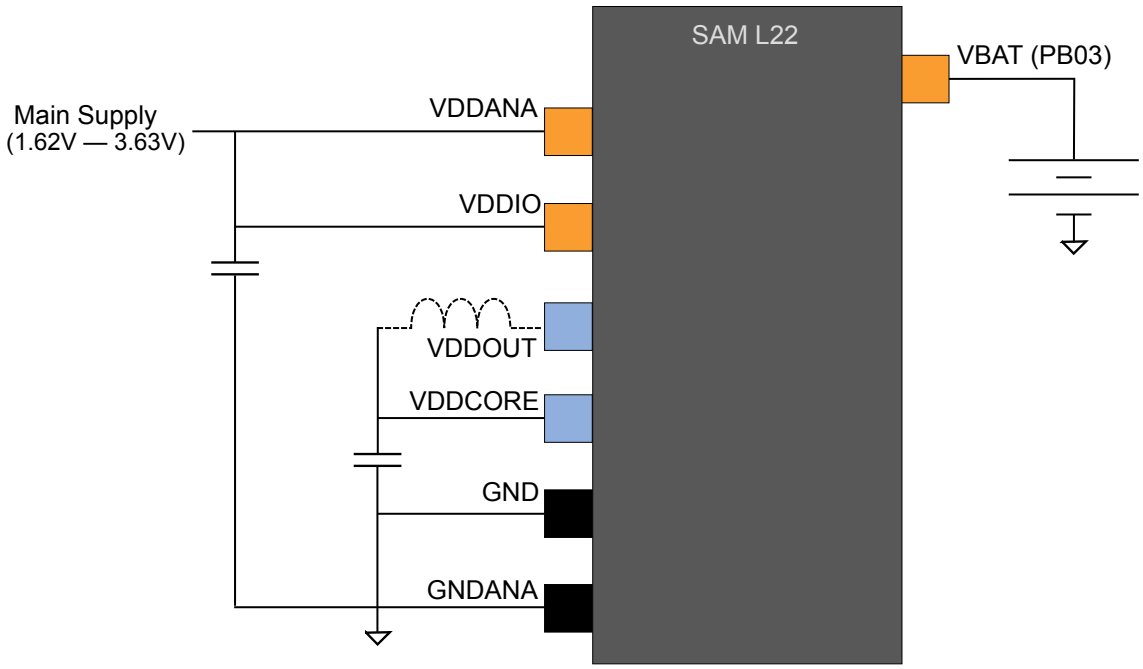


Figure 8-3. Power Supply Connection for Battery Backup



8.2.4. Power-Up Sequence

8.2.4.1. Supply Order

VDDIO and VDDANA must have the same supply sequence. Ideally, they must be connected together.

8.2.4.2. Minimum Rise Rate

One integrated power-on reset (POR) circuits monitoring VDDIO requires a minimum rise rate.

8.2.4.3. Maximum Rise Rate

The rise rate of the power supplies must not exceed the values described in Electrical Characteristics.

10. Memories

10.1. Embedded Memories

- Internal high-speed Flash with Read-While-Write (RWW) capability on a section of the array
- Internal high-speed RAM, single-cycle access at full speed

10.2. Physical Memory Map

The high-speed bus is implemented as a bus matrix. All high-speed bus addresses are fixed, and they are never remapped in any way, even during boot. The 32-bit physical address space is mapped as follows:

Table 10-1. SAM L22 Physical Memory Map

Memory	Start address	Size [KB]		
		SAML22x18(1)	SAML22x17(1)	SAML22x16(1)
Embedded Flash	0x00000000	256	128	64
Embedded RWW section	0x00400000	8	4	2
Embedded SRAM	0x20000000	32	16	8
Peripheral Bridge A	0x40000000	64	64	64
Peripheral Bridge B	0x41000000	64	64	64
Peripheral Bridge C	0x42000000	64	64	64
IOBUS	0x60000000	0.5	0.5	0.5

Note: 1. x = G, J, or E.

Table 10-2. Flash Memory Parameters

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	256	4096	64
SAML22x17(1)	128	2048	64
SAML22x16(1)	64	1024	64

Note: 1. x = G, J, or E.

Table 10-3. RWW Section Parameters(1)

Device	Flash size [KB]	Number of pages	Page size [Bytes]
SAML22x18(1)	8	128	64
SAML22x17(1)	4	64	64
SAML22x16(1)	2	32	64

Note: 1. x = G, J, or E.

11. Processor and Architecture

11.1. Cortex M0+ Processor

The Atmel SAM L22 implements the ARM ARM®Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

11.1.1. Cortex M0+ Configuration

Table 11-1. Cortex M0+ Configuration

Features	Cortex-M0+ options	SAM L22 configuration
Interrupts	External interrupts 0-32	27
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or absent	Present
Number of watchpoint comparators	0, 1, 2	2
Number of breakpoint comparators	0, 1, 2, 3, 4	4
Halting debug support	Present or absent	Present
Multiplier	Fast or small	Fast (single cycle)
Single-cycle I/O port	Present or absent	Present
Wake-up interrupt controller	Supported or not supported	Not supported
Vector Table Offset Register	Present or absent	Present
Unprivileged/Privileged support	Present or absent	Present
Memory Protection Unit	Not present or 8-region	8-region
Reset all registers	Present or absent	Absent
Instruction fetch width	16-bit only or mostly 32-bit	32-bit

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT and DIVAS with 1-cycle loads and stores.

11.1.2. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com)
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late

11.4.3. Configuration

Figure 11-1. Master-Slave Relations High-Speed Bus Matrix

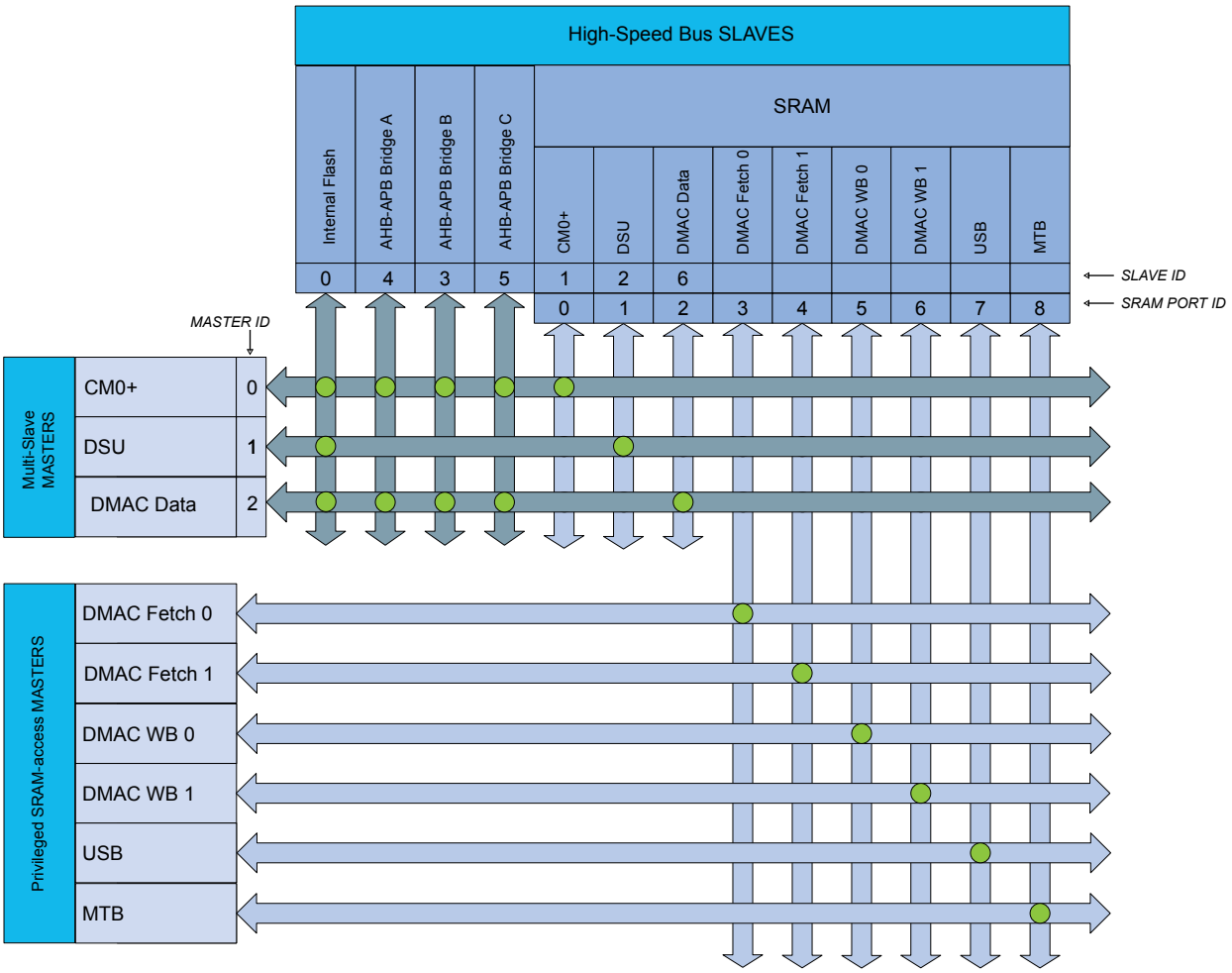


Table 11-4. High Speed Bus Matrix Masters

High-Speed Bus Matrix Masters	Master ID
CM0+ - Cortex M0+ Processor	0
DSU - Device Service Unit	1
DMAC - Direct Memory Access Controller / Data Access	2

Table 11-5. High-Speed Bus Matrix Slaves

High-Speed Bus Matrix Slaves	Slave ID
Internal Flash Memory	0
SRAM Port 0 - CM0+ Access	1
SRAM Port 1 - DSU Access	2
AHB-APB Bridge B	3
AHB-APB Bridge A	4

High-Speed Bus Matrix Slaves	Slave ID
AHB-APB Bridge C	5
SRAM Port 2 - DMAC Data Access	6

11.4.4. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, priority levels can be assigned to the masters for different types of access.

The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM, the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration is shown in the table below.

Table 11-6. Quality of Service

Value	Name	Description
0x0	DISABLE	Background (no sensitive operation)
0x1	LOW	Sensitive Bandwidth
0x2	MEDIUM	Sensitive Latency
0x3	HIGH	Critical Latency

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be a minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by the port ID. The lowest port ID has the highest static priority. See the tables below for details.

The MTB has a fixed QoS level HIGH (0x3).

The CPU QoS level can be written/read, using 32-bit access only, at address 0x4100C114, bits [1:0]. Its reset value is 0x3.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

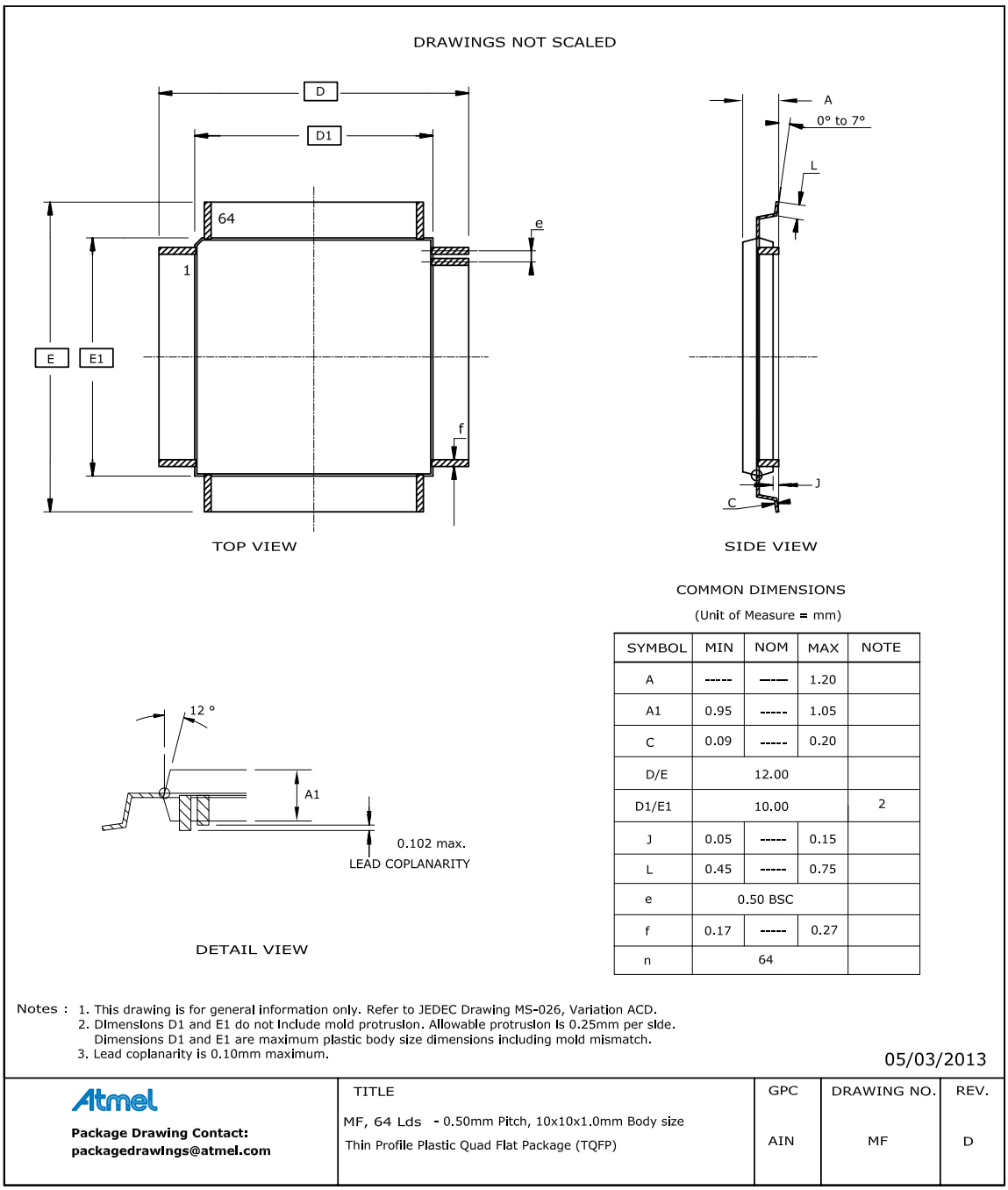
Table 11-7. SRAM Port Connections QoS

SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
CM0+ - Cortex M0+ Processor	0	Bus Matrix	0x4100C114, bits[1:0](1)	0x3
DSU - Device Service Unit	1	Bus Matrix	0x4100201C, bits[1:0](1)	0x2
DMAC - Direct Memory Access Controller - Data Access	2	Bus Matrix	IP-QOSCTRL.DQOS	0x2

SRAM Port Connection	Port ID	Connection Type	QoS	default QoS
DMAC - Direct Memory Access Controller - Fetch Access	3, 4	Direct	IP-QOSCTRL.FQOS	0x2
DMAC - Direct Memory Access Controller - Write-Back Access	5, 6	Direct	IP-QOSCTRL.WRBQOS	0x2
USB - Universal Serial Bus	7	Direct	IP-QOSCTRL	0x3
MTB - Micro Trace Buffer	8	Direct	STATIC-3	0x3

Note: 1. Using 32-bit access only.

12.2.2. 64 pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E		12.00		
D1/E1		10.00		2
J	0.05	-----	0.15	
L	0.45	-----	0.75	
e		0.50 BSC		
f	0.17	-----	0.27	
n		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

Atmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AIN	MF	D

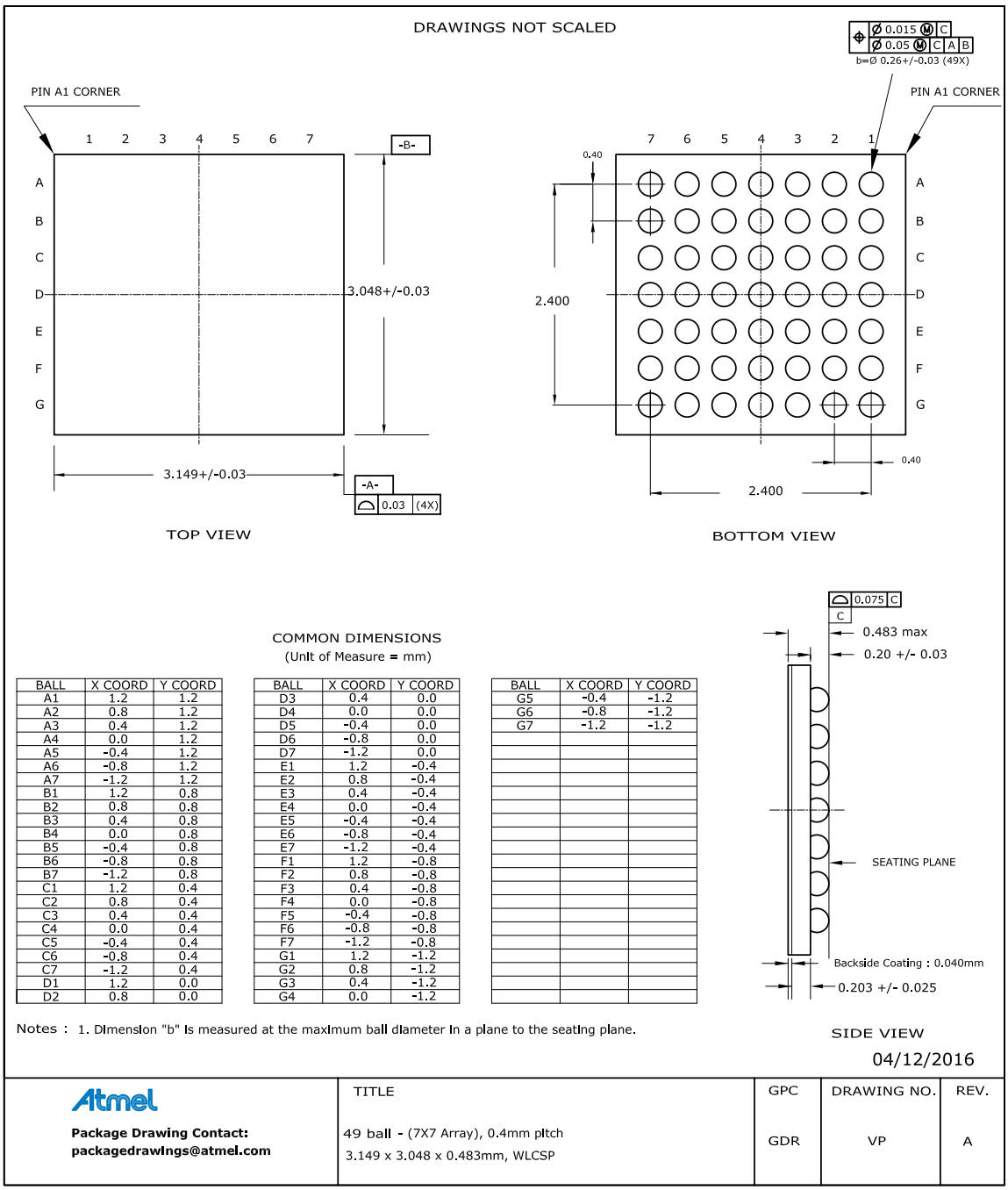
Table 12-5. Device and Package Maximum Weight

300	mg

Table 12-6. Package Characteristics

Moisture Sensitivity Level	MSL3

12.2.4. 49-Ball WLCSP



BALL	X COORD	Y COORD
A1	1.2	1.2
A2	0.8	1.2
A3	0.4	1.2
A4	0.0	1.2
A5	-0.4	1.2
A6	-0.8	1.2
A7	-1.2	1.2
B1	1.2	0.8
B2	0.8	0.8
B3	0.4	0.8
B4	0.0	0.8
B5	-0.4	0.8
B6	-0.8	0.8
B7	-1.2	0.8
C1	1.2	0.4
C2	0.8	0.4
C3	0.4	0.4
C4	0.0	0.4
C5	-0.4	0.4
C6	-0.8	0.4
C7	-1.2	0.4
D1	1.2	0.0
D2	0.8	0.0

BALL	X COORD	Y COORD
D3	0.4	0.0
D4	0.0	0.0
D5	-0.4	0.0
D6	-0.8	0.0
D7	-1.2	0.0
E1	1.2	-0.4
E2	0.8	-0.4
E3	0.4	-0.4
E4	0.0	-0.4
E5	-0.4	-0.4
E6	-0.8	-0.4
E7	-1.2	-0.4
F1	1.2	-0.8
F2	0.8	-0.8
F3	0.4	-0.8
F4	0.0	-0.8
F5	-0.4	-0.8
F6	-0.8	-0.8
F7	-1.2	-0.8
G1	1.2	-1.2
G2	0.8	-1.2
G3	0.4	-1.2
G4	0.0	-1.2

BALL	X COORD	Y COORD
G5	-0.4	-1.2
G6	-0.8	-1.2
G7	-1.2	-1.2

Table 12-11. Device and Package Maximum Weight

8.45	mg

Table 12-12. Package Characteristics

Moisture Sensitivity Level	MSL1