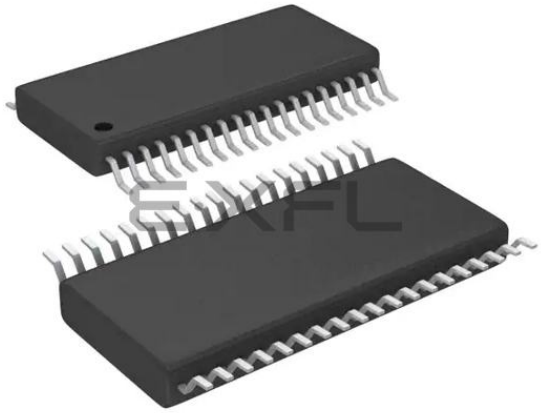

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C800
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	RAM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-c868-1sr-ba

C868

8-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

- One 8-bit and one 5 bits general purpose push-pull I/O ports
  – Enhanced sink current of 10 mA on Port 1/3 (total max current of 43 mA @ 100^{o}C)
- Three 16-bit timers/counters
  –Timer 0 / 1 (C501 compatible)
  –Timer 2 (up/down counter feature)
  –Timer 1 or 2 can be used for serial baudrate generator
- Capture/compare unit for PWM signal generation
  –3-channel, 16-bit capture/compare unit
  –1-channel, 16-bit compare unit
- Full duplex serial interface (UART)
- 5 channel 8-bit A/D Converter
  – Start of conversion can be synchronized to capture/compare timer 12/13.
- 13 interrupt vectors with four priority levels
- Programmable 16-bit Watchdog Timer
- Brown out detection
- Power Saving Modes
  –Slow-down mode
  –Idle mode (can be combined with slow-down mode)
  –Power-down mode with wake up capability through $\overline{\text{INT0}}$ or RxD pins.
- Single power supply of 3.3V, internal voltage regulator for core voltage of 2.5V.
- P-DSO-28-1, P-TSSOP-38-1 packages
- Temperature ranges:
  SAF-C868-1RR BA, SAF-C868-1SR BA, SAF-C868-1RG BA, SAF-C868-1SG BA, SAF-C868A-1RR BA, SAF-C868A-1SR BA, SAF-C868A-1RG BA, SAF-C868A-1SG BA, SAF-C868P-1SR BA, SAF-C868P-1SG BA T_A = – 40 to 85 ^{o}C
  SAK-C868-1RR BA, SAK-C868-1SR BA, SAK-C868-1RG BA, SAK-C868-1SG BA, SAK-C868A-1RR BA, SAK-C868A-1SR BA, SAK-C868A-1RG BA, SAK-C868A-1SG BA, SAK-C868P-1SR BA, SAK-C868P-1SG BA T_A = – 40 to 125 ^{o}C

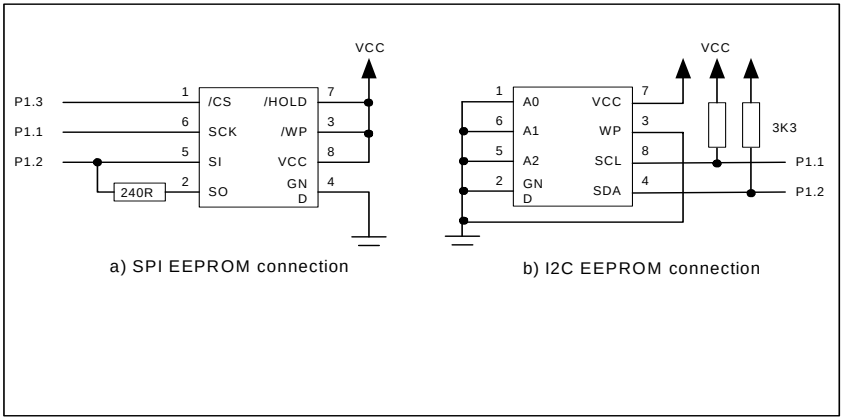

Figure 9 EEPROM connections for a) SPI and b) I2C

Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$**[1]	**00_H**
	ADCON1	A/D Converter Control Register 1	$D9_H$	$XX000000_B$[2]
	ADDATH	A/D Converter Data Register	DB_H	00_H
Ports	P1 [4]	Port 1 Register	**90_H**[1]	**FF_H**
	P1DIR [3]	Port 1 Direction Register	**90_H**[1]	**FF_H**
	P3 [4]	Port 3 Register	**$B0_H$**[1]	**FF_H**
	P3DIR [3]	Port 3 Direction Register	**$B0_H$**[1]	**FF_H**
	P3ALT	Port 3 Alternate Function Register	$B1_H$	00_H
	P1ALT	Port 1 Alternate Function Register	$B4_H$	$XXX00X00_B$[2]
Watchdog	WDTCON	Watchdog Timer Control Register	$A2_H$	$XXXXXX00_B$[2]
	WDTREL	Watchdog Timer Reload Register	$A3_H$	00_H
	WDTL	Watchdog Timer, Low Byte	$B2_H$	00_H
	WDTH	Watchdog Timer, High Byte	$B3_H$	00_H
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$**[1]	**00_H**
	T2MOD	Timer 2 Mode Register	$C9_H$	$XXXXXXX0_B$[2]
	RC2H	Timer 2 Reload/Capture, High Byte	CB_H	00_H
	RC2L	Timer 2 Reload/Capture, Low Byte	CA_H	00_H
	T2H	Timer 2, High Byte	CD_H	00_H
	T2L	Timer 2, Low Byte	CC_H	00_H

1) Bit-addressable special function registers
2) "X" means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Add-ress	Contents after Reset
Cap-ture/ Com-pare Unit	ISSL[3]	Cap/Com Int Status Set Reg, Low Byte	BC_H	00_H
	ISSH[3]	Cap/Com Int Status Set Reg, High Byte	BD_H	00_H
	ISRL[4]	Cap/Com Int Status Reset Reg, Low Byte	BC_H	00_H
	ISRH[4]	Cap/Com Int Status Reset Reg,High Byte	BD_H	00_H
	INPL[3]	Cap/Com Int Node Ptr Reg, Low Byte	BE_H	40_H
	INPH[3]	Cap/Com Int Node Ptr Reg, High Byte	BF_H	39_H
	IENL[4]	Cap/Com Interrupt Register, Low Byte	BE_H	00_H
	IENH[4]	Cap/Com Interrupt Register, High Byte	BF_H	00_H
	CC60SRL	Cap/Com Channel 0 Shadow, Low Byte	FA_H	00_H
	CC60SRH	Cap/Com Channel 0 Shadow, High Byte	FB_H	00_H
	CC61SRL	Cap/Com Channel 1 Shadow, Low Byte	FC_H	00_H
	CC61SRH	Cap/Com Channel 1 Shadow, High Byte	FD_H	00_H
	CC62SRL	Cap/Com Channel 2 Shadow, Low Byte	FE_H	00_H
	CC62SRH	Cap/Com Channel 2 Shadow, High Byte	FF_H	00_H
	CC63SRL	T13 Compare Shadow Reg, Low Byte	$B6_H$	00_H
	CC63SRH	T13 Compare Shadow Reg, High Byte	$B7_H$	00_H
	MODCTRL[3]	Modulation Control Register, Low Byte	$D6_H$	00_H
	MODCTRH[3]	Modulation Control Register, High Byte	$D7_H$	00_H
	TRPCTRL	Trap Control Register, Low Byte	CE_H	00_H
	TRPCTRH	Trap Control Register, High Byte	CF_H	00_H
	PSLRL	Passive State Level Register, Low Byte	$A6_H$	00_H
	MCMOUTL[3]	MCM Output Register, Low Byte	DC_H	00_H
	MCMOUTH[3]	MCM Output Register, High Byte	DD_H	00_H
	MCMOUTSL[4]	MCM Output Shadow Register, Low Byte	DC_H	00_H
	MCMOUTSH[4]	MCM Output Shadow Register,High Byte	DD_H	00_H
	MCMCTRLL[4]	MCM Control Register, Low Byte	$D6_H$	00_H
	T12MSELL	T12 Cap/Com Mode Sel Reg, Low Byte	$F6_H$	00_H
	T12MSELH	T12 Cap/Com Mode Sel Reg, High Byte	$F7_H$	00_H

1) Bit-addressable special function registers
2) "X" means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$E6_H$	T12DTCL	00_H		–	DTM5	DTM4	DTM3	DTM2	DTM1	DTM0
$E7_H$	T12DTCH	00_H	–	DTR2	DTR1	DTR0	–	DTE2	DTE1	DTE0
$E8_H$	PMCON1	$XXXX\ X000_B$	–	–	–	–	–	CCUDIS	T2DIS	ADCDIS
EA_H	CMPMODIFL	00_H	–	MCC63S	–	–	–	MCC62S	MCC61S	MCC60S
EB_H	CMPMODIFH	00_H	–	MCC63R	–	–	–	MCC62R	MCC61R	MCC60R
EC_H	T12L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
ED_H	T12H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
EE_H	T13L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
EF_H	T13H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F2_H$[2)]	TCTR4L	00_H	T12STD	T12STR	–	–	DTRES	T12RES	T12RS	T12RR
$F2_H$[3)]	TCTR2L	00_H	–	T13TED1	T13TED0	T13TEC2	T13TEC1	T13TEC0	T13SSC	T12SSC
$F3_H$[2)]	TCTR4H	00_H	T13STD	T13STR	–	–	–	T13RES	T13RS	T13RR
$F4_H$	CMPSTATL	00_H	–	CC63ST	–	–	–	CC62ST	CC61ST	CC60ST
$F5_H$	CMPSTATH	00_H	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
$F6_H$	T12MSELL	00_H	MSEL613	MSEL612	MSEL611	MSEL610	MSEL603	MSEL602	MSEL601	MSEL600
$F7_H$	T12MSELH	00_H	–	–	–	–	MSEL623	MSEL622	MSEL621	MSEL620

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Timer/Counter 2 with Compare/Capture/Capture

Timer 2 is a 16-bit timer/counter with an up/down count feature. It has three operating modes:

- 16-bit auto-reload mode (up or down counting)
- 16-bit capture mode
- Baudrate generator

Table 9 Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	T2EX	Remarks	System Clock	
	RCLK or TCLK	CP/$\overline{RL2}$	TR2	DCEN	EXEN			Inte-rnal	T2
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{SYS} /12	max f_{SYS} /24
	0	0	X	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	down counting		
	0	0	1	1	X	1	up counting		
16-bit Capture	0	1	1	X	0	X	16-bit Timer/ Counter (only up-counting)	f_{SYS} /12	max f_{SYS} /24
	0	1	1	X	1	↓	capture T2H,T2L-> RC2H,RC2L		
Baudrate Generator	1	X	1	X	0	X	no overflow interrupt request(TF2)	f_{SYS} /2	-
	1	X	1	X	1	↓	extra external interrupt (“Timer 2“)		
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note: denotes a falling edge

Switching Examples

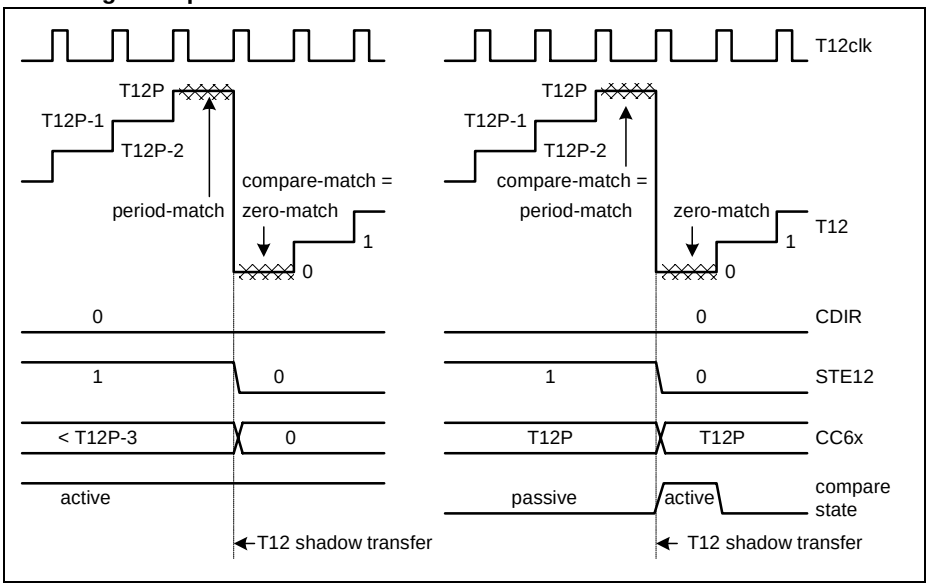

Figure 16 Edge-aligned mode with duty cycles near 100% and near 0%. Applicable to T13 as well.

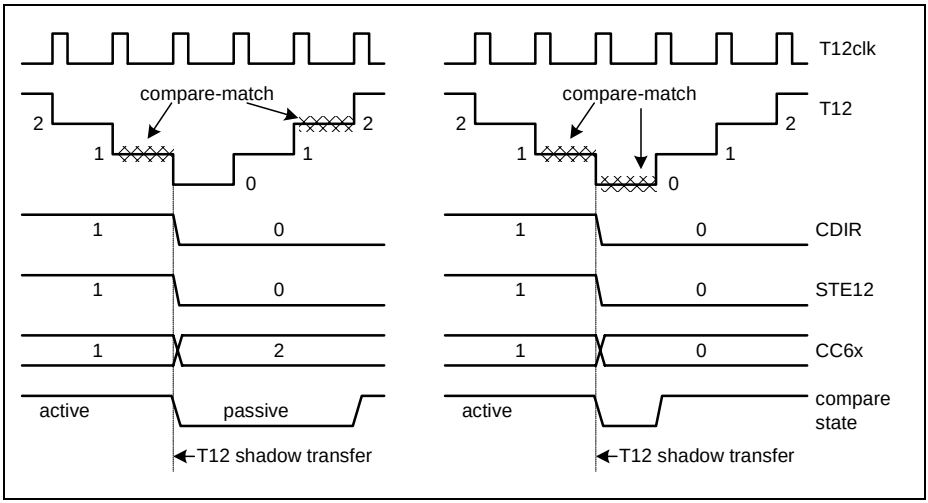

Figure 17 Centre-aligned mode with duty cycles near 100% and near 0%.

Dead-time Generation

The dead-time generation logic is built in a similar way for all three channels of T12. Each of the three channels works independently with its own dead-time counter and the trigger and enable signals.

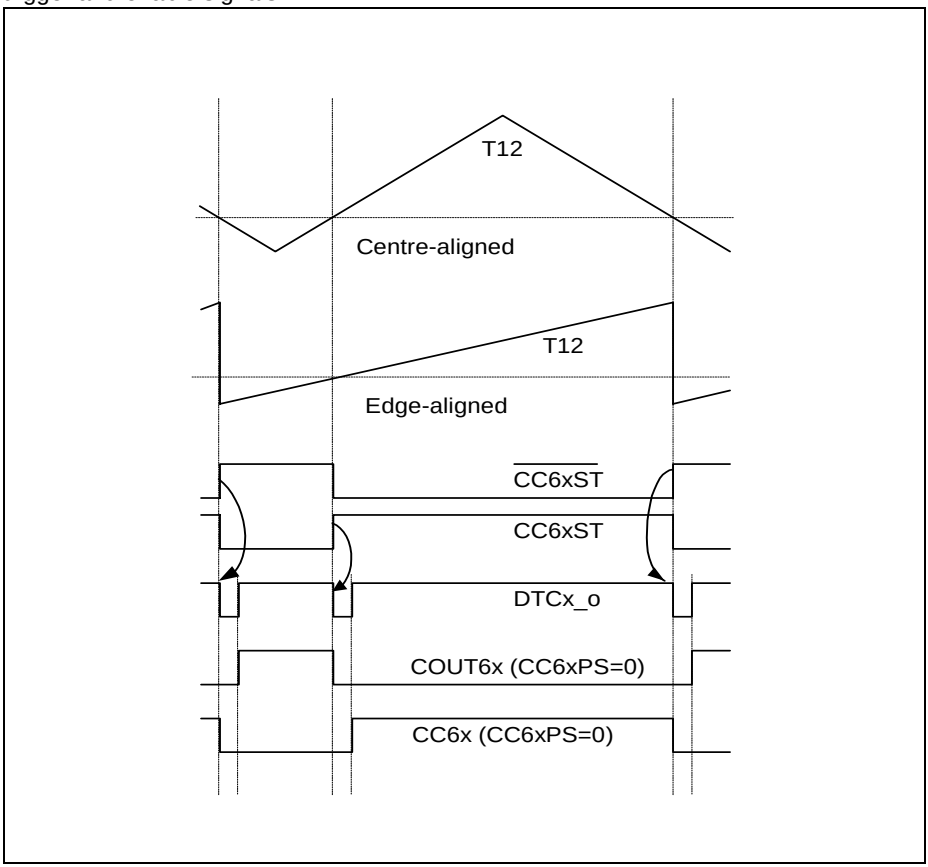

Figure 18 Dead-time generation for centre and edge aligned modes

Capture Mode

In capture mode the bits CC6xST indicate the occurrence of the selected capture event according to the bit fields MSEL6x. A rising and/or a falling edge on the pins CC6x can be selected as capture event, that is used to transfer the contents of timer T12 to the CC6xR and CC6xSR registers. In order to work in capture mode, the capture pins have to be configured as inputs.

Hall Sensor Mode

In **Brushless-DC motors** the next multi-channel state values depend on the pattern of the Hall inputs. There is a strong correlation between the **Hall pattern** (CURH) and the **modulation pattern** (MCMP). Because of different machine types the modulation pattern for driving the motor can be different. Therefore it is wishful to have a wide flexibility in defining the correlation between the Hall pattern and the corresponding modulation pattern. The CCU6 offers this by having a register which contains the actual Hall pattern (CURHS), the next expected Hall pattern (EXPHS) and its output pattern (MCMPS). At every correct Hall event (CHE, see figure *Hall Event Actions*) a new Hall pattern with its corresponding output pattern can be loaded (from a predefined table) by software into the register MCMOUTS. Loading this shadow register can also be done by a write action on MCMOUTS with bit STRHP = '1'

The **sampling** of the Hall pattern (on CCPOSx) is done with the T12 clock. By using the dead-time counter DTC0 (mode MSEL6x= '1000') a hardware **noise filter** can be implemented to suppress spikes on the Hall inputs due to high di/dt in rugged inverter environment. In case of a Hall event the DTC0 is reloaded and starts counting. When the counter value of one is reached, the CCPOSx inputs are sampled (without noise and spikes) and are compared to the current Hall pattern (CURH) and to the expected Hall pattern (EXPH). If the sampled pattern equals to the current pattern the edge on CCPOSx was due to a noise spike and no action will be triggered (implicit noise filter). If the sampled pattern equals to the next expected pattern the edge on CCPOSx was a correct Hall event, the bit CHE is set which causes an interrupt and the resets T12 (for speed measurement, see description mode '1000' below).

This correct Hall event can be used as a transfer request event for register MCMOUTS. The transfer from MCMOUTS to MCMOUT transfers the new CURH-pattern as well as the next EXPH-pattern. In case of the sampled Hall inputs were neither the current nor the expected Hall pattern, the bit WHE (wrong Hall event) is set which also can cause an interrupt and sets the IDLE mode clearing MCMP (modulation outputs are inactive). To restart from IDLE the transfer request of MCMOUTS have to be initiated by software (bit STRHP and bitfields SWSEL/SWSYN).

A/D Converter

The C868 includes a high performance / high speed 8-bit A/D-Converter (ADC) with 5 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 5 multiplexed input channels, which can also be used as digital inputs
- 8-bit resolution with TUE of +/- 2 LSB8.
- Single or continuous conversion mode
- Start of conversion by software and hardware
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Powerdown in normal, idle and slow-down modes

The ADC supports two conversion modes - single and continuous conversions. For each mode, there are two ways in which conversion can be started - by software and by the T13PM signal from the CCU module.

Writing a ‘0’ to bit CCU_ADEX select conversion control by ADST. Writing a ’1’ to bit field ADST starts conversion on the channel that is specified by ADCH. In single conversion mode, bit field ADM is cleared to ’0’. This is the default mode selected after hardware reset. When a conversion is started, the channel specified is sampled. The busy flag ADBSY is set and ADST is cleared. When the conversion is completed, the interrupt request signal ADCIRQ is asserted possitively for 2 clocks and the 8-bit result together with the number of the converted channel is transferred to the result register ADDATH.

In continuous conversion mode, bit field ADM is set to ’1’. In this mode, the ADC repeatedly converts the channel specified by ADCH. Bit ADST is cleared at the beginning of the first conversion. The busy flag ADBSY is asserted until the last conversion is completed. At the end of each conversion, the interrupt request signal ADCIRQ will be activated. To stop conversion, ADM has to be reset by software. If the channel number ADCH is changed while continuous conversion is in progress, the new channel specified will be sampled in the conversions that follow.

A new request to start conversion will be allowed only after the completion of any conversion that is in progress.

Writing a ‘1’ to bit CCU_ADEX select conversion control by T13PM trigger signal from the CCU module.

Note: Caution must be taken when changing conversion start source. To change conversion source from software to hardware trigger, it is best to let remaining software conversion to complete before changing. To change conversion source from hardware trigger to software, it is best to change source first, let any

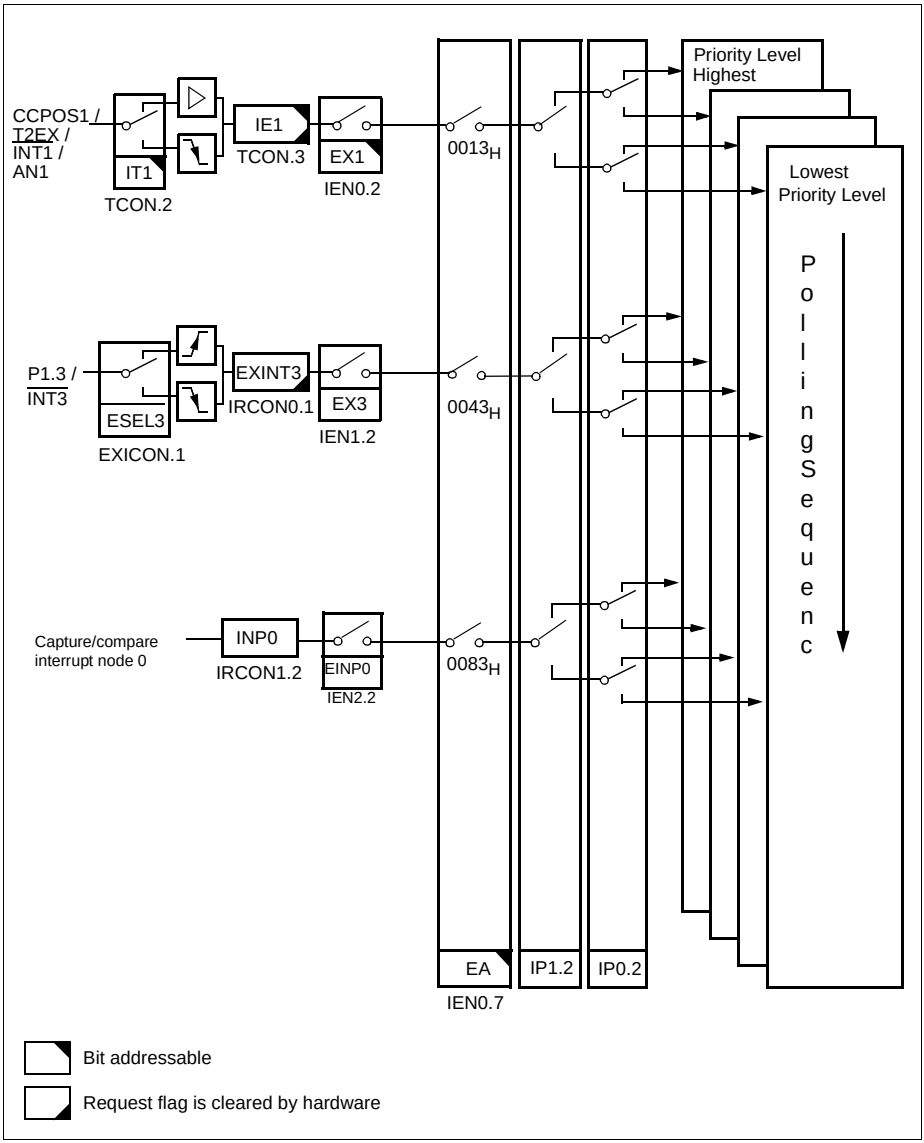

Figure 25 Interrupt Structure, Overview Part 2

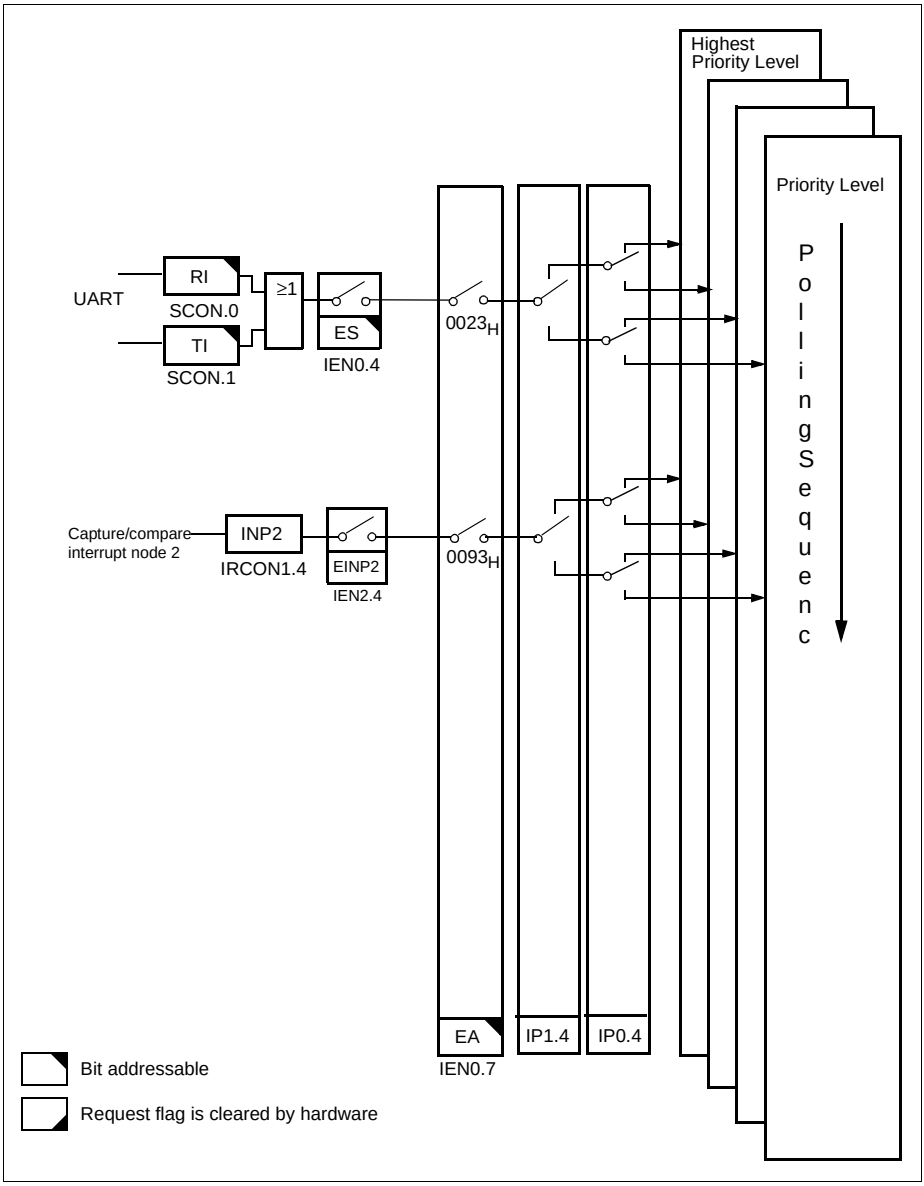

Figure 27 Interrupt Structure, Overview Part 4

Table 15 Power Saving Modes Overview

Mode	Entering	Leaving by	Remarks
Idle Mode	ORL PCON,#01_H	Occurance of any enabled interrupt Hardware Reset	CPU clock is stopped; CPU maintains its data; peripheral units are active (if enabled) and provided with clock
Slow Down Mode	In normal mode: ORL PCON,#10_H	ANL PCON,#$0EF_H$ or Hardware Reset	Internal clock rate is reduced to a configurable factor of $^1/_2$ to $^1/_{32}$ of the system clock rate
	With idle mode: ORL PCON,#11_H	Occurance of any enabled interrupt to exit idle mode and the instruction ANL PCON,#$0EF_H$ to terminate slow down mode Hardware Reset	CPU clock is stopped; CPU maintains all its data; Peripheral units are active (if enabled) and provided with a configurable factor of $^1/_2$ to $^1/_{32}$ of the system clock rate
Software Power Down mode	With external wake-up capability from power down enabled ORL PMCON0,#01_H (to wake-up via pin $\overline{INT0}$) or ORL PMCON0,#03_H (to wake-up via pin RxD) ORL PCON,#02_H	Hardware Reset When $\overline{INT0}$ or RxD goes low for at least 10 µs (latch phase). But it is desired that the corresponding pin must be held at high level during the power down mode entry and up to the wake-up.	Oscillator is stopped; Contents of on-chip RAM and SFR's are maintained
	With external wake-up capability from power down disabled ORL PCON,#02_H	Hardware Reset	

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C868. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DDP}	3.0	3.6	V	Active mode, f_{SYSmax} = 40 MHz
		tbd	3.6	V	PowerDown mode[1]
Digital ground voltages	V_{SSC}, V_{SSP}	0		V	-
Ambient temperature	T_A	-40	85	°C	SAF-C868...
		-40	125	°C	SAK-C868...
Analog reference voltage	V_{AREF}	3.0V	V_{DDP} + 0.1	V	-
Analog ground voltage	V_{AGND}	V_{SSP} - 0.1	V_{SSP} + 0.1	V	-
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	-
External Clock	f_{OSC}	6.67	10.67	MHz	-
Input current on any pin during overload condition except int/ analog and XTAL	I_{OV0}	-5	5	mA	-[2)3)]
int/analog pin	I_{OV1}	-2	5	mA	-[3)4)]
XTAL pin	I_{OV2}	-5	5	mA	-[3)5)]
Absolute sum of all input currents during overload condition	ΣI_{OV}	-	|20|	mA	-[3)]

Notes:

1) Oscillator or external clock disabled.

2) Overload conditions under operating conditions occur if the voltage on the respective pin exceeds the specified operating range (i.e. $V_{OV} > V_{DDP}$ +0.5V or $V_{OV} < V_{SSP}$ -0.5V). The absolute sum of input currents on all port pins may not exceed 20mA. The suply voltages V_{DDP} and V_{SSP} must remain within the specified limits.

3) Not 100% tested, but guaranteed by design characterization.

DC Characteristics

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages all except XTAL2, int/analog int/analog XTAL2	 V_{IL0} V_{IL1} V_{IL2}	 -0.5 -0.5 -0.5	 $0.3V_{DDP}$ $0.3V_{DDC}$ $0.1V_{DDC}$	 V V V	–[1]
Input high voltages all except XTAL2, int/analog int/analog XTAL2	 V_{IH0} V_{IH1} V_{IH2}	 $0.7V_{DDP}$ $0.7V_{DDC}$ $0.7V_{DDC}$	 V_{DDP}+0.5 V_{DDP}+0.5 V_{DDC}+0.5	 V V V	–
Output low voltage	V_{OL}	–	0.45	V	SAF-C868... I_{OL}=10mA
		–	0.55	V	SAK-C868... I_{OL}=10mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH}=10mA
Input leakage current (all except int/analog)	I_{LI0}	–	±0.5	uA	$0.4<V_{IN}<V_{DDP}$
Input leakage current (int/ analog)	I_{LI1}	–	±0.5	uA	$0.4<V_{IN}<V_{DDP}$[2]
Input low current (XTAL2)	I_{LI2}	–	±10	uA	$0.4<V_{IN}<V_{DDC}$
Digital supply voltage	V_{DDC}	2.25[3]	2.75	V	–
Blocking capacitor for V_{DDC}		136	470	nF	–[4]
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A= 25°C

Note:

1) Interrupt/analog pins are input only and has CMOS characteristics whereas the other I/O pins have TTL characteristics.

2) The leakage current of interrupt/analog pins depends on the leakage current of the CMOS pad for the digital functions and the analog pad.

3) The V_{DDC} is measured under the following conditions:

Microcontroller in power down mode;$\overline{\text{RESET}}$ = V_{DDP}; XTAL2 = V_{SSC}; XTAL1 = N.C.; V_{AGND}= V_{SSP}; V_{AREF}= V_{DDP}; RxD/INT0 = V_{DDP}; all other pins are set to input and connected to gnd; ALE output disabled and connected to gnd; 20mA current sourced from the V_{DDC} pin.

4) Ceramic type (±20%) max ESR: 25mΩ ,max trace length to capacitor is 10mm.

4) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

5) Not 100% tested, but guaranteed by design characterization.

Clock calculation table for ADC

TVC[1]	32								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	322	386	450	514	578	642	706	770	t_{SYS}
t_S	64	128	192	256	320	384	448	512	t_{SYS}

TVC[1]	28								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	282	338	394	450	506	562	618	674	t_{SYS}
t_S	56	112	168	224	280	336	392	448	t_{SYS}

TVC[1]	24								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	242	290	338	386	434	482	530	578	t_{SYS}
t_S	48	96	144	192	240	288	336	384	t_{SYS}

TVC[1]	20								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	202	242	282	322	362	402	442	482	t_{SYS}
t_S	40	80	120	160	200	240	280	320	t_{SYS}

TVC[1]	16								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	162	194	226	258	290	322	354	386	t_{SYS}
t_S	32	64	96	128	160	192	224	256	t_{SYS}

TVC[1]	12								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	122	146	170	194	218	242	266	290	t_{SYS}
t_S	24	48	72	96	120	144	168	192	t_{SYS}

AC Characteristics

(Operating Condition Apply)

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Ext Clock 6.67 to 10.67 MHz		
		min	max	
Oscillating period	t_{OSC}	93.75	150	ns
High time	t_1	46.875	75	ns
Low time	t_2	46.875	75	ns
Rise time	t_R	-	10	ns
Fall time	t_F	-	10	ns

ALE Characteristics

Parameter	Symbol	Limit Values		Unit
		System freq = 6.25MHz to 40MHz Duty Cycle 0.5		
		min	max	
ALE pulse width	t_{AWD}	50	320	ns
ALE period	t_{ACY}	150	960	ns

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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