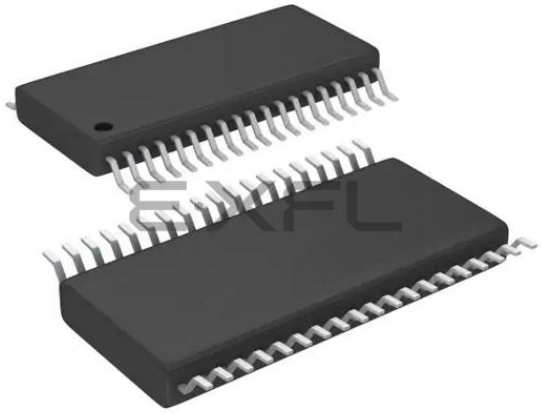

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C800
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	RAM
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-c868p-1sr-ba

C868

8-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Revision History: **2003-05** V 1.0

Previous Version: -

Page	Subjects (major changes since last revision)
	Current data updated
	Description of I2C included

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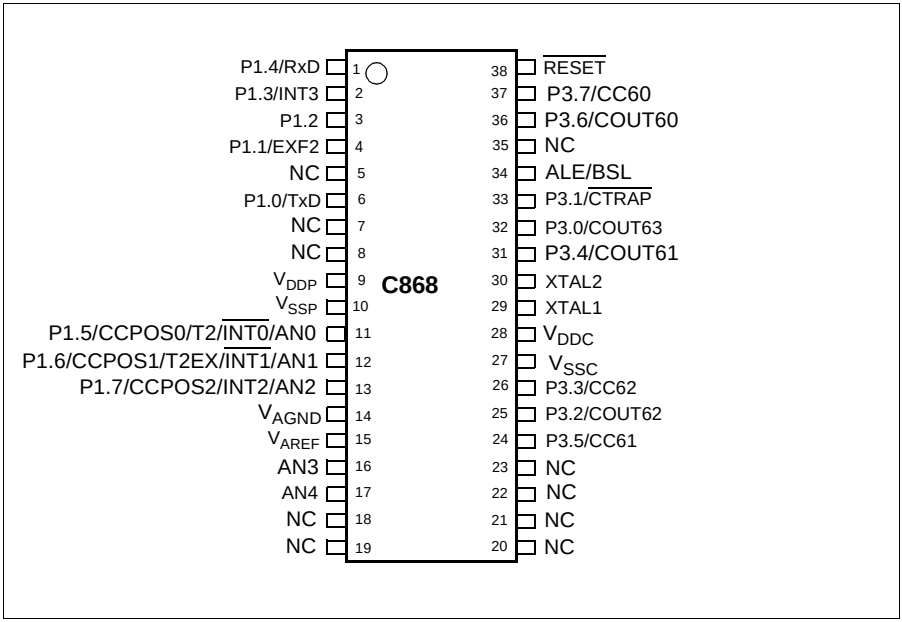

Figure 3 C868 Pin Configuration P-TSSOP-38 Package (top view)

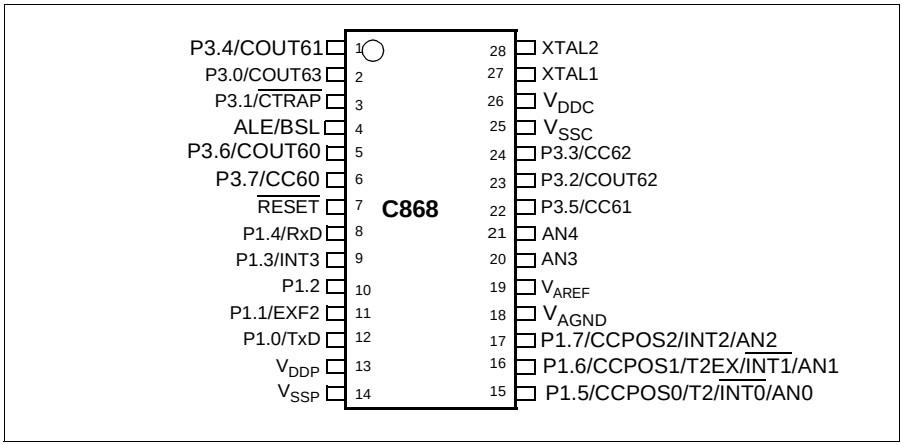

Figure 4 C868 Pin Configuration P-DSO-28 Package (top view)

Memory Organization

The C868 CPU manipulates operands in the following five address spaces:

- up to 8 Kbyte of RAM internal program memory : 8K ROM for C868-1R
  : 8K RAM for C868-1S
- 4 Kbyte of internal Self test and Boot ROM
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- 128 byte special function register area

Figure 0-1 illustrates the memory address spaces of the C868.

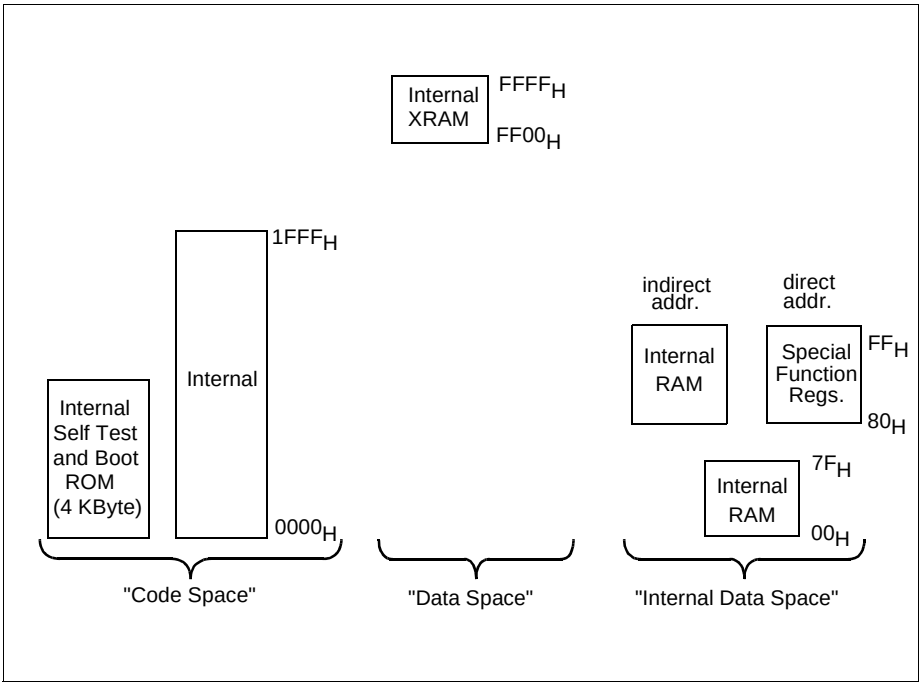

Figure 0-1 C868 Memory Map

The PLL output frequency is determined by:

$$f_{PLL} = f_{VCO} / K = \frac{15}{K} \times f_{OSC} \quad [1]$$

The range for the VCO frequency is given by:

$$100\ MHz \leq f_{VCO} \leq 160\ MHz \quad [2]$$

The relationship between the input frequency and VCO frequency is given by:

$$f_{VCO} = 15 \times f_{OSC} \quad [3]$$

This gives the range for the input frequency which is given by:

$$6.67\ MHz \leq f_{OSC} \leq 10.67\ MHz \quad [4]$$

Table 5 Output Frequencies f_{PLL} Derived from Various Output Factors

K-Factor		f_{PLL}		Duty Cycle [%]	Jitter
Selected Factor	**KDIV**	**f_{VCO} = 100 MHz**	**f_{VCO} = 160 MHz**		
2	000_B	50	80	50	linear depending on f_{VCO} at f_{VCO} =100MHz: +/-300ps at f_{VCO} =160MHz: +/-250ps additional jitter for odd Kdiv factors tbd.
4	010_B	25	40	50	
5[1)]	011_B	20	32	40	
6	100_B	16.67	26.67	50	
8	101_B	12.5	20	50	
9[1)]	110_B	11.11	17.78	44	
10	111_B	10	16	50	
16	001_B	6.25	10	50	

1) These odd factors should not be used (not tested because off the unsymmetrical duty cycle).

2) Shaded combinations should not be used because they are above the maximum CPU frequency of 40MHz.

Figure 12 shows the recommended oscillator circuitries for crystal and external clock operation.

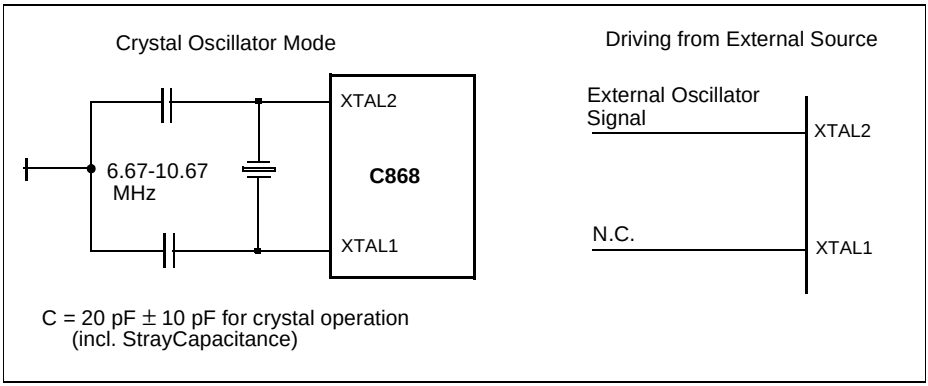

Figure 12 Recommended Oscillator Circuit

In this application the on-chip oscillator is used as a crystal-controlled, positive-reactance oscillator (a more detailed schematic is given in **Figure 13**). It is operated in its fundamental response mode as an inductive reactor in parallel resonance with a capacitor external to the chip. The crystal specifications and capacitances are non-critical. In this circuit tbd pF can be used as single capacitance at any frequency together with a good quality crystal. A ceramic resonator can be used in place of the crystal in cost-critical applications. If a ceramic resonator is used, the two capacitors normally have different values depending on the oscillator frequency. We recommend consulting the manufacturer of the ceramic resonator for value specifications of these capacitors.

Table 6 Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Capture/ Compare Unit	T12L	Timer T12 Counter Register, Low Byte	EC_H	00_H
	T12H	Timer T12 Counter Register, High Byte	ED_H	00_H
	T13L	Timer T13 Counter Register, Low Byte	EE_H	00_H
	T13H	Timer T13 Counter Register, High Byte	EF_H	00_H
	T12PRL	Timer T12 Period Register, Low Byte	DE_H	00_H
	T12PRH	Timer T12 Period Register, High Byte	DF_H	00_H
	T13PRL	Timer T13 Period Register, Low Byte	$D2_H$	00_H
	T13PRH	Timer T13 Period Register, High Byte	$D3_H$	00_H
	CC60RL	Capture/Compare Ch 0 Reg, Low Byte	$C2_H$	00_H
	CC60RH	Capture/Compare Ch 0 Reg, High Byte	$C3_H$	00_H
	CC61RL	Capture/Compare Ch 1 Reg, Low Byte	$C4_H$	00_H
	CC61RH	Capture/Compare Ch 1 Reg, High Byte	$C5_H$	00_H
	CC62RL	Capture/Compare Ch 2 Reg, Low Byte	$C6_H$	00_H
	CC62RH	Capture/Compare Ch 2 Reg, High Byte	$C7_H$	00_H
	CC63RL	T13 Compare Register, Low Byte	$D4_H$	00_H
	CC63RH	T13 Compare Register, High Byte	$D5_H$	00_H
	T12DTCL	Timer T12 Dead Time Ctrl, Low Byte	$E6_H$	00_H
	T12DTCH	Timer T12 Dead Time Ctrl, High Byte	$E7_H$	00_H
	CMPSTATL	Compare Timer Status, Low Byte	$F4_H$	00_H
	CMPSTATH	Compare Timer Status, High Byte	$F5_H$	00_H
	CMPMODIFL	Compare Timer Modification, Low Byte	EA_H	00_H
	CMPMODIFH	Compare Timer Modification, High Byte	EB_H	00_H
	TCTR0L	Timer Control Register 0, Low Byte	$E2_H$	00_H
	TCTR0H	Timer Control Register 0, High Byte	$E3_H$	00_H
	TCTR2L[3]	Timer Control Register 2, Low Byte	$F2_H$	00_H
	TCTR4L[4]	Timer Control Register 4, Low Byte	$F2_H$	0_H
	TCTR4H[4]	Timer Control Register 4, High Byte	$F3_H$	00_H
	ISL	Cap/Com Interrupt Register, Low Byte	$E4_H$	00_H
	ISH	Cap/Com Interrupt Register, High Byte	$E5_H$	00_H
	PISELH	Port Input Selector Register, High Byte	BB_H	00_H

1) Bit-addressable special function registers
2) "X" means that the value is undefined and the location is reserved
3) Register is mapped by bit RMAP in SYSCON0.4=1
4) Register is mapped by bit RMAP in SYSCON0.4=0

Table 7 Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$A2_H$	WDTCON	$XXXX\ XX00_B$	–	–	–	–	–	–	–	WDTIN
$A3_H$	WDTREL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$A6_H$	PSLRL	00_H	PSL63	–	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
$A8_H$	IEN0	$0X00\ 0000_B$	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IEN1	$XXXX\ X000_B$	–	–	–	–	–	EX3	EX2	EADC
AA_H	IEN2	$XX00\ 00XX_B$	–	–	EINP3	EINP2	EINP1	EINP0	–	–
AC_H	IP1	$XX00\ 0000_B$	–	–	.5	.4	.3	.2	.1	.0
AD_H	SYSCON0	$XX10\ XXX1_B$	–	–	EALE	RMAP	–	–	–	XMAP0
AF_H	SYSCON1	$00XX\ X0X0_B$	ESWC	SWC	_	_	_	BSLEN	_	SWAP
$B0_H$[2]	P3	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$B0_H$[3]	P3DIR	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$B1_H$	P3ALT	00_H	CC60	COUT60	CC61	COUT61	CC62	COUT62	CTRAP	COUT63
$B2_H$	WDTL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$B3_H$	WDTH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$B4_H$	P1ALT	$XXX0\ 0X00_B$	_	_	_	RxD	INT3	_	EXF2	TxD
$B6_H$	CC63SRL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$B7_H$	CC63SRH	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) This register is mapped with RMAP (SYSCON0.4)=0
3) This register is mapped with RMAP (SYSCON0.4)=1
Shaded registers are bit-addressable special function registers

Ports

The C868 has two kinds of ports. The first kind is push-pull ports instead of the traditional quasi-bidirectional ports. The ports belonging to this kind are lsb of port 1 which is a 5-bit I/O port and port 3 which is an eight-bit I/O port. When configured as inputs, these ports will be high impedance with Schmitt trigger feature. Port 3 is alternate for capture/compare functions whereas, port 1 has alternate functions for some of the pins.

The second kind is input ports which are shared by msb of port 1 which is a 3-bit input port, the interrupts, timer 2 inputs, capture/compare hall inputs and analog inputs.

Timer 0 and 1

Timer 0 and 1 can be used in four operating modes as listed in **Table 8**:

Table 8 Timer 0 and 1 Operating Modes

Mode	Description	TMOD		System Clock
		M1	M0	
0	8-bit timer with a divide-by-32 prescaler	0	0	f_{SYS}/(12*32)
1	16-bit timer	0	1	f_{SYS}/12
2	8-bit timer with 8-bit autoreload	1	0	
3	Timer 0 used as one 8-bit timer and one 8-bit timer timer 1 stops	1	1	

The register is incremented every machine cycle. Since the machine cycle consist of twelve oscillator periods, the count rate is 1/12th of the system frequency. External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate to facilitate pulse width measurements. **Figure 15** illustrates the input clock logic.

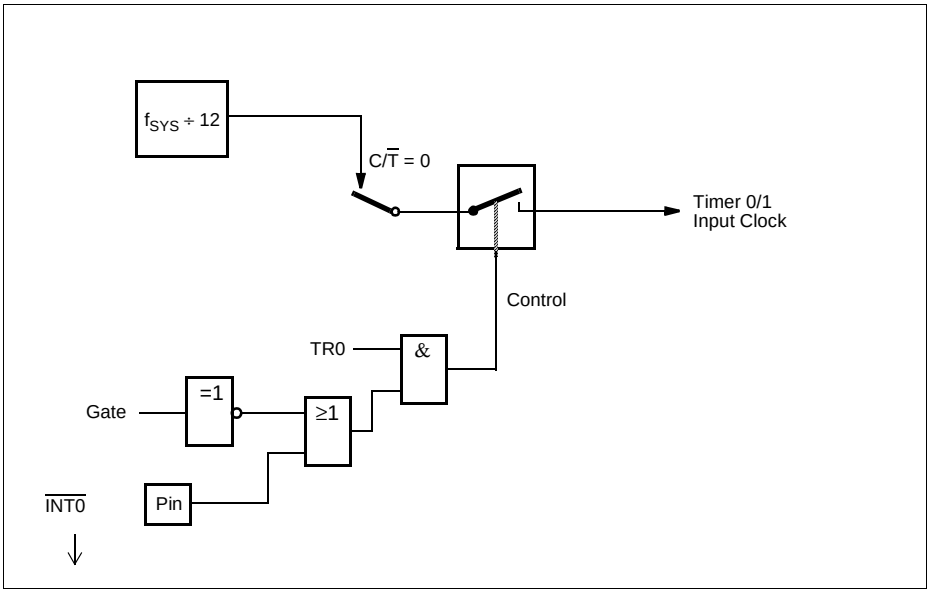

Figure 15 Timer 0 and 1 Input Clock Logic

Trap Handling

The trap functionality permits the PWM outputs to react on the state of the input pin CTRAP. This functionality can be used to switch off the power devices if the trap input becomes active (e.g. as emergency stop).

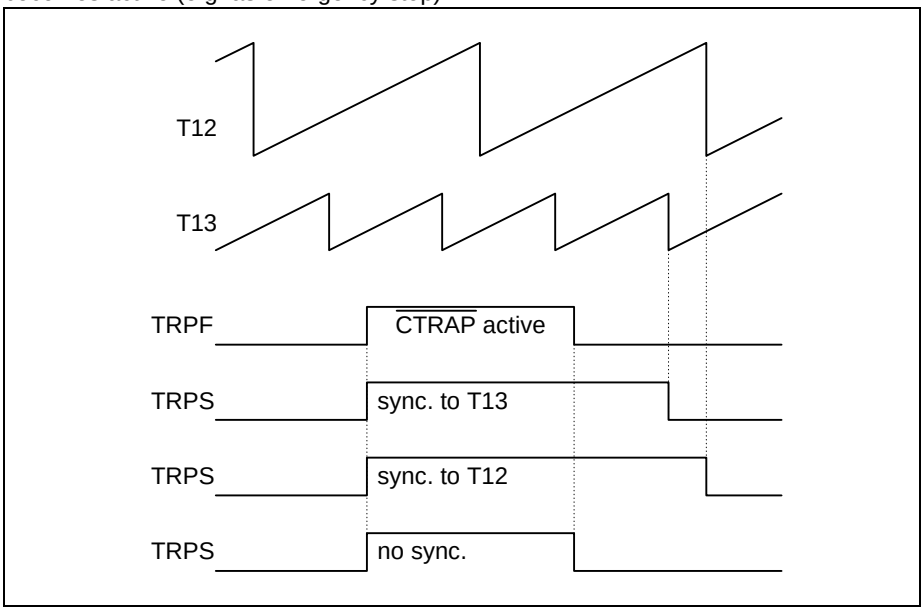

Figure 21 Trap State Synchronization (with TRM2='0')

For **Brushless-DC** motors there is a special mode (MSEL6x = ’1000b’) which is triggered by a change of the Hall-inputs (CCPOSx). This mode shows the capabilities of the CCU6. Here T12’s channel 0 acts in capture function, channel 1 and 2 in compare function (without output modulation) and the multi-channel-block is used to trigger the output switching together with a possible modulation of T13.
After the detection of a valid Hall edge the T12 count value is captured to channel 0 (representing the actual motor speed) and resets the T12. When the timer reaches the compare value in channel 1, the next multi-channel state is switched by triggering the shadow transfer of bit field MCMP (if enabled in bit field SWEN). This trigger event can be combined with several conditions which are necessary to implement a noise filtering (correct Hall event) and to synchronize the next multi-channel state to the modulation sources (avoiding spikes on the output lines). This compare function of channel 1 can be used as a phase delay for the position input to the output switching which is necessary if a sensorless back-EMF technique is used instead of Hall sensors. The compare value in channel 2 can be used as a time-out trigger (interrupt) indicating that the motors destination speed is far below the desired value which can be caused by a abnormal load change. In this mode the modulation of T12 has to be disabled (T12MODENx = ’0’).

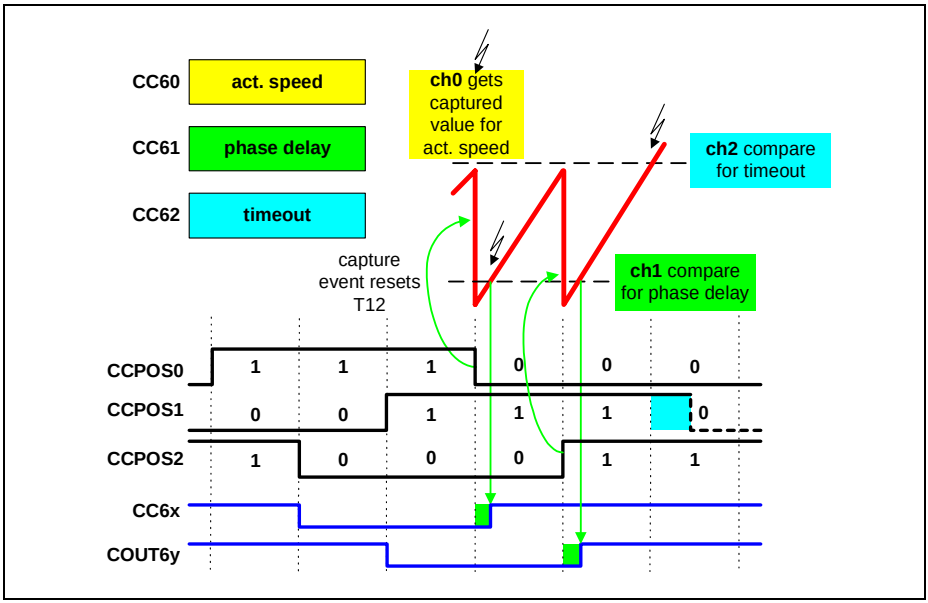

Figure 0-2 Timer T12 Brushless-DC Mode (MSEL6x = 1000)

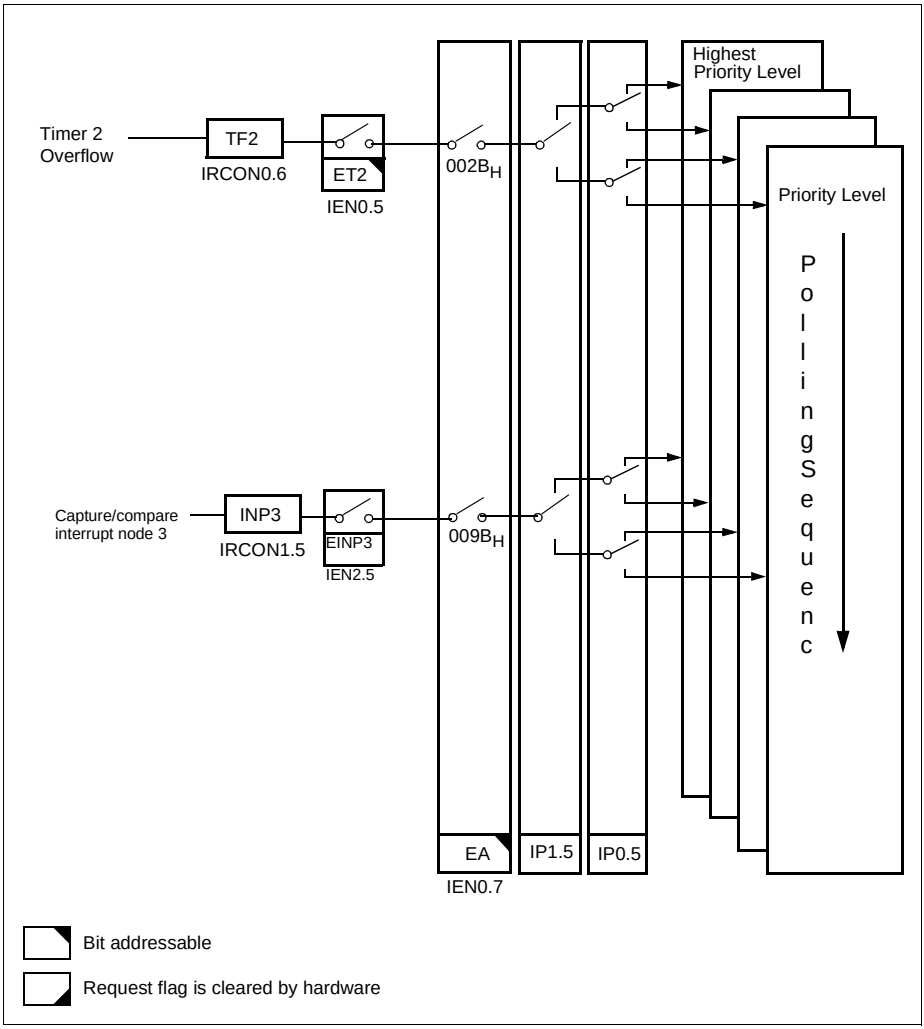

Figure 28 Interrupt Structure, Overview Part 5

Fail Save Mechanisms

The C868 offers enhanced fail save mechanisms, which allow an automatic recovery from software upset or hardware failure :

a programmable watchdog timer (WDT), with variable time-out period from 12.8µs to 819.2µs at f_{SYS} = 40 MHz.

Programmable Watchdog Timer

To protect the system against software failure, the user's program has to clear this watchdog within a previously programmed time period. If the software fails to do this periodical refresh of the watchdog timer, an internal reset will be initiated. The software can be designed so that the watchdog times out if the program does not work properly. It also times out if a software error is based on hardware-related problems.

The watchdog timer in the C868 is a 16-bit timer, which is incremented by a count rate of f_{SYS}/2 upto f_{SYS}/128. The machine clock of the C868 is divided by a prescaler, a divide-by-two or a divide-by-128 prescaler. The upper 8 bits of the Watchdog Timer can be preset to a user-programmable value via a watchdog service access in order to vary the watchdog expire time. The lower 8 bits are reset on each service access. **Figure 29** shows the block diagram of the watchdog timer unit.

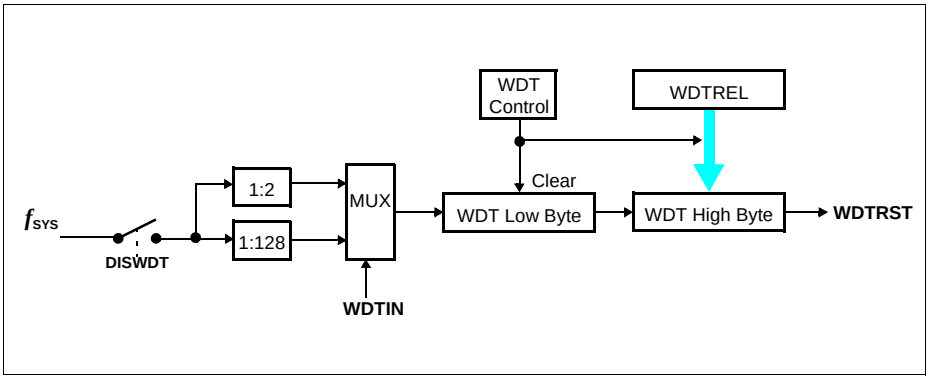

Figure 29 Block Diagram of the Programmable Watchdog Timer

After a reset, the Watchdog Timer is automatically enabled. If it is disabled, it cannot be enabled again during active mode of the device. If the software fails to clear the watchdog timer an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software (status flag WDTR in SCUWDT is set). A refresh of the watchdog timer is done by setting bits WDTRE and WDTRS (in

SFR SCUWDT) consecutively. This double instruction sequence has been implemented to increase system security.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes"). It is not possible to use the idle mode in combination with the watchdog timer function. Therefore, even the watchdog timer cannot reset the device when one of the power saving modes has been entered accidentally.

The time period for an overflow of the Watchdog Timer is programmable in two ways :

- **the input frequency** to the Watchdog Timer can be selected via bit WDTIN in register WDTCON to be either $f_{SYS}/2$ or $f_{SYS}/128$.
- **the reload value** WDTREL for the high byte of WDT can be programmed in register WDTCON.

The period P_{WDT} between servicing the Watchdog Timer and the next overflow can therefore be determined by the following formula:

[0.1]

$$P_{WDT} = \frac{2^{(1 + WDTIN*6)} * (2^{16} - WDTREL * 2^{8})}{f_{SYS}}$$

Table 14 lists the possible ranges for the watchdog time which can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 14 Watchdog Time Ranges

Reload value in WDTREL	Prescaler for f_{SYS}					
	2 (WDTIN = '0')			128 (WDTIN = '1')		
	40 MHz	20 MHz	16 MHz	40 MHz	20 MHz	16 MHz
FF_H	12.8 µs	25.6 µs	32.0 µs	819.2 µs	1.64 ms	2.05 ms
$7F_H$	1.65 ms	3.3 ms	4.13 ms	105.7 ms	211.3 ms	264 ms
00_H	3.28 ms	6.55 ms	8.19 ms	209.7 ms	419.4 ms	524 ms

For safety reasons, the user is advised to rewrite WDTCON each time before the Watchdog Timer is serviced.

Device Specifications

Absolute Maximum Ratings

Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature under bias	T_A	-40	125	°C	
Storage temperature	T_{STG}	-65	150	°C	-
Voltage on V_{DDP} pins with respect to ground (V_{SSP})	V_{DDP}	-0.3	4.6	V	-
Voltage on any pin except int/ analog and XTAL with respect to ground (V_{SSP})	V_{IN0}	-0.5	4.6	V	-
Voltage on any int/analog pin with respect to ground (V_{SSP})	V_{IN1}	-0.5	4.6	V	-
Voltage on XTAL pins with respect to ground (V_{SSC})	V_{IN2}	-0.5	4.6	V	-
Input current on any pin during overload condition	I_{OV}	-10	10	mA	-[1)]
Absolute sum of all input currents during overload condition	$\Sigma\|I_{OV}\|$	-	43	mA	-
Power dissipation	P_{DISS}	-	tbd	W	-

1) Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL2 etc.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DDP}$ or $V_{IN}<V_{SSP}$, $V_{IN2}>V_{DDC}$ or $V_{IN2}<V_{SSC}$) the voltage on V_{DDP} pin with respect to ground (V_{SSP}) must not exceed the values defined by the absolute maximum ratings.

Power Supply Current Calculation Formulae

Parameter		Symbol	Formula[1)]
Active mode	C868-1S	I_{DDPtyp}	0.25* f_{SYS} + 3.1
		I_{DDPmax}	0.26 * f_{SYS} + 5.2
	C868-1R	I_{DDPtyp}	0.27* f_{SYS} + 2.7
		I_{DDPmax}	0.29 * f_{SYS} + 3.9
Idle mode	C868-1S	I_{DDPtyp}	0.13* f_{SYS} + 2.6
		I_{DDPmax}	0.13 * f_{SYS} + 4.0
	C868-1R	I_{DDPtyp}	0.13* f_{SYS} + 3.7
		I_{DDPmax}	0.15 * f_{SYS} + 3.1
Active mode with slow-down enabled	C868-1S	I_{DDPtyp}	0.01 * f_{SYS} + 3.1
		I_{DDPmax}	0.02 * f_{SYS} + 3.6
	C868-1R	I_{DDPtyp}	0.01 * f_{SYS} + 3.2
		I_{DDPmax}	0.01 * f_{SYS} + 3.7
Idle mode with slow-down enabled	C868-1S	I_{DDPtyp}	0.01* f_{SYS} + 3.0
		I_{DDPmax}	0.01 * f_{SYS} + 3.8
	C868-1R	I_{DDPtyp}	0.02* f_{SYS} + 2.8
		I_{DDPmax}	0.02 * f_{SYS} + 3.3

1) f_{SYS} is in MHz and results in mA.

Clock calculation table for ADC

TVC[1]	32								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	322	386	450	514	578	642	706	770	t_{SYS}
t_S	64	128	192	256	320	384	448	512	t_{SYS}

TVC[1]	28								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	282	338	394	450	506	562	618	674	t_{SYS}
t_S	56	112	168	224	280	336	392	448	t_{SYS}

TVC[1]	24								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	242	290	338	386	434	482	530	578	t_{SYS}
t_S	48	96	144	192	240	288	336	384	t_{SYS}

TVC[1]	20								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	202	242	282	322	362	402	442	482	t_{SYS}
t_S	40	80	120	160	200	240	280	320	t_{SYS}

TVC[1]	16								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	162	194	226	258	290	322	354	386	t_{SYS}
t_S	32	64	96	128	160	192	224	256	t_{SYS}

TVC[1]	12								
STC[2]	2	4	6	8	10	12	14	16	t_{ADC}[3]
t_{ADCC}	122	146	170	194	218	242	266	290	t_{SYS}
t_S	24	48	72	96	120	144	168	192	t_{SYS}

TVC[1)]	8								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	82	98	114	130	146	162	178	194	t_{SYS}
t_S	16	32	48	64	80	96	112	128	t_{SYS}

TVC[1)]	4								
STC[2)]	2	4	6	8	10	12	14	16	t_{ADC}[3)]
t_{ADCC}	42	50	58	66	74	82	90	98	t_{SYS}
t_S	8	16	24	32	40	48	56	64	t_{SYS}

1) TVC is the clock divider specified by bit fields ADCTC.

2) STC is the sample time control specified by bit fields ADSTC.

3) t_{ADC} is t_{SYS}*TVC

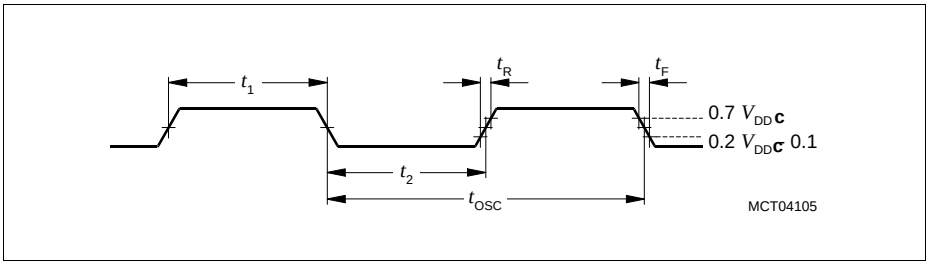

Figure 30 External Clock Drive on XTAL2

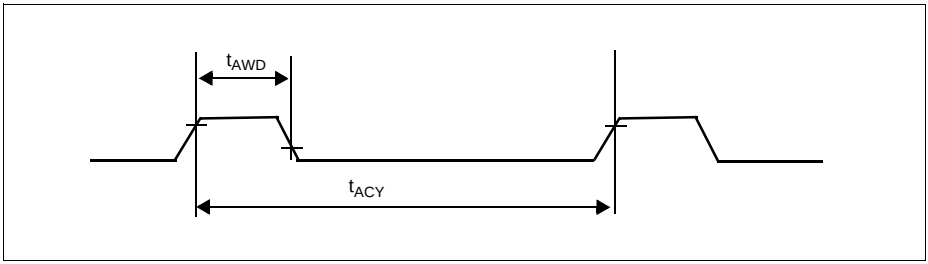

Figure 31 ALE Characteristic